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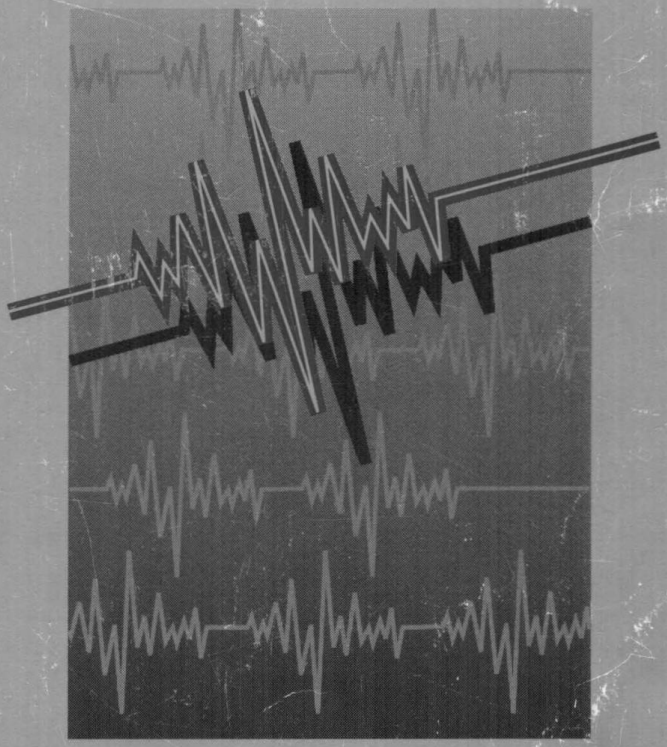
MIKROELEKTRONIKA MICROELECTRONICS

ANALOG

KOMUNIKACJA COMMUNICATIONS

PODRĘCZNIK HANDBOOK



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MICROELECTRONICS ANALOG COMMUNICATIONS HANDBOOK

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GENERAL INFORMATION

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INFORMATION

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Mitel Semiconductor

Mitel Semiconductor is an international supplier of mixed analog and digital telecommunication and data communication components. Since the founding of Mitel Semiconductor in 1976, the cornerstone of Mitel's success has been the innovative design of analog circuits such as tone-to-pulse converters, DTMF receivers and crosspoint switches.

Today, Mitel remains the leader in DTMF technology with products ranging from filters and decoders to completely integrated single chip DTMF receivers and transceivers. We have also developed a serial bus interface called the ST-BUS specifically for digital telecommunications and data communication applications. The ST-BUS is a bus architecture which simplifies the system design by providing a common set of functional parameters which are used synonymously on all ST-BUS circuits.

Mitel Semiconductor is dedicated to providing a system solution to all communication applications. This is justified by our vertical integration of products which consists of our Telecom IC's and hybrid family as well as a full line of board and software products.

To support our total systems solution concept, Mitel Semiconductor strives to contribute through every phase of the project implementation. This ranges from early consultation on technical feasibility to providing tools for product conception as well as after-sales service support.

Mitel Semiconductor has helped to set several ISDN standards and in the process has become recognized as the predominant supplier of complete ISDN solutions. Our constant innovation in new product development, teamed with superior applications support gives you the Mitel advantage. Also, Mitel Semiconductor has made a substantial investment in the quality assurance process with the result that all our customers receive a reliable product that meets or exceeds specifications every time.

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Zapewnienie jakości i niezawodności

Quality Assurance and Reliability

Zapewnienie jakości i niezawodności

As we prepare to enter the 1990's, it is increasingly apparent that traditional Quality Control activities are not sufficient to protect both the customer's and Mitel Semiconductor's best interests. To supplement the next generation of Mitel devices, a Quality system that is capable of withstanding the rigors of ever evolving customer needs, customer-supplier relationships and contractual agreements must be established. It is no longer sufficient to subject product to quality control gates and hope that probability theory will prevail and defective product detected and removed prior to shipment to the customer. Increasingly lower defect rates are not only common within the industry, they are demanded by cost conscious consumers who recognize the attendant cost of supporting a vendor who cannot or will not control his process and reduce or eliminate defects. With this in mind, Mitel Semiconductor has initiated programs that when fully implemented will provide the customer with a level of protection not easily achieved with traditional methods.

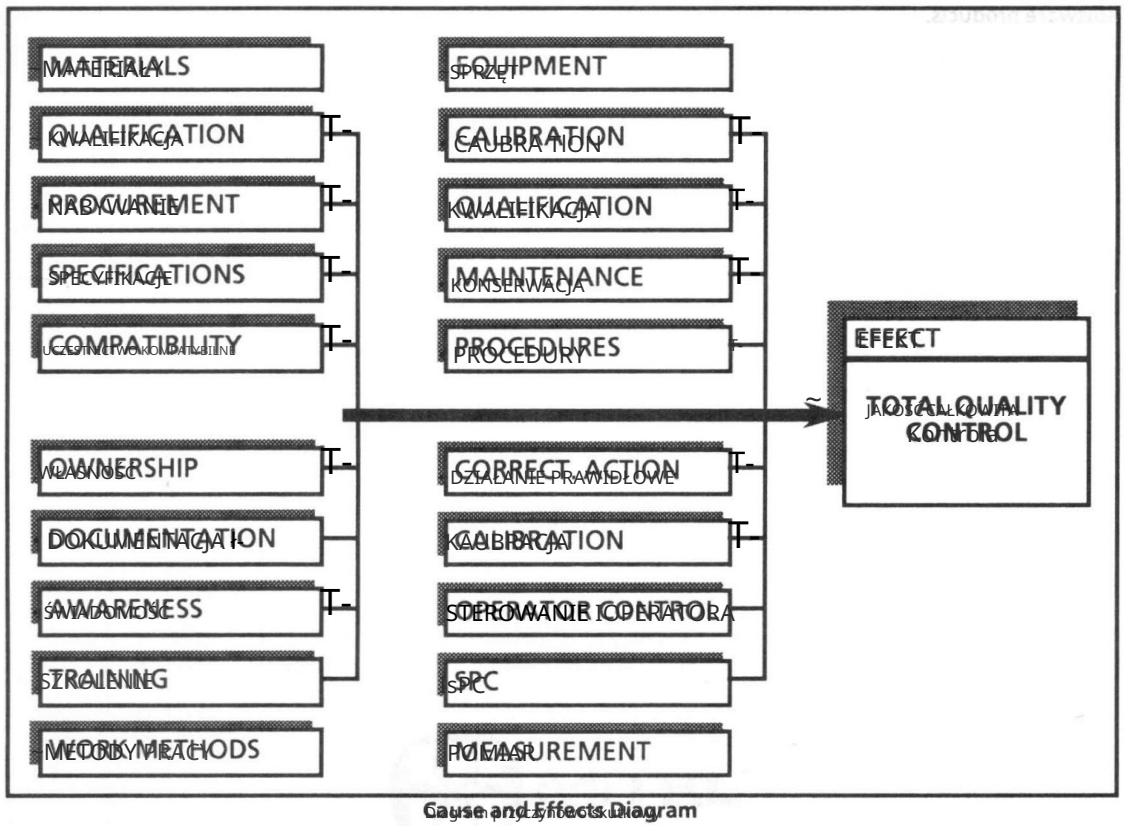
Gdy przygotowujemy się do wejścia w lata 90. XX wieku, coraz bardziej oczywiste, że tradycyjne działania w zakresie kontroli jakości nie są wystarczające, aby chronić zarówno klienta, jak i Mitel Semiconductor's najlepsze interesy. Aby uzupełnić następną generację urządzeń Mitel, należy ustanowić system jakości, który jest w stanie sprostać rygorom stale zmieniających się potrzeb klientów, relacji klient-dostawca i umów kontraktowych. Nie wystarczy już poddawać produkt bramkom kontroli jakości i liczyć na to, że prawdopodobieństwo wygra i wykryty i usunięty wadliwy produkt przed wysyłką do klienta. Coraz niższe wskaźniki defektów nie tylko są powszechne w branży, ale są wymagane przez świadomych kosztów konsumentów, którzy rozpoznają towarzyszące koszty utrzymania dostawcy, który nie może lub nie chce kontrolować swojego procesu i zredukować lub wyeliminować wady. Mając to na uwadze, firma Mitel Semiconductor zainicjowała programy, które po pełnym wdrożeniu zapewnią klientowi poziom ochrony, którego nie można łatwo osiągnąć tradycyjnymi metodami.

Leading the way in the quest for higher quality is the adoption of the International Standards Organization (ISO) 9000 or the American National Standards Institute (ANSI)/American Society for Quality Control (ASQC) Q90 series of Quality Systems. The principal objective of these systems is the achievement and sustaining of the customer's needs. With approval already granted to ISO 9001 (also known as British Standard (BS) 5750 in the United Kingdom) for the thick film hybrid facility and target dates of late 1990 for the integrated circuit facilities, Mitel Semiconductor is proceeding to establishing the foundation of a more efficient and effective quality management system.

Przewodząc w dążeniu do wyższej jakości, przyjęcie międzynarodowych standardów Organizacja (ISO) 9000 lub amerykańska organizacja krajowa Instytut Norm (ANSI)/Amerykańskie Towarzystwo Kontroli Jakości (ASQC) Seria Q90 kontroli jakości systemy. Głównym celem tych systemów jest osiągnięcie i podtrzymanie potrzeb klienta. Z uwzględnieniem zatwierdzonym już dla ISO 9001 (znana również jako Brytyjska Norma (BS) 5750 w Zjednoczone Królestwo) dla hybrydowego zakładu produkującego grube warstwy i docelowe daty na koniec 1990 r. dla zintegrowanego w zakładach produkujących obwody, Mitel Semiconductor kontynuuje do ustanowienia fundamentów bardziej wydajnego i skutecznego systemu zarządzania jakością.

In addition to the management system, progressive actions such as statistical process control (SPC) and design of experiments (focusing on Taguchi methods) will also yield significant return on investment as the emphasis migrates from reaction or screening to a system of prevention. The implementation of a system of prevention will then allow for the ownership of quality to be transferred to the production floor, with defect rates no longer being controlled through Quality Control acceptance sampling.

Oprócz systemu zarządzania podejmowane będą działania takie jak kontrola procesu statystycznego (SPC) i projektowanie eksperymentów (skupiając się na Taguchi metody) również przyniosą znaczący zwrot z inwestycji inwestycji, ponieważ nacisk przenosi się z reakcji od przesiewowego systemu zapobiegania. Wdrożenie systemu zapobiegania da wówczas możliwość przekazania własności jakości do produkcji podłogi, z wadami defektów nie są już kontrolowane poprzez kontrolę jakości akceptacji próbkowania.



Cause and Effects Diagram

Przyczyna i skutki

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The role of the Quality Assurance department is beginning to evolve from a policing authority to that of an audit confirming position serving to monitor the continued compliance to the processes and systems installed. The Cause and Effect diagram illustrated on the previous page simplifies the new tasks involved in Quality Assurance, identifying the departures from conventional techniques and the comprehensiveness of a total quality control system. From basics such as operator training and awareness, to proactive steps such as ensuring material compatibility and preventive maintenance, all areas are critical in ensuring that the desired effect is continually achieved.

In addition to these process oriented controls, effective development methodologies designed to establish conformance to requirements from the early stages in the product evolution cycle, comprehensive ESD programs and employee training in total quality control concepts (based upon the Philip Crosby quality system) also contribute to the integrity of the Mitel product that the customer receives.

At Mitel, it is recognized that all of these actions are required to continually supply customers with quality products and services. In addition, evolving customer requirements such as just-in-time and dock-to-stock programs leave absolutely no room for error on the part of the supplier. The product must be correct and defect free when received, to avoid production downtime, missed commitments and lost billings.

To illustrate the quality system installed at Mitel Semiconductor and its various publications have been made available to customers. The first is a brochure entitled 'Delivering the Commitment' details the quality management system, and outlines all manufacturing flows including wafer processing, IC assembly and test, and hybrid manufacturing. The second is the 'Reliability Data Book', which is published annually and contains valuable information such as data from accelerated stress testing on products detailed within this data book and detailed explanations of the reliability monitor program. Encompassing steady state life, temperature humidity bias, and high accelerated stress testing (HAST) as well as mechanical testing such as temperature cycling, thermal shock and vibration, most questions relating to the reliability of Mitel product can be found in this publication. To obtain a copy simply call the nearest Sales representative and identify the publication required. In addition, your name will be added to the mailing list to ensure that subsequent Quality News releases are sent to you.

At Mitel "Delivering the Commitment" is the stated quality goal and only through the focus identified above will this goal be constantly achieved into the 1990's and beyond.

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MITEL SEMICONDUCTOR

During the last decade, Mitel has participated in virtually all aspects of the semiconductor industry: as an innovative designer of telecommunications components and digital devices as a pioneer of the ISO-CMOS process, and as a participant in the merchant components market. Increasingly, companies need to obtain custom and semi-custom devices to survive in today's highly competitive market. Mitel offers the following range of services and facilities to design engineers for co-operative production of custom and semi-custom devices.

Design

The Mitel wafer foundry accepts customers designs in the form of a database tape, Pattern Generation (PG) tape, or a set of photo-masks.

Mitel Semiconductor supplies design rules and electrical parameters to customers who have the resources to produce their own design tooling.

Full design services are available through design houses. Complete information about this service is available upon request.

Wafer Foundry

This state of the art facility comprises:

- A 9,500 square foot wafer fab area consisting of class 100 clean room modules.
- A 5,000 square foot process development area.

The foundry currently processes silicon gate, P-well CMOS wafers in 5, 4, 3 and 2 micron geometries, and is compatible with a number of other major foundries. Double layer polysilicon is available on all processes, and there are a number of processes that can support double level metalizations.

A 9 micron metal gate CMOS process is offered for high voltage applications.

Fabrication equipment includes medium and high current implanters, plasma etching equipment, sputtering, projection alignment and direct step on wafer. The foundry maintains tight parametric control and consistently achieves high yields.

Mask Making

In order to achieve optimum yields and simplify the interface to the foundry, many customers find it convenient to have the Mitel photomask shop prepare the photomasks for their production requirements. The Mitel photomask shop uses optical pattern generation techniques to create high quality projection master plates from GDS-1 or GDS-2 database tapes or Mann 3000, Mann 3600 and Emask 2000 PG tapes.

Device Testing

Mitel has available the following equipment for wafer probe and final testing of devices:

- LTX with DX80 or 90 and full DSP capability
- Fairchild Sentinel and Sentry VII
- Megatest Q2/62

Prototype Packaging

Mitel Semiconductor offers rapid turn around on prototype packaging and supplies a complete choice of hermetic packages: Cerdip, Side-brazed DIP and Leadless Chip Carrier.

Mitel qualified subcontractors perform plastic packaging for prototyping or high volume assembly.

Customer Service

Mitel Semiconductor customer service is as important as being an important aspect of our wafer foundry business. The throughput commitment that Mitel measures itself against is a five week turnaround in wafer fabrication. Should photomask making be required, or wafer probing, an additional week would be required for each step.

Beyond this, the customer service group in Bromont, Quebec prides itself on the availability of timely information about the position and forecasted due-out date of foundry wafers. Whether by telephone or electronic mail, customers are kept well informed about the progress of their wafers as they move through the fabrication process.

CMOS Process Options

Several process options are available to customers at Mitel depending upon their needs. The process options listed in the following tables are given for guidance only. Many of the specific process parameters can be adjusted to suit customer requirements. For full process specifications, contact a Mitel Sales Office or representative.

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Gate Size 5 micron, High Threshold

Rozmiar bramki 5 mikron, wysoki próg

Parameter		N-Channel Kanał n	P-Channel Kanał p
Threshold Voltage Napięcie progowe	(volts @ 0µA) (wolty przy 0µA)	0.6 ÷ 1.2	0.6 ÷ 1.2
Field Threshold Próg pola	(Volts) (Wolty)	≥ 18	≥ 18
Breakdown Voltage BV_{DSS} Napięcie przebicia BV_{DSS}	(Volts) (Wolty)	≥ 18	≥ 18
K' K'	(µA/Volt²) (µA/Wolt²)	26.0	10.0
Body Effect Coefficient Współczynnik efektu ciała	(Volt$^{\frac{1}{2}}$) (Wolt$^{\frac{1}{2}}$)	1.10	0.55
Effective Channel Length Efektywna długość kanału	(µm) (µm)	3.0	3.4
Gate Oxide Thickness Grubość tlenku bramki	(Å) (Å)	800	800
Sheet Resistivity Rezystywność powierzchniowa	(Ohms/square) (Omów/kwadrat)	18 ÷ 38	40 ÷ 90
Polysilicon I Gate Resistivity Polisilikon I Rezystywność bramki I	(Ohms/square) (Omów/kwadrat)	14 ÷ 26	14 ÷ 26
Polysilicon II Resistivity Rezystywność polisilikonu II	(Ohms/square) (Omów/kwadrat)	30 ÷ 80	30 ÷ 80
Poly I to Poly II Capacitance Pojemność Poly I do Poly II	(10.4 pF/µm²) (10.4 pF/µm²)	6.0	
Metal Width/Spacing Szerokość/Odstęp metalu	(µm) (µm)	5/5	
Second Layer Metal Option Opcja drugiej warstwy metalu		None	
Process Compatibility Proces kompatybilności		AMI	

Gate Size 5 micron, Low Threshold

Rozmiar bramki 5 mikron, niski próg

Parameter		N-Channel Kanał n	P-Channel Kanał p
Threshold Voltage Napięcie progowe	(volts @ 0µA) (wolty przy 0µA)	0.4 ÷ 0.9	0.4 ÷ 0.9
Field Threshold Próg pola	(Volts) (Wolty)	≥ 18	≥ 18
Breakdown Voltage BV_{DSS} Napięcie przebicia BV_{DSS}	(Volts) (Wolty)	≥ 18	≥ 18
K' K'	(µA/Volt²) (µA/Wolt²)	26.0	10.0
Body Effect Coefficient Współczynnik efektu ciała	(Volt$^{\frac{1}{2}}$) (Wolt$^{\frac{1}{2}}$)	1.10	0.55
Effective Channel Length Efektywna długość kanału	(µm) (µm)	1.8	2.8
Gate Oxide Thickness Grubość tlenku bramki	(Å) (Å)	800	800
Sheet Resistivity Rezystywność powierzchniowa	(Ohms/square) (Omów/kwadrat)	6 ÷ 14	70 ÷ 110
Polysilicon I Gate Resistivity Polisilikon I Rezystywność bramki I	(Ohms/square) (Omów/kwadrat)	14 ÷ 26	14 ÷ 26
Polysilicon II Resistivity Polisilikon II Rezystywność	(Ohms/square) (Omów/kwadrat)	30 ÷ 80	30 ÷ 80
Poly I to Poly II Capacitance Pojemność Poly I do Poly II	(10.4 pF/µm²) (10.4 pF/µm²)	4.8	
Metal Width/Spacing Szerokość/Odstęp metalu	(µm) (µm)	5/5	
Second Layer Metal Option Opcja drugiej warstwy metalu		None	
Process Compatibility Proces kompatybilności		GTE Plessey	

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Optional Process Options

Gate Size: 4 micron

Parameter		N-Channel	P-Channel
Threshold Voltage (Napięcie progowe)	(volts @ 0µA) (Wolty przy 0µA)	0.4 - 0.9	0.4 - 0.9
Field Threshold (Pole progowe)	(Volts) (Wolty)	> 12	> 12
Breakdown Voltage BV_{dss} (Napięcie przebicia BV_{dss})	(Volts) (Wolty)	> 15	> 15
K'	(µA/Volt²) (µA/Volt²)	32.0	13.0
Body Effect Coefficient (Współczynnik efektu ciała)	(Volt$^{\frac{1}{2}}$) (Wolt$^{\frac{1}{2}}$)	0.90	0.45
Effective Channel Length (Efektywna długość kanału)	(µm) (µm)	1.6	2.6
Gate Oxide Thickness (Grubość izolatora bramki)	(Å) (Å)	640	640
Sheet Resistivity (Rezystywność powierzchniowa)	(Ohms/square) (Omów/kwadrat)	6 - 14	70 - 110
Polysilicon I Gate Resistivity (Polisilikon I Rezystywność bramki I)	(Ohms/square) (Omów/kwadrat)	14 - 26	14 - 26
Polysilicon II Resistivity (Rezystywność polikrzemu II)	(Ohms/square) (Omów/kwadrat)	30 - 80	30 - 80
Poly I to Poly II Capacitance (Pojemność Poly I do Poly II)	(10.4 pF/µm²) (10.4 pF/µm²)	4.8	
Metal Width/Spacing (Szerokość/odstęp ścieżek metalu)	(µm) (µm)	4 / 4	
Second Layer Metal Option (Opcja drugiej warstwy metalu)		None	
Process Compatibility (Kompatybilność procesu)		GTE Plessey	

Gate Size: 3 Micron

Parameter		N-Channel	P-Channel
Threshold Voltage (Napięcie progowe)	(volts @ 0µA) (Wolty przy 0µA)	0.6 - 1.0	0.6 - 1.0
Field Threshold (Pole progowe)	(Volts) (Wolty)	> 12	> 12
Breakdown Voltage BV_{dss} (Napięcie przebicia BV_{dss})	(Volts) (Wolty)	> 10	> 10
K'	(µA/Volt²) (µA/Volt²)	43.5	16.0
Body Effect Coefficient (Współczynnik efektu ciała)	(Volt$^{\frac{1}{2}}$) (Wolt$^{\frac{1}{2}}$)	0.43	0.53
Effective Channel Length (Efektywna długość kanału)	(µm) (µm)	2.4	2.2
Gate Oxide Thickness (Grubość izolatora bramki)	(Å) (Å)	480	480
Sheet Resistivity (Rezystywność powierzchniowa)	(Ohms/square) (Omów/kwadrat)	20 - 35	80 - 120
Polysilicon I Gate Resistivity (Polisilikon I Rezystywność bramki I)	(Ohms/square) (Omów/kwadrat)	15 - 30	15 - 30
Polysilicon II Resistivity (Rezystywność polikrzemu II)	(Ohms/square) (Omów/kwadrat)	75 - 125	75 - 125
Poly I to Poly II Capacitance (Pojemność Poly I do Poly II)	(10.4 pF/µm²) (10.4 pF/µm²)	4.8	
Metal Width/Spacing (Szerokość/odstęp ścieżek metalu)	(µm) (µm)	3 / 3	
Second Layer Metal Option (Opcja drugiej warstwy metalu)		Yes	
Process Compatibility (Kompatybilność procesu)		GTE LMP	

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Gate Size: 2.5 Micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0 µA)	0.6 - 1.0	0.6 - 1.0
Field Threshold	(Volts)	≥ 12	≥ 12
Breakdown Voltage BV_{dss}	(Volts)	≥ 10	≥ 10
K'	(µA/Volt²)	47.5	12.4
Body Effect Coefficient	(Volt$^{\frac{1}{2}}$)	0.44	0.47
Effective Channel Length	(µm)	1.9	1.9
Gate Oxide Thickness	(Å)	400	400
Sheet Resistivity	(Ohms/square)	20 - 35	80 - 120
Polysilicon 1 Gate Resistivity	(Ohms/square)	15 - 30	15 - 30
Polysilicon 1 Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly to Poly Capacitance	(0.44 pF/µm²)	5.3	
Metal Width/Spacing	(µm)	3/3	
Second Layer Metal Option		Yes	
Process Compatibility		None	

Gate Size: 2 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0 µA)	0.5 - 0.9	0.5 - 0.9
Field Threshold	(Volts)	≥ 12	≥ 12
Breakdown Voltage BV_{dss}	(Volts)	≥ 10	≥ 10
K'	(µA/Volt²)	65	22
Body Effect Coefficient	(Volt$^{\frac{1}{2}}$)	0.31	0.26
Effective Channel Length	(µm)	1.8	1.65
Gate Oxide Thickness	(Å)	325	325
Sheet Resistivity	(Ohms/square)	30 - 50	85 - 115
Polysilicon 1 Gate Resistivity	(Ohms/square)	15 - 25	15 - 25
Polysilicon 1 Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly to Poly Capacitance	(0.44 pF/µm²)	6.9	
Metal Width/Spacing	(µm)	2/2.5	
Second Layer Metal Option		Yes	
Process Compatibility		None	

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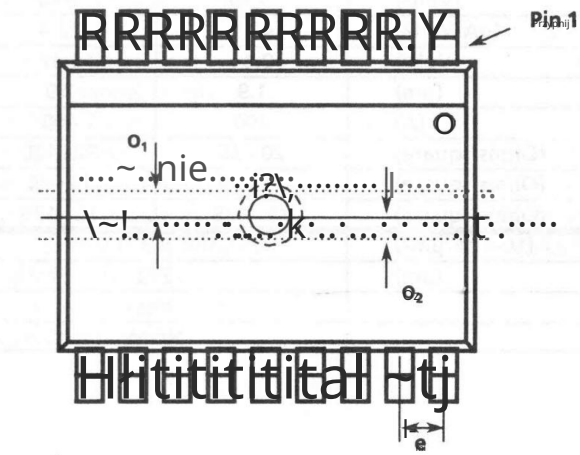
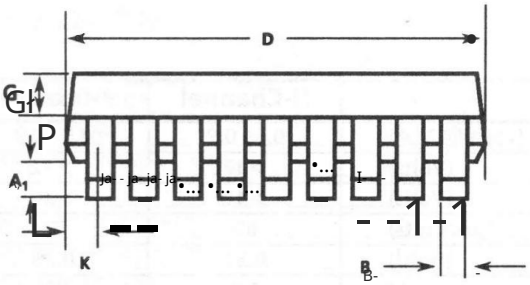
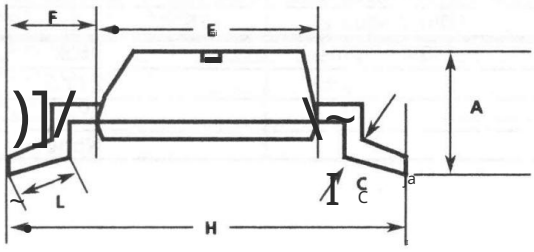
PACKAGING OUTLINES







DIM	18-Pin SOIC		20-Pin SOIC	
	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.447 (11.35)	0.469 (11.90)	0.496 (12.60)	0.518 (13.00)
E	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
F	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)
G	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
K	0.035 (0.889)	0.045 (1.143)	0.035 (0.889)	0.045 (1.143)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)
θ_1	-	0.005 (0.13)	-	0.005 (0.13)
θ_2	-	0.005 (0.13)	-	0.005 (0.13)

NOTE: (.) millimeters

NOTES:
1) A & B Maximum dimensions include allowable mold flash.
2) θ_1 & θ_2 are SYMMETRY dimensions.

Lead SOIC Package (S Suffix)

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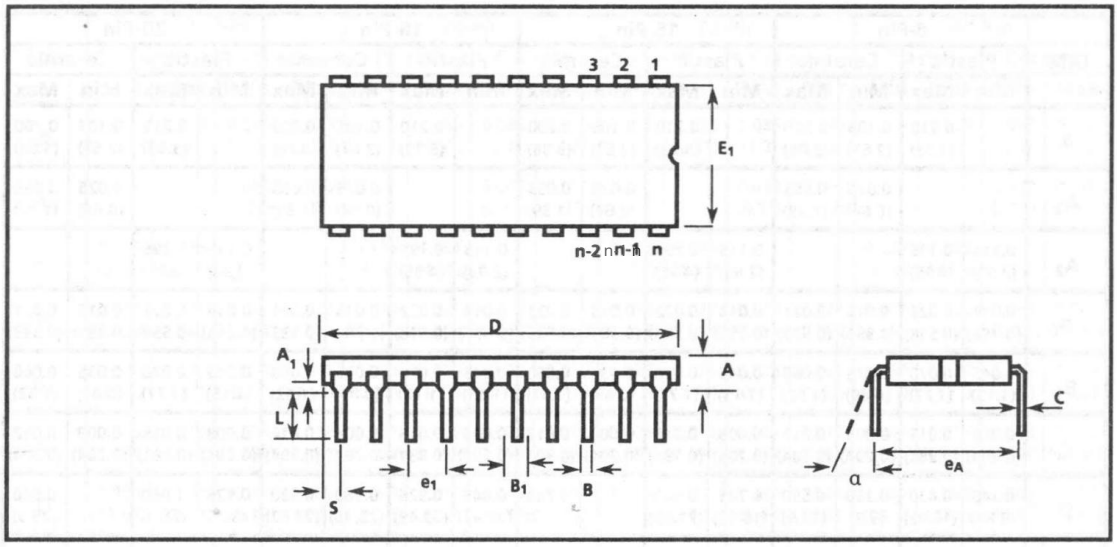
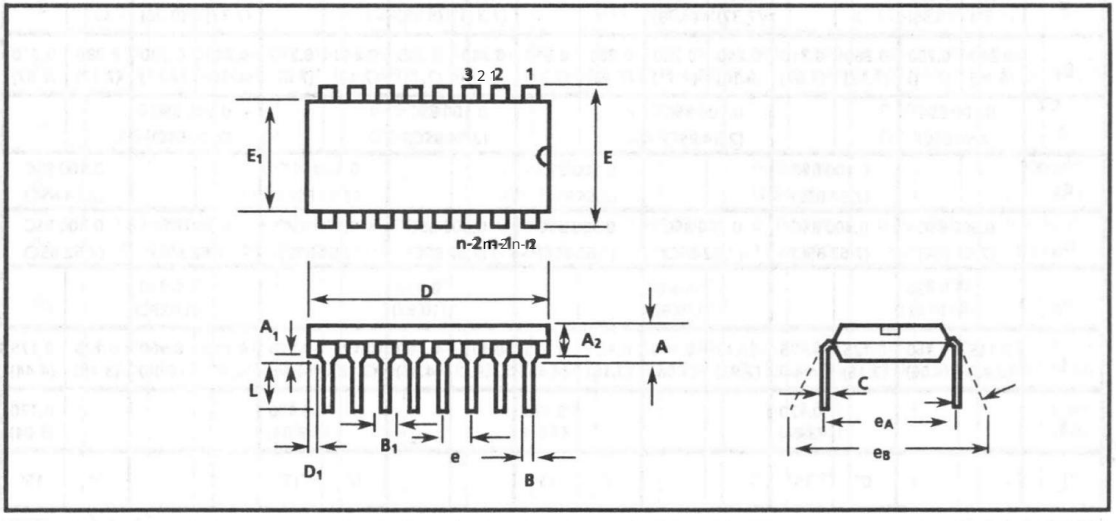


Ceramic Dual-In-Line Packages (CDIP) - C Suffix
Ceramiczne pakiety Dual-In-Line (CDIP) - sufiks C



Plastic Dual-In-Line Packages (PDIP) - E Suffix
Plastikowe opakowania Dual-In-Line (PDIP) - sufiks E

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Package Dimensions

DIM	8-Pin				16-Pin				18-Pin				20-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)
A_1			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)
A_2	0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)
B_1	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	0.348 (8.84)	0.430 (10.92)	0.380 (9.7)	0.550 (13.9)	0.745 (18.93)	0.840 (21.33)		0.784 (19.9)	0.845 (21.47)	0.925 (23.49)	0.880 (22.36)	0.980 (23.62)	0.925 (23.49)	1.060 (26.9)		0.996 (25.3)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)		
E_1	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_{m1}			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (2.54 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)	
e_B		0.430 (10.92)				0.430 (10.92)				0.430 (10.92)				0.430 (10.92)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

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DIM	22-Pin				24-Pin				28-Pin				40-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.090 (2.29)	0.225 (5.71)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)
A_1			0.025 (0.64)	0.055 (1.39)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)
A_2	0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)
B_1	0.045 (1.15)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	1.050 (26.67)	1.120 (28.44)	1.040 (26.42)	1.260 (32.0)	1.150 (29.3)	1.290 (32.7)	1.180 (29.88)	1.291 (32.80)	1.380 (35.1)	1.565 (39.7)	1.380 (35.06)	1.520 (38.61)	1.980 (50.3)	2.095 (53.2)	1.980 (50.30)	2.110 (53.60)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.390 (9.91)	0.430 (10.92)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)		
E_1	0.330 (8.39)	0.380 (9.65)	0.350 (8.89)	0.410 (10.41)	0.485 (12.32)	0.580 (14.73)	0.516 (13.1)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.618 (15.70)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.400 BSC (10.16 BSC)		0.400 BSC (10.16 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)	
e_B		0.500 (12.70)				0.700 (17.78)				0.700 (17.78)				0.700 (17.78)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.100 (2.54)				0.800 (2.05)				0.800 (2.05)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

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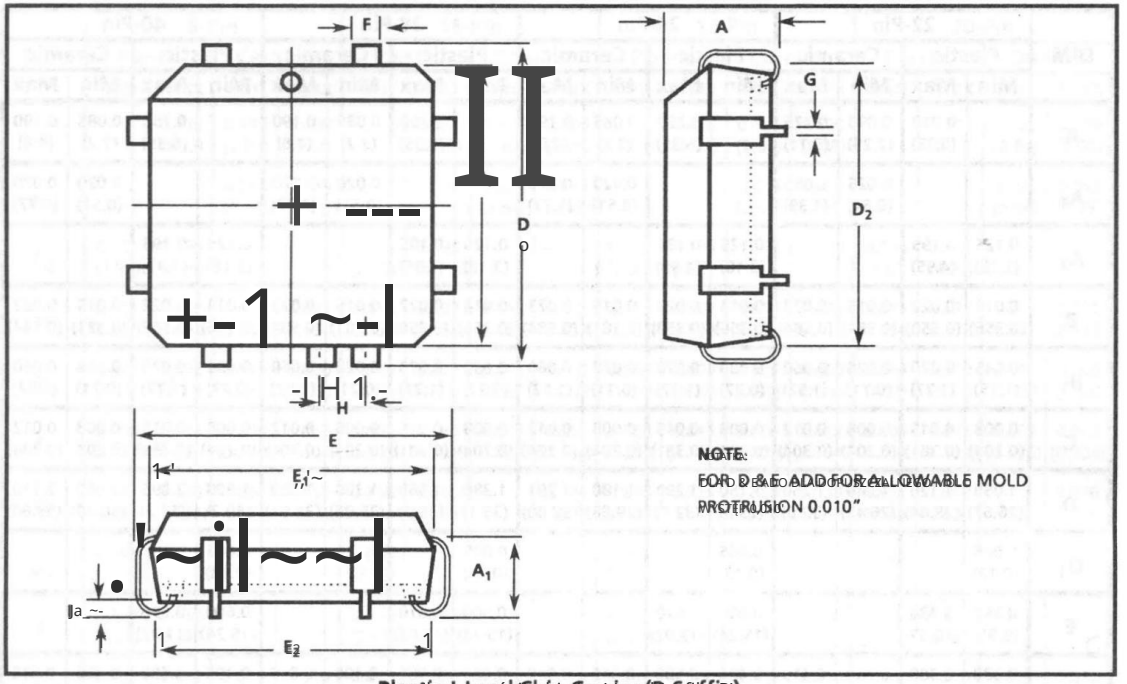

Plastic Leaded Chip Carrier (R Suffix)

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DIM	20-Pin PLCC		28-Pin PLCC		44-Pin PLCC		68-Pin PLCC		84-Pin PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
B			0.020 TP (0.51 TP)							
B_1										
B_2										
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D_4/E_4										
e			0.050 BSC (1.27 BSC)							
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)				0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
h			0.040 BSC (1.02 BSC)							
h_1										
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
L										
L_1										
R_1										

NOTE: ( ) Millimeters

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Tube Quantities

PIN COUNT	DEVICE QUANTITY BY PACKAGE TYPE					
	PLASTIC DIP	PLCC	SOIC	CERDIP	LCC	SIDE BRAZE
8	50	-	-	-	-	-
16	25	-	-	24	-	-
18	21	-	41	20	-	-
20	18	-	37	19	-	-
22	17	-	-	17	-	-
24	15	-	-	15	47	-
28	13	38	-	13	42	12
40	9	-	-	9	-	9
44	-	27	-	-	29	-
68	-	19	-	-	-	-
84	-	16	-	-	-	-

Standard IC Tube Quantity

Note: Standard IC shipping tube length is 50 cm ± 0.2 cm (19.75 in ± 0.08 in)

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Ordering Information
Informacje o zamówieniu

Part Number Identification
Identyfikacja numeru katalogowego

Mitel Semiconductor products are identified by a prefix defining the product family, a device type designation number, a specification suffix and a package suffix. The specification suffix defines variants of a particular device type and its significance is described in the data sheet of the device concerned. The package suffix defines the package type, refers to drawings in the data book section "Package Outlines" and identifies the package style. The first page of each data sheet carries a section named "Ordering Information" which shows the full part number for each of the variants and package styles available for the device, and should be consulted to determine the correct part number for ordering purposes. A breakdown of a typical part number is shown below for reference.

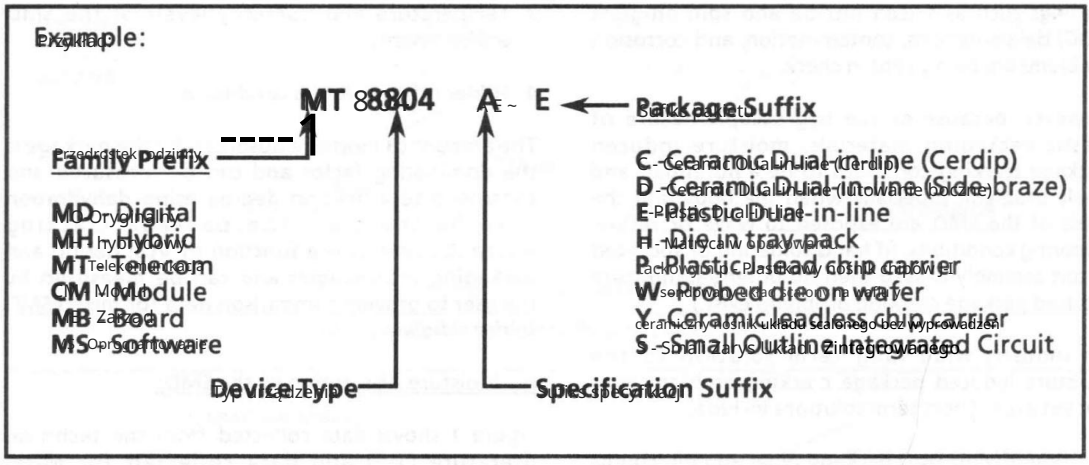
Produkty firmy Mitel Semiconductor są identyfikowane za pomocą prefiksu definiującego rodzinę produktów, numeru oznaczenia typu urządzenia, sufiksu specyfikacji i sufiksu obudowy. Sufiks specyfikacji definiuje warianty danego typu urządzenia, a jego znaczenie jest opisane w karcie katalogowej danego urządzenia. Sufiks obudowy określa typ obudowy, odnosi się do rysunków w sekcji „Package Outlines" w katalogu danych i identyfikuje styl obudowy. Pierwsza strona każdej karty katalogowej w sekcji zawiera informacje dla całej rodziny i części dla każdego wariantu. Należy zapoznać się z tą sekcją, aby określić prawidłowy numer części do celów zamówienia. Poniżej przedstawiono podział typowego numeru części w celu uzyskania informacji.

Advance and Preliminary Data
Dane wstępne i wstępne

Some data sheets carry the designation "Advance" or "Preliminary". Advance information represents the design objective for a device type in developement and may be revised without notice before the device reaches production. Preliminary information is intended for design guidance purposes and refers to a device type in production where device characterization is ongoing and information is still subject to change without notice. Current information on the status of Advance or Preliminary programs may be obtained from Mitel Sales Offices, Representatives, or Distributors.

Niektóre arkusze danych mają oznaczenie „Advance" lub „Preliminary". Informacje Advance przedstawiają cel projektowy dla typu urządzenia w fazie rozwoju i mogą zostać zmienione bez powiadomienia przed osiągnięciem produkcji. Informacje wstępne są przeznaczone do celów wskazówek projektowych dotyczących typu urządzenia w produkcji, gdzie charakterystyka urządzenia jest w toku i informacje mogą ulec zmianie bez powiadomienia. Aktualne informacje na temat programów Advance lub Preliminary można uzyskać w biurach sprzedaży Mitel, przedstawicieli lub dystrybutorów.

Example:
Przykład:



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Obudowy SMD, kontrola wilgoci i lutowanie rozpływowe

1.0 Wprowadzenie

Coraz powszechniejsze stosowanie elementów montowanych powierzchniowo (SMD), takich jak plastikowe nośniki układów scalonych (PLCC) i małe układy scalone (SOIC) zamiast tradycyjnych elementów lutowanych przewlekanie, uwypukliło nowe problemy związane z niezawodnością .

Poddanie obudów SMD procesom montażu rozpływowego lutowania ujawniło nastę pujące problemy:

1. Pę kanie opakowań spowodowane wilgocią (znane również jako efekt „popcornu”)

2. Rozwarstwienie matrycy i/lub ramki wyprowadzeń prowadzące do gromadzenia się zanieczyszczeń lub korozji.

Dzię ki postę pom w konstrukcji materiałów ramek wyprowadzeń (miedź zastę pująca Alloy-42 w celu poprawy dopasowania termicznego mię dzy ramką wyprowadzeń a plastikiem), promotorom przyczepności ramek wyprowadzeń (w celu poprawy łączenia plastiku z ramką wyprowadzeń) ulepszeniom w konstrukcji ramek wyprowadzeń (otwory blokujące wyprowadzenia i zmniejszenie padów mocujących matrycę w celu utworzenia pojedynczego monolitu zamiast górnej i dolnej kanapki z matrycą i ramką wyprowadzeń pomię dzy nimi) oraz ulepszonym powłokom górnym matrycy, takim jak azotek krzemu i rozwarstwienia typu SOG (spin-on-glass), problemy związane z zanieczyszczeniami i korozją są utrzymywane pod kontrolą .

Jednakże ze wzglę du na higroskopijną naturę materiałów opakowaniowych z tworzyw sztucznych, pę kanie opakowań pod wpływem wilgoci nadal stanowi potencjalny i kosztowny problem, zwłaszcza gdy obudowa i wyprowadzenia SMD są narażone na warunki lutowania falowego lub rozpływowego. (Jeśli stosuje się lutowanie rę czne lub montaż obwodów w gniazdach , nie wystę puje potencjalny problem pę kania opakowań pod wpływem wilgoci).

Długoterminowe rozwiązanie problemu pę kania opakowań wywołanego wilgocią nie jest weryfikowalne w całej branży . Krótkoterminowe rozwiązania obejmują:

1. Identyfikacja typów obudów SMD i liczby pinów o najwyższym ryzyku.

2. Pomiar progów poziomu pochłonię tej wilgoci dla SMD.

3. Wykonanie procesu odwadniania przed lutowaniem SMD.

W niniejszym biuletynie opisano prace, które Mitel Semiconductor wykonał w celu zidentyfikowania typów obudów wysokiego ryzyka i liczby pinów oraz określenia progów wilgotności dla tych obudów SMD. Zawarto również szczegóły dotyczące sposobu przeprowadzania wypalania odwadniającego przed lutowaniem.

2.0 Charakterystyka sorpcji wilgoci .

Wilgoć jest absorbowana z otoczenia przez plastikowy SMD i dyfunduje do opakowania zgodnie z prawem dyfuzji Ficksa. Ponieważ istnieje gradient dyfuzji wilgoci, stę żenie i lokalizacje wilgoci w opakowaniu nie są dokładnie znane, ale całkowitą ilość pochłonię tej wilgoci można obliczyć za pomocą:

(masa mokra - masa początkowa) / masa początkowa x 100 = % masy wchłonię tej.

Poziom desorpcji wilgoci uzyskany w wyniku pieczenia z odwodnieniem można łatwo obliczyć za pomocą:

(masa początkowa - masa po upieczeniu)/ masa początkowa x 100 = % masy po desorbcji.

Na pę kanie opakowań spowodowane wilgocią wpływają:

1. Charakterystyka absorpcji wilgoci przez SMD.

2. Próg pę kania obudowy SMD.

3. Temperatura i wilgotność otoczenia SMD.

4. Warunki procesu lutowania rozpływowego.

Ilość wilgoci pochłonię tej przez opakowanie jest czynnikiem dominującym i może być mierzona i kontrolowana w ograniczonym stopniu za pomocą pieczenia odwadniającego przez użytkownika. Poziom podatności na pę kanie opakowania jest funkcją VLSI design i technologii pakowania i może być mierzony przez użytkownika w celu zapewnienia danych porównawczych dla mieszanego lutowania rozpływowego SMD.

A. Absorpcja wilgoci przez SMD:

Rysunek 1 przedstawia dane zebrane z literatury technicznej (1-5) oraz dane zebrane dla SMD Mitel Semiconductor. Poziomy absorpcji wilgoci wię ksze niż 0,16-0,22% (wagowo) są uważane za podatne na pę kanie obudowy podczas lutowania rozpływowego.

B. Próg pę kania obudowy SMD :

Rysunek 2 łączy rozmiar matrycy i grubość podstawy pakietu, aby wytworzyć „OBSZAR BEZPIECZNY” i „OBSZAR PĘKNIĘCIA” opisany przez R. Lina (1,2).
Dane SMD firmy Mitel Semiconductor zostały dodane do tego wykresu na rysunku 3. Dane te są przydatne przy określaniu, czy konkretny SMD jest wzglę dnie bardziej podatny na pę knię cia w porównaniu z innym

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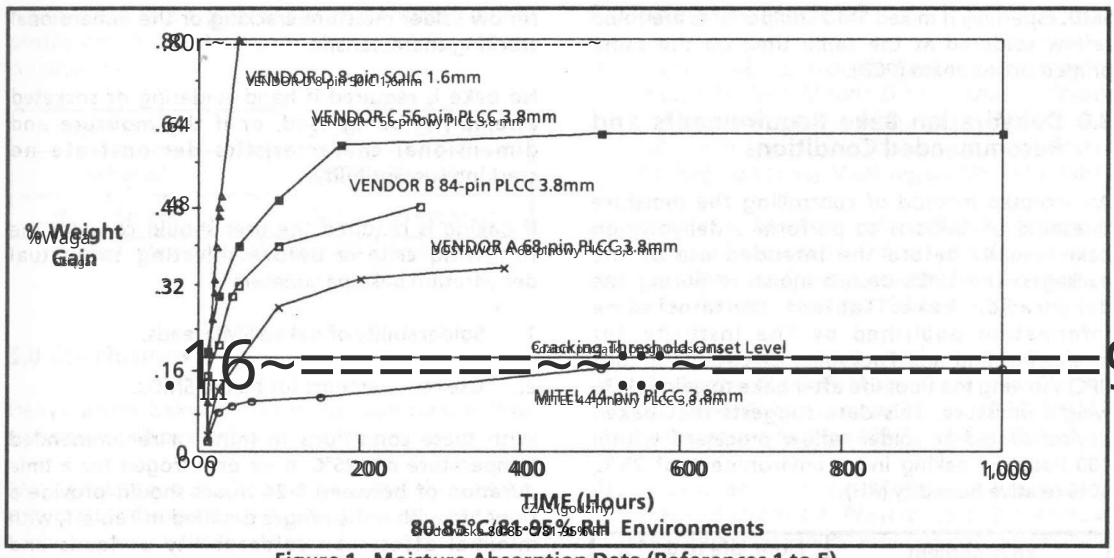

Figure 1. Moisture Absorption Data (References 1 to 5)

Rysunek 1. Dane dotyczące absorpcji wilgoci (odniesienia 1 do 5)

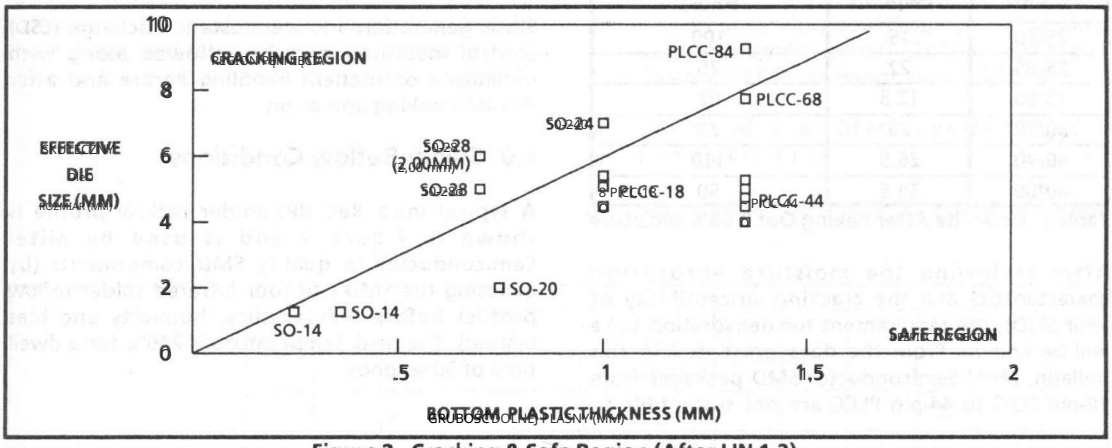

Figure 2. Cracking & Safe Region (After LIN 1,2)

Rysunek 2. Pęknięcia i bezpieczny region (po LIN 1,2)

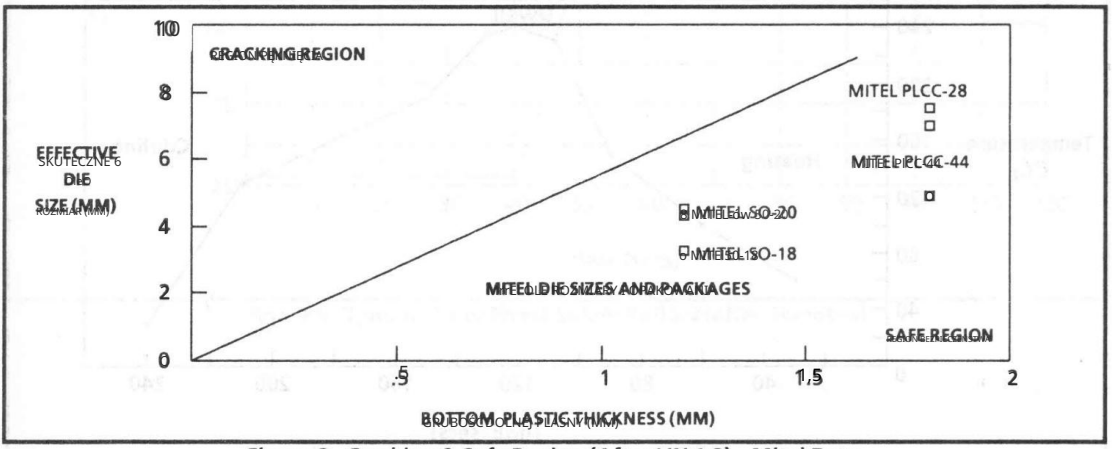

Figure 3. Cracking & Safe Region (After LIN 1,2) - Mitel Data

Rysunek 3. Pęknięcia i bezpieczny region (po LIN 1,2) Dane Mitel

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SMD, especially if they are SMD components are to be reflow soldered at the same time on the same printed circuit board (PCB).

3.0 Dehydration Bake Requirements and Recommended Conditions

An accepted method of controlling the moisture threshold of SMDs is to perform a dehydration bake, usually before the intended use of the packages. The SMDs desorb moisture during the dehydration bake. Table 1 contains some information published by The Institute for Interconnecting and Packaging Electronic Circuits (IPC) showing the floor life after bake to gain 0.11% weight moisture. This data suggests that baked devices should be solder reflow processed within 100 hours of baking in an environment of 25°C, 50% relative humidity (RH).

Environment		Floor Life to 0.11%
°C/%RH	Dewpoint	Hours
25/50	15	100
25/85	22	75
30/60	12.8	92
30/70	25	72
40/40	26.5	110
40/80	38.6	50

Table 1: Floor Life After Baking 0.005% Moisture

After reviewing the moisture absorption characteristics and the cracking susceptibility of your SMDs, the requirement for dehydration bake will be known. From the data presented in this bulletin, Mitel Semiconductor SMD packages from 18-pin SOIC to 44-pin PLCC are not susceptible to reflow solder moisture cracking or the dimensional cracking characteristic.

No bake is required if hand soldering or socketed assembly is being used, or if the moisture and dimensional characteristics demonstrate no cracking susceptibility.

If baking is required the user should consider the following criteria before selecting the actual dehydration bake parameter:

1. Solderability of baked SMD leads.

2. Use requirements for baked SMDs.

With these conditions in mind, a recommended temperature of 125°C in air or nitrogen for a time duration of between 8-24 hours should provide a floor life within the ranges detailed in Table 1, with minimal affect to solderability of leads and provide adequate floor life.

Static generation and electrostatic discharge (ESD) control measures must be followed along with minimized component handling before and after the SMD baking operation.

4.0 Solder Reflow Conditions

A typical Infra Red (IR) solder reflow profile is shown in Figure 4 and is used by Mitel Semiconductor to qualify SMD components (by exposing the SMD's to four infrared solder reflow profiles before temperature, humidity and bias testing). The peak temperature is 240°C for a dwell time of 30 seconds.

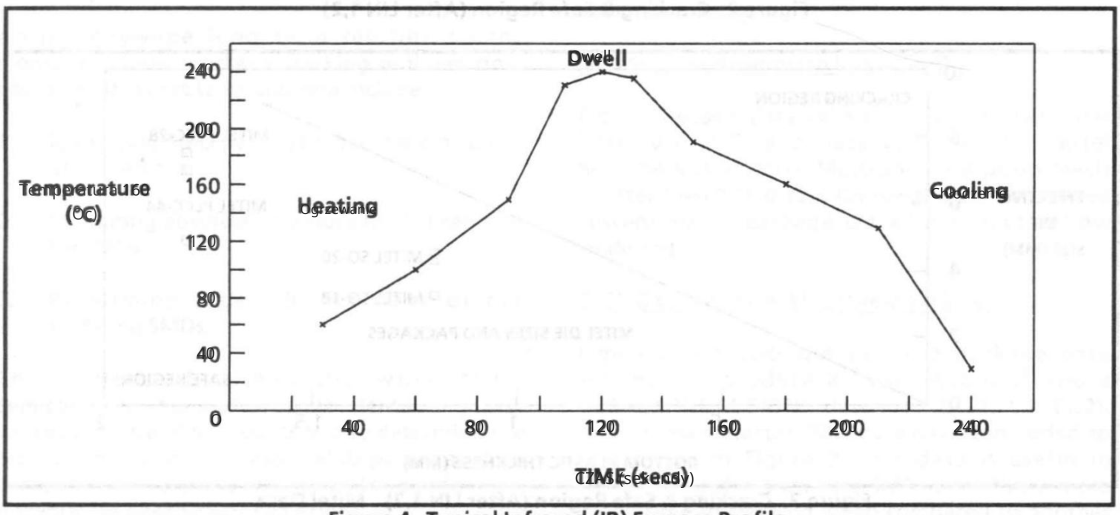

Figure 4. Typical Infrared (IR) Furnace Profile

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Figure 5 shows a typical vapor phase solder reflow profile and Table 2 contains other solder reflow conditions.

Rysunek 5 przedstawia typowy profil lutowania rozpływowego w fazie gazowej, a tabela 2 zawiera inne warunki lutowania rozpływowego.

Vapor Phase Faza parowa	220°C 60 seconds 220°C, 60 sekund
Infrared Podczerwień	240°C 30 seconds 240°C, 30 sekund
Wave Solder Lutowanie falowe	260°C 60 seconds 260°C, 60sekund

Table 2. Various Solder Reflow Conditions
Tabela 2. Różne warunki lutowania rozpływowego

5.0 Conclusions
5.0 Wnioski

Dehydration bake of Mitel Semiconductor SMD packages of 44 pins or less is not required.

Nie jest wymagane odwadnianie obudów SMD firmy Mitel Semiconductor zawierających 44 wyprowadzenia lub mniej.

SMD package sizes above 44 pins should be dehydration baked before solder reflow according to the procedure described above.

Obudowy SMD o rozmiarach powyżej 44 pinów przed lutowaniem rozpływowym należy poddać procesowi odwadniania, zgodnie z procedurą opisaną powyżej.

Mitel Semiconductor SMD packages can be dehydration baked at the conditions described in this bulletin and the packages can withstand four solder reflow profile conditions detailed in Figure 4.

Obudowy SMD firmy Mitel Semiconductor można poddać procesom odwadniania w warunkach opisanych w niniejszym biuletynie. Obudowy te wytrzymują cztery warunki profilu lutowania rozpływowego przedstawione na rysunku 4.

6.0 Reference Material
6.0 Materiał referencyjny

(1) R. Lin i in., Kontrola pękania obudów w urządzeniach montowanych powierzchniowo z tworzyw sztucznych podczas procesu lutowania, Materiały z 7. dorocznej (konferencji) Międzynarodowego Towarzystwa Pakowania Urządzeń Elektrycznych, s. 995-1010, 1987.

(2) R. Lin i in., Wilgotność obudowy w elementach montowanych powierzchniowo wywołane pękaniem z tworzywa sztucznego podczas procesu lutowania, IEEE IRPS Proceedings, 1988.

(3) Terry O. Steiner i David Suhl, Badania pękania dużych obudów PLCC podczas montażu powierzchniowego, IEEE/CHMT Transactions 10-2, s. 209-216, czerwiec 1987.

(4) I. Fukuzawa i in., Degradacja LSI z tworzywa sztucznego pod wpływem wilgoci w wyniku lutowania przepływowego, IEEE/IRPS Proceedings, s. 192-197, 1985.

(5) Satoshi Ito et al., Specjalne właściwości związków formujących do formowania małych urządzeń w opakowaniach o miniaturowych kształtach, IEEE Proceedings, s. 360-363, 1986.

(6) IPC-SM-786 Impact Of Moisture On Plastic IC Package Cracking.
Uderzenie wilgoci na układ scalony z tworzywa sztucznego Łamanie pakietów.

(7) Signetics SMD Reliability Data Update Section 4.
(7) Aktualizacja danych dotyczących niezawodności SMD firmy Signetics - sekcja 4.

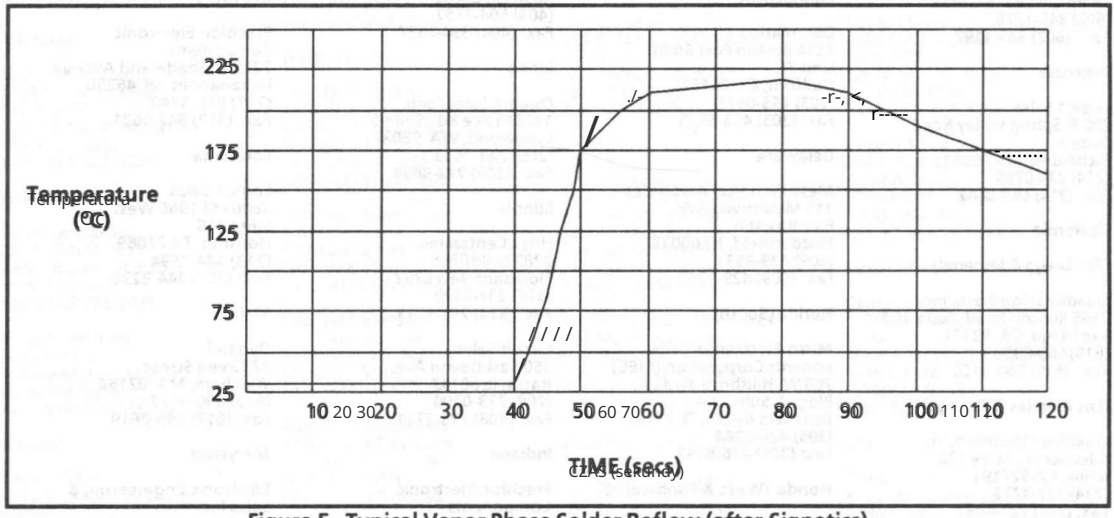

Figure 5. Typical Vapor Phase Solder Reflow (after Signetics)
Rysunek 5. Typowe lutowanie rozpływowe w fazie gazowej (według Signetics)

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Florida (West & Panhandle)

Micro-Electronics Components Corporation (MEC)
10637 Harborside Dr. N.
Largo, Florida 34643
(813) 393-5011
Fax: (813) 393-5202

Florida (Central, Orlando & East)

Micro-Electronics Components Corporation (MEC)
11 Emerald Court
Satellite Beach, FL
32937
(407) 773-1100
Fax: (407) 777-6529

Georgia

Southern Component Sales, Inc.
4146 Westchester Crossing
Roswell, GA 30075
(404) 594-7557
Fax: (404) 594-7537

Idaho

Quadra Sales Corp.
14231 Lakes Rd. Suite B,
Lynnwood, WA 98037
(206) 743-2633
Fax: (206) 742-9899

Illinois

Hitec Central Inc.
2282 Goldfinch
Florissant, MO 63031
(314) 291-5920
Fax: (314) 291-5713

Circuit Sales
650 East Devon Ave.
Itasca, IL 60143
(708) 773-0200
Fax: (708) 773-2721

Indiana

Precision Electronic Components
7202 N. Shadeland Ave.
Indianapolis, IN 46250
(317) 842-3740
Fax: (317) 842-0621

Iowa

Hitec Central Inc.
1644 26th St. N.W.
Cedar Rapids, IA 52405
(319) 396-3228
Fax: (319) 396-8025

Kansas

Hitec Central Inc.
803 Choctaw
Independence, MO 64056
(816) 796-6684
Fax: (816) 796-6562

Kentucky

Precision Electronic Components
7202 N. Shadeland Avenue
Indianapolis, IN 46250
(317) 842-3740
Fax: (317) 842-0621

Louisiana

Logic 1 Sales
4606 FM 1960 West
Suite 418
Houston, TX 77069
(713) 444-7594
Fax: (713) 444-8236

Maine

Dynasel
22 Green Street
Waltham, MA 02154
(617) 890-6777
Fax: (617) 899-0619

Maryland

Electronic Engineering & Sales Inc.
235 Prince George St.
Annapolis, MD 21401
(301) 269-4234
Fax: (301) 269-6476

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North American Representatives (cont'd.)

Massachusetts

Dynasel
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Michigan

Leading Edge Sales Corp.
28807 W. 8 Mile Road
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Livonia, MI 48152
(313) 478-6700
Fax: (313) 478-4026

Minnesota

Tecteam Sales Inc.
3050 Metro Dr. Ste 301
Minneapolis, MN 55425
(612) 854-6616
Fax: (612) 854-8031

Mississippi

Southern Component Sales, Inc.
307 Clinton Ave E, Ste 413
Huntsville, AL 35801
(205) 533-6500
Fax: (205) 533-6578

Missouri

Hitec Central Inc.
3466 Bridgeland Drive
Bridgeton, MO 63044
(314) 291-5920
Fax: (314) 291-5713

Hitec Central Inc.
803 Choctaw
Independence, MO 64056
(816) 796-6684

Montana

Gemini Electronics
8120 Sheridan Blvd.
Suite C-206
Arvada, CO 80003-6104
(303) 428-5600
Fax: (303) 428-5689

Nebraska

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1644 26th St. N.W.
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Fax: (319) 396-8025

Hitec Central Inc.
803 Choctaw
Independence, MO 64056
(816) 796-6684
Fax: (816) 796-6562

Nevada

Cantec Sales, Inc.
4645 S. Lakeshore Drive
Suite 4
Tempe, AZ 85282-2152
(602) 345-1276
Fax: (602) 345-1197

Straube Associates, Inc.
2551 Casey Avenue
Mountain View, CA 94043
(415) 969-6060
Fax: (415) 964-6526

New Hampshire

Dynasel
22 Green Street
Waltham, MA 02154
(617) 890-6777
Fax: (617) 899-0619

New Jersey (North)

Comtronic Associates
555 Broad Hollow Road
Melville, NY 11747
(516) 249-0505
Fax: (516) 249-0536

New Jersey (South)

Mesa Technical Associates
1 Merrimac Ave.
PO Box 466
Haddonfield, NJ 08033
(609) 429-9531
Fax: (609) 429-1242

New Mexico

Cantec Sales Inc.
5736 Osuna Rd. N.E. #11
Albuquerque, New Mexico
87109-2588
(505) 889-9165
Fax: (505) 889-9198

New York (Long Island)

Comtronic Associates
555 Broad Hollow Road
Melville, NY 11747
(516) 249-0505
Fax: (516) 249-0536

(Upstate)

Gen-Tech Electronics
4855 Executive Drive
Liverpool, NY 13088
(315) 454-3480
Fax: (315) 451-0988
TWX: (710) 545-0288

Gen-Tech Electronics
5 Arbutus Lane
Binghamton, NY 13901
(607) 648-8833
Fax: (315) 451-0988

Gen-Tech Electronics
70 Sandoris Circle
Rochester, NY 14622
(716) 467-5016
Fax: (315) 451-0988

Gen-Tech Electronics
41 Burning Tree Lane
Penfield, NY 14526
(716) 381-5159
Fax: (315) 451-0988

Gen-Tech Electronics
16 Creek Bend Rd.
Poughkeepsie, NY 12603
(914) 462-2939

North Carolina

Godwin Associates
1100 Logger Court
Suite B102
Raleigh, NC 27609
(919) 878-8000
Fax: (919) 878-3923

Godwin Associates
3127 Eastway Dr. Suite 205
Charlotte, NC 28205
(704) 549-8500
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North Dakota

Tecteam Sales Inc.
3050 Metro Dr. Ste 301
Minneapolis, MN 55425
(612) 854-6616
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Ohio

The Lyons Corporation
4812 Frederick Road
Suite 101
Dayton, OH 45414
(513) 278-0714
Fax: (513) 278-3609

The Lyons Corporation
248 North State Street
Westerville, OH 43081
(614) 895-1447
Fax: (513) 278-3609

The Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
(216) 659-9224
Fax: (216) 659-9227

Oklahoma

Logic 1 Sales
2005 Spring Valley Road
Suite A
Richardson, TX 75081
(214) 234-0765
Fax: (214) 669-3042

Oregon

Quadra Sales Corp.
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Fax: (206) 742-9899

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The Lyons Corporation
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South Dakota

Tecteam Sales Inc.
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Minneapolis, MN 55425
(612) 854-6616

Tennessee

Southern Component Sales, Inc.
307 Clinton Ave E, Ste 413
Huntsville, AL 35801
(205) 533-6500
Fax: (205) 533-6578

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Logic 1 Sales
11499 Research Blvd.
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Logic 1 Sales
4606 FM 1960 West
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(713) 444-7594
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Logic 1 Sales
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Fax: (505) 889-9198

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Wisconsin

Tech-Tam Sales Inc.
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Circuit Sales
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Fax: (708) 773-2721

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CANADA

Alberta

Deskin Sales
3504 78th Ave.
Edmonton, AB T6B 2X9
(403) 466-2106
Fax: (403) 468-3019
TWX: (610) 831-1660

Deskin Sales
Suite 502
609 14th Ave. N.W.
Calgary, AB T2N 2A1
(403) 270-4440
Fax: (403) 283-2491

British Columbia

Deskin Sales
8650 Cambie St.
Vancouver, BC V6P 6M6
(604) 324-8343
Fax: (604) 324-6965
TWX: (610) 922-5036

Manitoba

Deskin Sales
P.O. Box 473
Transcona, MAN R2C 2Z9
(0) Zenith 06009
(403) 466-2106
Fax: (204) 224-2084
TWX: (610) 821-7394

Ontario

Deskin Sales
155 Clayton Drive
Markham, ONT L3R 5T9
(416) 475-1412
Telex: 06-966559
Fax: (416) 474-9105
TWX: (610) 492-5113

Deskin Sales
6 Antares Dr., Suite 204
Nepean, ONT K2E 8A9
(613) 228-1201
TWX: (610) 421-3793
Fax: (613) 228-1499

Quebec

Deskin Sales
5655 Thimens Blvd.
Ville St. Laurent, PQ H4R 2K9
(514) 334-2860
Telex: 05-824838
TWX: (610) 421-37 93
Fax: (514) 331-8692

North American Distributors

UNITED STATES

Alabama

Jaco/QC, Inc.
6035 Atlantic Blvd., Suite J
Norcross, GA 30071
(404) 449-9508
Fax: (404) 449-0275

Arizona

Anthem Electronics
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
(602) 966-6600
Fax: (602) 966-4826

Sterling Electronics Inc.
(Billing Address)
P.O. Drawer 20867
Phoenix, AZ 85036
(602) 437-1500
Fax: (602) 437-5588

Sterling Electronics Inc.
(Shipping Address)
3312 East Broadway Rd.
Phoenix, AZ 85040

Time Electronics
1301 West Geneva Drive
Tempe, AZ 85282
(602) 967-2000
Fax: (602) 967-5923

Arkansas

Jaco/QC Inc.
425 Kellway Circle
Addison, TX 75264
(214) 733-4300

Time Electronics
330 Sovereign Court
St. Louis, MO 63011-4491
(314) 391-6444

Time Electronics
1876 Firman
Richardson, TX 75081
(214) 644-4644
Fax: (214) 644-6668

California

Anthem Electronics
9339 Oakdale Ave.
Chatsworth, CA 91311
818-700-1000
Fax: (818) 775-1302

Anthem Electronics
1 Oldfield Drive
Irvine, CA 92718-9208
(714) 768-4444
Fax: (714) 380-4747

Anthem Electronics
1040 E. Brokaw Road
San Jose, CA 95131
(408) 453-1200
Fax: (408) 452-2281

Anthem Electronics
9369 Carroll Park Drive
San Diego, CA 92121
(619) 453-4871
Fax: (619) 546-7893

Anthem Electronics
580 Menlo Drive, Suite 8
Rocklin, CA 95677
(916) 624-9744

Almo Electronics
2107 N. First St., Suite 690
San Jose, CA 95110
(408) 436-8822
Fax: (408) 436-8928
TWX: (910) 328-6161

Almo Electronics
3017 South Daimler St.
Santa Ana, CA 92705-5812
(714) 757-0444
Fax: (714) 757-0410

Almo Electronics
5137 Clareton Drive, Ste. 200
Agoura Hills, CA 91301
(818) 991-3984
Fax: (818) 706-0549

Semi Dice
1096 Bloomfield Drive
Los Alamitos, CA 90720
(213) 594-4631
TWX: (910) 341-7710

Time Electronics
370 South Crenshaw Blvd.,
Suite E-704
Torrance, CA 90503-1727
(213) 320-0880
Fax: (213) 320-6372

Time Electronics
1039 Moffett Park Dr.
Sunnyvale, CA 94086
(408) 734-9888
Fax: (408) 734-1719

Time Electronics
30343 Canwood St.
Suite 210
Agoura Hills, CA 91301
(818) 707-2880
Fax: (818) 707-3657

Counties in California

(Los Angeles & Kern)

Time Electronics
975 Independence Street
Chatsworth, CA 91311
(818) 998-7200
Fax: (818) 998-0143

Jaco Electronics
2260 Townsgate Rd.
Westlake Village, CA 91361
(805) 495-9998
Fax: (805) 494-3864

(San Diego & Imperial)

Time Electronics
8525 Arjons Drive, Suite A
San Diego, CA 92126
(619) 586-1331
Fax: (619) 271-7011

Jaco Electronics
1541 Parkway Loop "D"
Tustin, CA 92680
(714) 258-9003
Fax: (714) 258-1909

(Orange)

Time Electronics
3002 Dow Ave., Suite 102
Tustin, CA 92680
(714) 669-0100
Fax: (714) 544-2526

Jaco Electronics
1541 Parkway Loop "D"
Tustin, CA 92680
(714) 258-9003
Fax: (714) 258-1909

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North American Distributors (cont'd.)

Colorado

Anthem Electronics
373 Inverness Drive, South
Englewood, CO 80112
(303) 790-4500
Fax: (303) 790-4532

Time Electronics
7399 South Tucson Way
Englewood, CO 80112
(303) 799-8851
Fax: (303) 799-0012

Connecticut

Jaco Electronics
384 Pratt Street
Meriden, CT 06450
(203) 235-1422
Fax: (203) 634-4884

Delaware

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East H-1
Bellmawr, NJ 08031
(609) 931-5305
Fax: (609) 931-4928

District of Columbia

Time Electronics
905 Red Branch Road
Columbia, MD 21045
(301) 964-3090
Fax: (301) 964-9274

Jaco Electronics
10270 Old Columbia Rd.
Columbia, MD 21046
(301) 995-6620
Fax: (301) 995-6032

Florida

Jaco Electronics
1060 Holland Dr., Suite 3K
Boca Raton, FL 33487
(407) 241-7943
Fax: (407) 241-7950

Time Electronics
4203 Vineland Rd. K-7
Orlando, FL 32811
(407) 841-6565
Fax: (407) 648-0814

Georgia

Jaco/QC, Inc.
6035 Atlantic Blvd, Suite J
Norcross, GA 30071
(404) 449-9508
Fax: (404) 449-0275

Idaho

Anthem Electronics
19017 120th Ave. N.E.
Suite 102
Bothell, WA 98011
(206) 483-1700
Fax: (206) 486-0571

Time Electronics
860 Willows Road, N.E.
Redmond, WA 98052
(206) 882-1500
Fax: (206) 883-1158

Illinois

Classic Components
3336 Commercial
Northbrook, IL 60062
(708) 272-9650
TWX: (910) 686-4783

Time Electronics
2000 Algonquin Rd.
Schaumburg, IL 60173
(708) 303-3000
Fax: (708) 303-3030

Illinois (South)

Time Electronics
330 Sovereign Court
St. Louis, MO 63011
(314) 391-6444

Indiana

Bell Industries
5230 West 79th St.
Indianapolis, IN 46268
(317) 875-8200

Bell Industries
3606 Enterprise Drive
Fort Wayne, IN 46801
(219) 423-3422

Iowa

Sterling Electronics
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
Twx: (910) 576-3135

Kansas

Time Electronics
330 Sovereign Court
St. Louis, MO 63011
(314) 391-6444

Sterling Electronics
9535 Alden St.
Lenexa, Kansas 66215
(913) 492-5406

Kentucky

Bell Industries
5230 West 79th St.
Indianapolis, IN 46268
(317) 875-8200

Bell Industries
3606 Enterprise Drive
Fort Wayne, IN 46801
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Louisiana

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1005 Industrial Blvd
Sugarland, TX 77478
(713) 240-2255

Time Electronics
1876 Firman
Richardson, TX 75081
(214) 644-4644
Fax: (214) 644-6668

Maine

Jaco Electronics
1053 East St.
Tewksbury, MA 01876
(508) 640-0010
Fax: (508) 640-0755

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

Maryland

Time Electronics
905 Red Branch Road
Columbia, MD 21045
(301) 964-3090
Fax: (301) 964-9274

Jaco Electronics
10270 Old Columbia Road
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Fax: (508) 640-0755

Time Electronics
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Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

Michigan

Time Electronics
945 N. Edgewood Dr. Suite G
Wooddale, IL 60191
(708) 350-0610

Bell Industries
3981 Varsity Drive
Ann Arbor, MI 48106
(313) 971-9093

Minnesota

Sterling Electronics
5000 West 78th Street
Minneapolis, MN 55435
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Wooddale, IL 60191
(708) 350-0610

Mississippi

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(404) 449-9508
Fax: (404) 449-0275

Missouri

Time Electronics
330 Sovereign Court
St. Louis, MO 63011-4491
(314) 391-6444

Montana

Time Electronics
7399 South Tucson Way
Englewood, CO 80112
(303) 799-8851
Fax: (303) 799-0012

Nevada

Anthem Electronics
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
(602) 966-6600
Fax: (602) 966-4826

Sterling Electronics Inc.
3312 East Broadway Road
Phoenix, AZ 85282
(602) 268-2121
Fax: (602) 437-5588

Nevada (North)

Time Electronics
1339 Moffet Park Drive
Sunnyvale, CA 94086
(408) 734-9888
Fax: (408) 734-1719

New Hampshire

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1053 East St.
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(508) 640-0010
Fax: (508) 640-0755

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

New Jersey

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East H-1
Bellmawr, NJ 08031
(609) 931-5305
Fax: (609) 931-4928

Jaco Electronics
140 Green Ralf Ave.
Wayne, NJ 07470
(201) 904-9510
Fax: (201) 904-9521

Time Electronics
70 Marcus Blvd
Hauppauge, NY 11788
(516) 273-0100
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New Mexico

Time Electronics
130 West Geneva Drive
Tempe, AZ 85282
(602) 967-2000
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North American Distributors (cont'd.)

New York

Time Electronics
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Pacific Electronics
200 Newtown Road
Plainview, NY 11803
(516) 293-6630
TWX: (510) 224-6550
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145 Oser Avenue
Hauppauge, NY 11788
(516) 273-5500
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Upstate New York

Time Electronics
7010 Fly Rd.
East Syracuse, NY 13057
(315) 432-0355
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Jaco/QC, Inc.
3029-107 Stonybrook Drive
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Time Electronics
9800-L Southern Pine Blvd.
Charlotte, NC 28210
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Ohio

Bell Industries
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Time Electronics
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(314) 391-6444

Time Electronics
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Richardson, TX 75081
(214) 644-4644
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9090 S.W. Gemini Dr.
Beaverton, OR 97005
(503) 643-1114
Fax: (503) 626-7928

Time Electronics
15688 S.W. 72nd Ave.,
Portland, OR 97224-7743
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Pennsylvania (East)

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Interstate Industrial Park
Kop-Center East H-1
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Pennsylvania (West)

Advarcom Inc.
5620 West Road
McKean, PA 16426
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Advarcom Inc.
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Export, PA 15632
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Fax: (404) 449-0275

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Jaco/QC, Inc.
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(512) 835-0220

Jaco/QC, Inc.
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Sugarland, TX 77478
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Fax: (801) 973-8555

Time Electronics
2446 Progress Drive
West Valley, UT 84119
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ANALOG SWITCHES

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Features

- Microprocessor compatible control inputs
- On chip control memory and address decoding
- Row addressing
- Master reset
- 32 crosspoint switches in 8 × 4 array
- 5.0V to 15.0V operation
- Low crosstalk between switches
- Low on resistance: 90Ω (typ.) at 13V
- Matched switch characteristics
- Switches frequencies up to 40MHz

- Wejścia sterujące zgodne z mikroprocesorem Pamięć sterująca w układzie scalonym i dekodowanie adresów
- Adresowanie wierszowe
- Reset główny 32 przełączniki krzyżowe w układzie 8 x 4 Praca 5.0V do 15.0 V Niski przesłuch między przełącznikami Niska rezystancja w stanie załączenia (typ.) przy 13 V Dopasowane charakterystyki przełączników Szybkość przełączania do 40 MHz

Applications

- PABX and key sytems
- Data acquisition systems
- Test equipment/instrumentation
- Analog/digital multiplexers

Zastosowania

- Centrale PABX i systemy centralnego sterowania
- Systemy akwizycji danych i sprzęt testowy i aparatura pomiarowa
- Multipleksery analogowe/cyfrowe

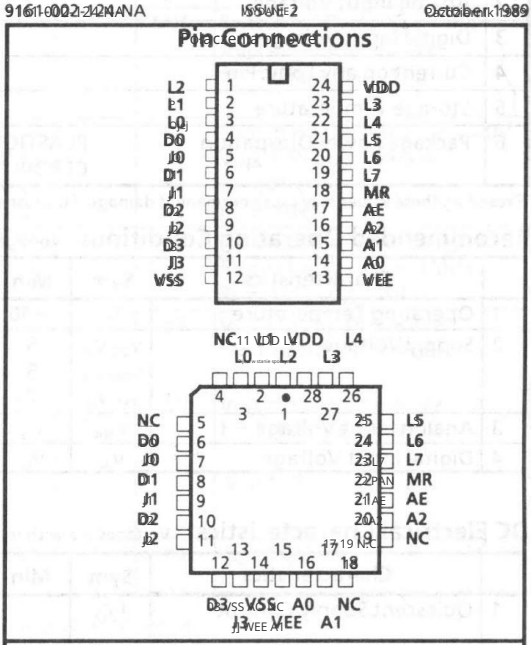
Description

The MT8804A is a CMOS/LSI 8 × 4 Analog Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. This circuit has digitally controlled analog switches having very low "ON" resistance and very low "OFF" leakage current. Switches will operate with analog signals at frequencies to 40 MHz and up to 15.0Vp-p. A "HIGH" on the Master Reset input switches all channels "OFF" and clears the memory. This device is ideal for crosspoint switching applications.

Układ CMOS/LSI 8 × 4 Analogowy Układ Przełączający zawierający pamięć sterującą (32 bity), dekoder i cyfrowe układy logiczne konwertujące poziom sygnałów. Ten układ scalony ma cyfrowo sterowane analogowe przełączniki o bardzo małej rezystancji w stanie załączenia i bardzo małym prądzie upływu w stanie wyłączenia. Przełączniki mogą pracować z sygnałami analogowymi o częstotliwościach do 40 MHz i napięciach do 15,0 Vp-p. Podanie stanu wysokiego na wejście zerowania głównego powoduje wyłączenie wszystkich kanałów i wyzerowanie pamięci. Układ ten jest idealny do zastosowań w przełączaniu krzyżowym.

Pin Connections

Połączenia wyprowadzeń



Ordering Information

Informacje dotyczące zamówień

MT8804AC	24 Pin CERDIP
MT8804AE	24 Pin PLASTIC DIP
MT8804AP	28 Pin PLCC

Zakres temperatur: -40° do 85°C – 40° to 85°C

MT8804AC – 24-stykowy CERDIP

MT8804AE – 24-stykowy PLASTIC DIP

MT8804AP – 28-stykowy PLCC

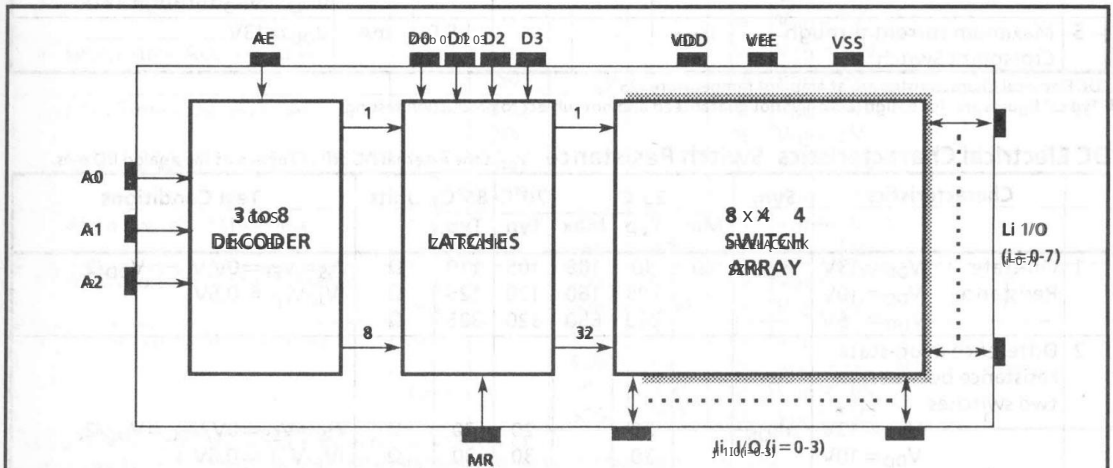


Figure 1 - Functional Block Diagram

Rysunek 1 - Schemat blokowy funkcji

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Absolute Maximum Ratings*

Maksymalne wartości graniczne* – Napięcie zasilania względem V_{SS} chyba że podano inaczej.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage Napięcie zasilania	$V_{DD}-V_{SS}$	-0.3	16	V
		$V_{DD}-V_{EE}$	-0.3	16	V
		$V_{SS}-V_{EE}$	-0.3	16	V
2	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	V_{EE}-0.3	V_{DD}+0.3	V
3	Digital Input Voltage Wejściowe napięcie cyfrowe	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any Logic Pin Prąd na dowolnym pinie logicznym	I		10	mA
5	Storage Temperature Temperatura przechowywania	T_{ST}	-65	+150	°C
6	Package Power Dissipation Pakiet rozpraszania mocy	PLASTIC DIP Plastik DIP P_D		0.6	W
		CERDIP Ceramika P_D		1.2	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Funkcjonalne działanie w tych warunkach nie jest domniemane.

Recommended Operating Conditions

Zalecane warunki pracy – Napięcia względem V_{SS} chyba że podano inaczej.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature Temperatura robocza	T_O	-40	25	85	°C	
2	Supply Voltage Napięcie zasilania	$V_{DD}-V_{SS}$	5	5	15	V	
		$V_{DD}-V_{EE}$	5	10	15	V	
		$V_{SS}-V_{EE}$	0	5	10	V	
3	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage Dwustanowy cyfrowy napięcie wejściowe	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics

Charakterystyka elektryczna DC – Chyba że podano inaczej, napięcia są mierzone względem $V_{EE}=0V$, $V_{SS}=0V$.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Quiescent Supply Current Prąd zasilania spoczynkowego	I_{DD}		1	100	µA	$V_{DD}=15V$. All digital inputs at $V_{IN}=V_{SS}$ or V_{DD} V_{DD}, wszystkie wejścia cyfrowe przy
2	Off-state Leakage Current (Any line to any junctor) Prąd upływu w stanie wyłączonym (dowolna linia do dowolnego łącznika)	I_{OFF}		±0.1	±500	nA	$V_{DD}=13V$, Switch is 'Off' V_{DD}, przełącznik w pozycji „wył.”
3	Input Logic "0" level Poziom logiki wejściowej „0”	V_{IL}			3.0 1.5	V	$V_{DD}=10V$ $V_{DD}=5V$ $V_{INA}=V_{DD}$ through 1kΩ $V_{INA}=V_{DD}$ przez 1kΩ
4	Input Logic "1" level Wejście logiczne „1” poziom	V_{IH}	7.0 3.5			V	$V_{DD}=10V$ $V_{DD}=5V$ $V_{INA}=V_{DD}$ through 1kΩ $V_{INA}=V_{DD}$ przez 1kΩ
5	Maximum current through Crosspoint Switch Maksymalny prąd przepływający przełącznik crosspoint	I_{MAX}			±8.0	mA	$V_{DD}=13V$

†DC Electrical Characteristics are at ambient temperature (25°C).
†Dane Elektryczne Charakterystyki są w temperaturze otoczenia (25°C).
†Typical figures are for design aid only, not guaranteed and not subject to production testing.
†Podane wartości typ. są przeznaczone wyłącznie pomocniczo w projektowaniu, nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics: Switch Resistance

Charakterystyka elektryczna DC – Rezystancja przełącznika. V_{DC} to zewnętrznie przesunięcie DC przyłożone do pinów analogowych I/O.

	Characteristics	Sym	25°C			70°C	85°C	Units	Test Conditions
			Min	Typ	Max	Typ	Typ		
1	On-state Resistance Rezystancja VDD = 10	$V_{DD}=13V$ R_{ON} $V_{DD}=10V$ $V_{DD}=5V$	60	90 105 290	108 160 650	105 120 320	110 125 325	Ω Ω Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Ji}-V_{Lj}\rvert = 0.6V$
2	Difference in on-state resistance between two switches Różnica w stanie włączonym rezystancja między dwoma przełącznikami	$V_{DD}=13V$ ΔR_{ON} $V_{DD}=10V$		20 30		20 30	20 30	Ω Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Ji}-V_{Lj}\rvert = 0.6V$

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AC Electrical Characteristics† - Crosspoint Performance

V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to $V_{DD} = 10V$, $V_{SS} = V_{EE} = 0V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch Line Capacitance	C_{WP}		5		pF	
2	Switch Junctor Capacitance	C_{OS}		20		pF	
3	Feedthrough Capacitance	C_I		0.2		pF	
4	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{INA}) = -3dB$	F_{3dB}		40		MHz	Switch is "ON"; $V_{DC} = 5V$, $V_{INA} = 5Vpp$ sine wave $f = 1kHz$; $R_L = 1k\Omega$
5	Total Harmonic Distortion	THD					Switch is "ON"; $V_{EE} = V_{SS} = 0V$
	$V_{DD} = 15V/V_{DC} = 7.5V$			0.1		%	$V_{INA} = 5Vpp$ sine wave
	$V_{DD} = 10V/V_{DC} = 5V$			0.2		%	$f = 1kHz$;
	$V_{DD} = 5V/V_{DC} = 2.5V$			1.0		%	$R_L = 10k\Omega$
6	Feedthrough Channel "OFF" Feed $= 20LOG(V_{OUT}/V_{INA})$	FDT		-50		dB	All Switches "OFF"; $V_{INA} = 5Vpp$ sine wave $f = 1MHz$; $R_L = 1k\Omega$. $V_{DC} = 5V$
7	Crosstalk between any two channels for switches $Li - Ji$ and $Lj - Jj$.	X_{talk}		-40		dB	$V_{INA} = 2Vpp$ sine wave $f = 1.0MHz$; $R_L = 600\Omega$.
	$Li - Ji$ is "ON" $Lj - Jj$ is "OFF" $Xtalk = 20LOG(V_{Jj}/V_{Li})$.			-90		dB	$V_{INA} = 2Vpp$ sine wave $f = 3.4kHz$; $R_L = 600\Omega$. $V_{DC} = 5V$
8	Propagation delay through switch	t_{PS}		10		ns	$C_L = 50pF$

† AC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Control and I/O Timings

Voltages are with respect to $V_{SS} = V_{EE} = 0V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Digital Input Capacitance	C_{DI}		5		pF	$V_{DD} = 10V$
2	Setup Time D0-D3 to AE	t_{DS}	150			ns	$V_{DD} = 10V$
			200			ns	$V_{DD} = 5V$
3	Hold Time D0-D3 to AE	t_{DH}	120			ns	$V_{DD} = 10V$
			300			ns	$V_{DD} = 5V$
4	Setup Time Address to AE	t_{AS}	0			ns	$V_{DD} = 10V$
			50			ns	$V_{DD} = 5V$
5	Hold Time Address to AE	t_{AH}	120			ns	$V_{DD} = 10V$
			300			ns	$V_{DD} = 5V$
6	AE Pulse Width	t_{AEW}	100			ns	$V_{DD} = 10V$
			250			ns	$V_{DD} = 5V$
7	AE to Switch Status Delay	t_{PAE}		200	300	ns	$V_{DD} = 10V$ ①
				650	900	ns	$V_{DD} = 5V$ ①
8	DATA to Switch Status Delay	t_{PLH}		250	400	ns	$V_{DD} = 10V$ ①
		t_{PHL}		650	1000	ns	$V_{DD} = 5V$ ①
9	MR to Switch Status Delay	t_{MR}		250	400	ns	$V_{DD} = 10V$ ②
				500	600	ns	$V_{DD} = 5V$ ②
		t_{MRR}		200	350	ns	$V_{DD} = 10V$ ②
				500	750	ns	$V_{DD} = 5V$ ②

† AC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.
① $R_L = 10k\Omega$, $C_L = 50pF$
② $R_L = 1k\Omega$, $C_L = 50pF$
Digital Input rise time (tr) and fall time (tf) = 5ns.

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MEMORY RESET MR	ADDRESS ENABLE AE	ADDRESS A2	ADDRESS A1	ADDRESS A0	ADDRESSED LINE	INPUT DATA TO CONTROL MEMORY D3	D2	D1	D0	JUNCTORS CONNECTED TO ADDRESSED LINE J3	J2	J1	J0
1	X	X	X	X	ALL	X	X	X	X	All Switches "OFF"			
0	0	X	X	X	NONE	X	X	X	X	No Change of State			
0	1	0	0	0	L0	0	0	0	0	●	●	●	●
0	1	0	0	0	L0	0	0	0	1	●	●	●	+
0	1	0	0	0	L0	0	0	1	0	●	●	+	●
0	1	0	0	0	L0	0	0	1	1	●	●	+	+
0	1	0	0	0	L0	0	1	0	0	●	+	●	●
0	1	0	0	0	L0	0	1	0	1	●	+	●	+
0	1	0	0	0	L0	0	1	1	0	●	+	+	●
0	1	0	0	0	L0	0	1	1	1	●	+	+	+
0	1	0	0	0	L0	1	0	0	0	+	●	●	●
0	1	0	0	0	L0	1	0	0	1	+	●	●	+
0	1	0	0	0	L0	1	0	1	0	+	●	+	●
0	1	0	0	0	L0	1	0	1	1	+	●	+	+
0	1	0	0	0	L0	1	1	0	0	+	+	●	●
0	1	0	0	0	L0	1	1	0	1	+	+	●	+
0	1	0	0	0	L0	1	1	1	0	+	+	+	●
0	1	0	0	0	L0	1	1	1	1	+	+	+	+
0	1	0	0	1	L1	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	0	1	L1	1	1	1	1	+	+	+	+
0	1	0	1	0	L2	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	1	0	L2	1	1	1	1	+	+	+	+
0	1	0	1	1	L3	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	1	1	L3	1	1	1	1	+	+	+	+
0	1	1	0	0	L4	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	0	0	L4	1	1	1	1	+	+	+	+
0	1	1	0	1	L5	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	0	1	L5	1	1	1	1	+	+	+	+
0	1	1	1	0	L6	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	0	L6	1	1	1	1	+	+	+	+
0	1	1	1	1	L7	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	1	L7	1	1	1	1	+	+	+	+

Table 1 Address Decode Truth Table

NOTES:
0 - Low Logic Level
1 - High Logic Level
X - Don't Care Condition
+ - Indicates Connection Between Junctor and Addressed Line
● - Indicates No Connection Between Junctor and Addressed Line

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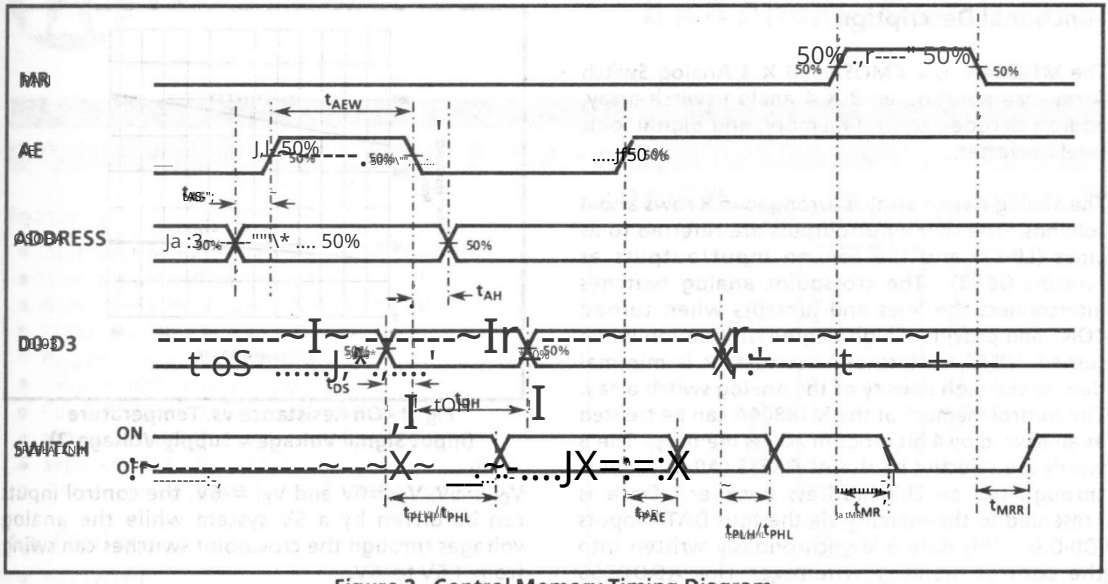

Figure 2 - Control Memory Timing Diagram

Rysunek 2 – Diagram czasowy pamięci sterującej

Pin Description

Opis pinów

Pin #*	Name	Description
1-3	L2-L0	**L2-L0 Analog Lines (Inputs/Outputs):** these are connected to the L2-L0 columns of the switch array.
4	D0	**D0 Data (Input):** Active High.
5	J0	**J0 Analog Junctor (Input/Output):** is connected to the J0 row of the switch array.
6	D1	**D1 Data (Input):** Active High.
7	J1	**J1 Analog Junctor (Input/Output):** is connected to the J1 row of the switch array.
8	D2	**D2 Data (Input):** Active High.
9	J2	**J2 Analog Junctor (Input/Output):** is connected to the J2 row of the switch array.
10	D3	**D3 Data (Input):** Active High.
11	J3	**J3 Analog Junctor (Input/Output):** is connected to the J3 row of the switch array.
12	V_{SS}	**Digital Ground Reference.**
13	V_{EE}	**Negative Power Supply.**
14-16	A0-A2	**A0-A2 Address Lines (Inputs).**
17	AE	**Address Enable/Strobe (Input):** enables function selected by address and data. Address must be stable before AE goes high and D0-D3 must be stable on the falling edge of the AE. Active High.
18	MR	**Master RESET (Input):** this is used to turn off all switches. Active High.
19-23	L7-L3	**L7-L3 Analog Lines (Inputs/Outputs):** these are connected to the L7-L3 columns of the switch array.
24	V_{DD}	**Positive Power Supply.**

* Pins 1 and 12 are reversed for CERDIP only

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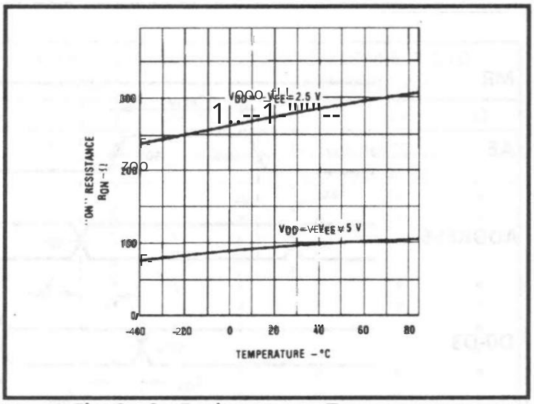
Opis funkcjonalny

MT8804A to przełącznik analogowy CMOS/ISI 8 X 4 Macierz zawierająca tablicę przełączników analogowych 8 X 4, dekoder adresów, pamięć sterującą i logikę cyfrową konwerter poziomów.

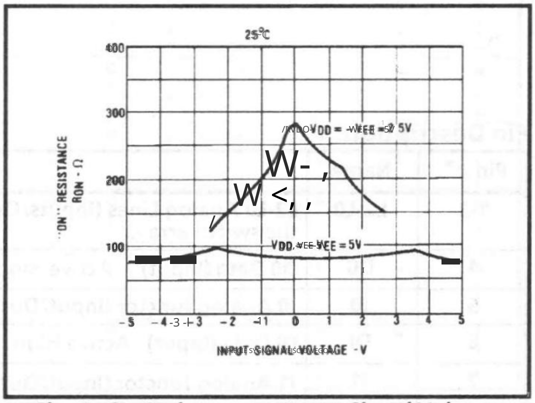
Tablica przełączników analogowych jest ułożona w 8 rzędach i 4 kolumny. Wiersz wejścia/wyjścia są określane jako linie (LO-L7), kolumny wejścia/wyjścia jako Junctors (JO-J3). Analogowe przełączniki crosspoint połączyć linie i skrzyżowania po przekręceniu „ON" i zapewnia wysoki stopień izolacji, gdy wyłączony . Przesłuch międzykanałowy jest minimalny pomimo dużej gęstości układu przełączników analogowych . Pamięć sterującą MT8804A może być traktowana as an 8 słów przez 4 bity random access memory. 8 słowa są wybierane przez wejścia ADRES (A0-A2) poprzez dekoder adresów na chipie. Dane są prezentowane w pamięci poprzez cztery wejścia DATA (D0-D3). Dane te są asynchronicznie zapisywane do pamięć sterująca zawsze, gdy ADRES Wejście ENABLE (AE) jest WYSOKIE. Napisano wysoki poziom w komórkę pamięci zamienia odpowiadającą przełącznik krzyżowy „ON" podczas niskiego poziomu powoduje punkt przełączania na "WYŁ".

Tylko przełączniki krzyżowe odpowiadające adresowane słowa pamięci są narażone na wpływ danych zapisane w pamięci. Pozostałe przełączniki zachowują swoje poprzednie stany. By ustanawiające odpowiednie wzorce w pamięci sterującej, dowolne połączenie linii i skrzyżowań może być połączony. Poziom wysoki na MASTER RESET (MR) wejście przywraca wszystkie lokalizacje pamięci do stanu niskiego poziom i wyłącza wszystkie przełączniki krzyżowe skutecznie izolując linie od skrzyżowań. Konwertery poziomu logicznego cyfrowego umożliwiają cyfrowe wejście poziomy różnią się od limitów poziomów analogowych przełączane przez tablicę . Na przykład, z



Ryg. 3 - Rezystancja w zależności od temperatury (Napięcie sygnału wejściowego = Napięcie zasilania/2)

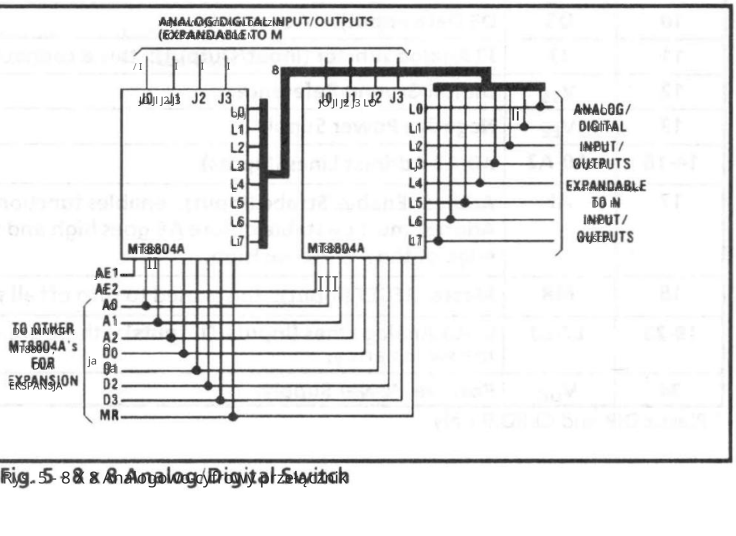
V_{DD} = 5V, V_{SS} = 0V, i V_{EE} = -6V, wejścia sterujące może być napędzany przez system 5 V, podczas gdy analogowy napięcia przechodzące przez przełączniki krzyżowe mogą się wahać od +5V do -6V.



Ryg. 4 - Rezystancja w stosunku do napięcia sygnału wejściowego

8 x 8 Przełącznik analogowo-cyfrowy

Dwa MT8804A skonfigurowane, jak pokazano, wdrożyć 8 x 8 analogowo/cyfrowy przełącznik. Pojemność przełącznika może być rozszerzono do tablicy M x N wejścia/wyjścia. Rozszerzenie w M wymiar jest taki, jak pokazano z Linie MT8804A (L0-L7) połączone w jedną całość. Rozszerzenie w wymiarze N to osiągnięte poprzez powielenie obwodu pokazano i podłączono MT8804A skrzyżowania (J0-J3) wspólne. adres, włączanie i dane wejściowe MT8804A można podłączyć w wspólne dla każdego rozmiaru przełącznika pod warunkiem, że adres włączający (AE) wejścia są sterowane indywidualnie. A konkretna ścieżka sygnału jest połączona przez ustawienie odpowiednich sygnałów na adres i linie danych i pobieranie odpowiedniej wejście włączające wysokie. Reset główny (MR), gdy jest wysokie, rozłącza każdy sygnał ścieżki.



Ryg. 5 - 8 X 8 Analogowo/cyfrowy przełącznik

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MITEL

ISO-CMOS MT8806
8 x 4 tablica przełączników analogowych

9161-002-097-NA Wydanie 2 Listopad 1988

Cechy

- Wewnętrzne zatrzaski sterujące i dekoder adresowy
- Krótki czas przygotowania i utrzymania
- Szeroki zakres napięcia roboczego: 4,5 V do 13,2 V
- Możliwość obsługi sygnału analogowego 12 Vpp
- R_{ON} 65Ω maks. @V_{DD}=12V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @V_{DD}=12V, 25°C
- Przełącznik Full CMOS zapewniający niskie zniekształcenia
- Minimalne przebicie i przesłuchy
- Oddzielne zasilanie analogowe i cyfrowe
- Niski pobór mocy w technologii ISO-CMOS

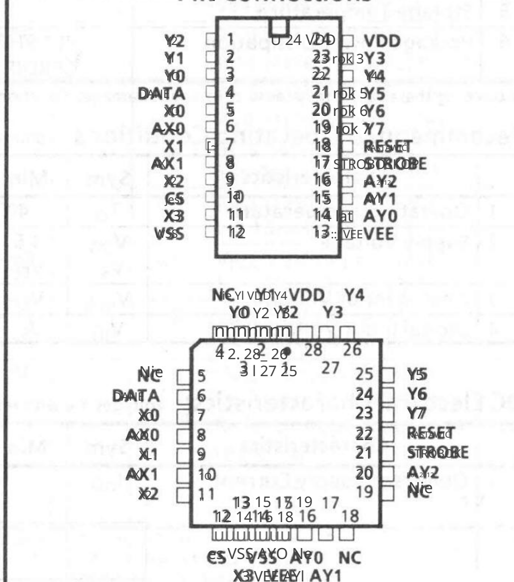
Aplikacje

- Systemy kluczowe
- Systemy PBX
- Radio mobilne
- Sprzęt testowy/instrumentacja
- Multipleksery analogowo-cyfrowe
- Przełączanie audio/wideo

Opis

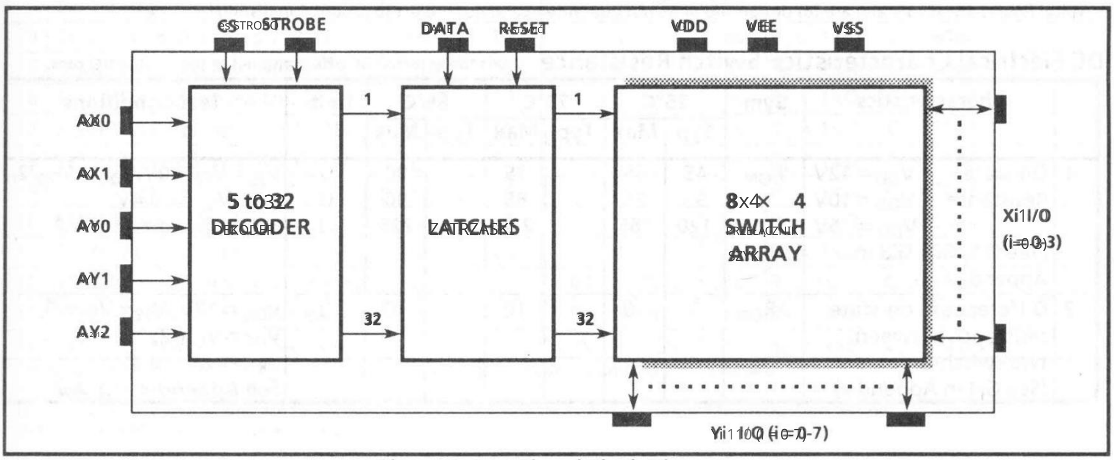
Mitel MT8806 to technologia fabrykated w ISO-CMOS firmy MITEL zapewniająca niskie rozpraszanie mocy i wysoką niezawodność. Urządzenie zawiera tablicę 8x4 przełączników krzyżowe wraz z linią 5 do 32 obwody dekodera i zatrzasku. Każdy z 32 przełączników można adresować poprzez wybranie odpowiednie bity adresu tywnego. Wybrany przełącznik można włączyć lub wyłączyć, stosując logiczną lub zero do wejścia DATA. Vss to odniesienie do uziemienia wejść cyfrowych. Zasięg analogowy sygnał pochodzi z Voo do VEE. Chip Select (CS) pozwala rozwinięcie szyk być kaskadowo połączona macierzą punktu przecięcia.

Połączenia pinów



Informacje o zamówieniu -40° do 85°C

MT8806AC	24-pinowy CERDIP
MT8806AE	24-pinowy plastikowy DIP
MT8806AP	28-stykowy PLCC



Rysunek 1 - Schemat blokowy funkcji

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Absolute Maximum Ratings*

Parametry maksymalne bezwzględne* Voltages are with respect to V_{SS} unless otherwise stated. Napięcia odniesione do V_{SS}, jeżeli nie podano inaczej.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage Napięcie zasilania	V_{DD} V_{SS}	-0.3 -0.3	15.0 V_{DD} + 0.3	V V
2	Analog Input Voltage Wejściowe napięcie analogowe	V_{INA}	-0.3	V_{DD} + 0.3	V
3	Digital Input Voltage Wejściowe napięcie cyfrowe	V_{IN}	V_{SS} - 0.3	V_{DD} + 0.3	V
4	Current on any I/O Pin Prąd na dowolnym pinie I/O	I		±15	mA
5	Storage Temperature Temperatura przechowywania	T_S	-65	+150	°C
6	Package Power Dissipation Maksymalna moc rozpraszana w układzie	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Funkcjonalne działanie w tych warunkach NIE JEST gwarantowane. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Zalecane warunki pracy Voltages are with respect to V_{SS} unless otherwise stated. Napięcia odniesione do V_{SS}, jeżeli nie podano inaczej.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature Temperatura pracy	T_O	-40	25	85	°C	
2	Supply Voltage Napięcie zasilania	V_{DD} V_{SS} - V_{EE}	4.5		13.2 V_{DD} - 4.5	V V	
3	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage Wejściowe napięcie cyfrowe	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics*

Charakterystyka elektryczna prądu stałego* Voltages are with respect to V_{EE} = V_{SS} = 0V, V_{DD} = 12V unless otherwise stated. Napięcia odniesione do V_{EE} = V_{SS} = 0V, V_{DD} = 12V, jeżeli nie podano inaczej.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current Prąd zasilania spoczynkowego	I_{DD}		1	100	µA	All digital inputs at V_{SS} or V_{DD} Wejścia cyfrowe ustawione na V_{SS} lub V_{DD}
				0.4	1	mA	All digital inputs at V_{IN} = 2.4 + V_{SS}, V_{SS} = 7.0V Wejścia cyfrowe ustawione na V_{IN} = 2.4 + V_{SS}, V_{SS} = 7.0V
				5	15	mA	All digital inputs at V_{IN} = 3.4V Wejścia cyfrowe ustawione na V_{IN} = 3.4V
2	Off-state Leakage Current Prąd upływu stanu wyłączonego (See G.9 in Appendix) (patrz G.9 w załączniku)	I_{OFF}		±1	±500	nA	V_{IN} = V_{DD} - V_{EE} V_{IN} = V_{DD} - V_{EE} See Appendix, Fig. A.1 Zobacz Załącznik, rys. A.1
3	Input Logic "0" Level Logiczny poziom wejściowy "0"	V_{IL}			0.8 + V_{SS}	V	V_{SS} = 7.5V; V_{EE} = 0V V_{SS} = 7,5 V; V_{EE} = 0V
4	Input Logic "1" Level Logiczny poziom wejściowy "1"	V_{IH}	2.0 + V_{SS}		V_{SS} = 6.5V; V_{EE} = 0V V_{SS} = 6,5 V; V_{EE} = 0V		
5	Input Logic "1" Level Logiczny poziom wejściowy "1"	V_{IH}	3.3			V	
6	Input Leakage (digital pins) Upływ sygnału wejściowego (piny cyfrowe)	I_{LEAK}		0.1	10	µA	All digital inputs at V_{IN} = V_{SS} or V_{DD} Wszystkie wejścia cyfrowe przy V_{IN} = V_{SS} lub V_{DD}

*Dla Electrical Characteristics are over recommended temperature range. Charakterystyka elektryczna zawarta w zalecanym zakresie temperatur.

†Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing. Typowe wartości podane dla 25°C służą tylko pomocą projektową, nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics - Switch Resistance

Charakterystyka elektryczna prądu stałego - rezystancja przełącznika* Voltages are with respect to V_{EE} = V_{SS} = 0V unless otherwise stated. Napięcia odniesione do V_{EE} = V_{SS} = 0V, jeżeli nie podano inaczej.

	Characteristics		Sym	25°C		70°C		85°C		Units	Test Conditions
				Typ	Max	Typ	Max	Typ	Max		
1	Switch On-state Resistance Rezystancja przełącznika w stanie włączonym (See G.1, G.2, G.3 in Appendix) (patrz G.1, G.2, G.3 w załączniku)	V_{DD} = 12V, V_{SS} = 0V	R_{ON}	45	65		75		80	Ω	V_{SS} = 0V, V_{EE} = 0V, V_{DC} = V_{DD}/2, V_{IN} = 0.4V V_{SS} = 0V, V_{EE} = 0V, V_{DC} = V_{DD}/2, V_{IN} = 0,4V See Appendix, Fig. A.2 Zobacz Załącznik, rys. A.2
		V_{DD} = 10V, V_{SS} = 0V		55	75		85		90	Ω	
		V_{DD} = 5V, V_{SS} = 0V		120	185		215		225	Ω	
2	Difference in on-state resistance between two switches Różnica w stanie włączonym rezystancja między dwoma przełącznikami (See G.4 in Appendix) (patrz G.4 w załączniku)	V_{DD} = 12V, V_{SS} = 0V	ΔR_{ON}	5	10		10		10	Ω	V_{SS} = 0V, V_{EE} = 0V, V_{DC} = V_{DD}/2, V_{IN} = 0.4V V_{SS} = 0V, V_{EE} = 0V, V_{DC} = V_{DD}/2, V_{IN} = 0,4V See Appendix, Fig. A.2 Zobacz Załącznik, rys. A.2

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AC Elektryczny Charakterystyka† - Wydajność punktu przecięcia - Napięcia względem $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, chyba że podano inaczej.

	Charakterystyka	Sym	Min	Typ‡	Maksymalna liczba jednostek	Jednostki	Warunki testowe
1	Przełącznik o pojemności	C_S		20		pF	f = 1 MHz
2	Przepust Pojemność	C_F		0,2		pF	f = 1 MHz
3	Odpowiedź częstotliwościowa Kanał „WŁ.” 20LOG(V_{OUT}/V_{Xi}) = -3dB	F_{3dB}		45		MHz	Przełącznik jest w pozycji „ON”; V_{INA} = 2Vpp fala sinusoidalna; R_L = 1kΩ Zobacz załącznik, rys. A.3
4	Total Harmonic Distortion (Zobacz G.5, G.6 w Załączniku)	THD		0,01		%	Przełącznik jest „WŁ.”; V_{INA} = 2Vpp sinusoidalna f = 1kHz; R_L = 1kΩ
5	Kanał przepustowy „WYŁ” Podawanie = 20LOG (V_{OUT}/V_{Xi}) (Zobacz G.8 w załączniku)	FDT		-95		dB	All Switches „WYŁ”; V_{INA} = 2Vpp fala sinusoidalna f = 1kHz; R_L = 1kΩ. Zobacz załącznik, rys. A.4
6	Przesłuch między dowolnymi dwoma kanałami dla przełączników Xi-Yi i Xj-Yj. Xtalk = 20LOG (V_{Yj}/V_{Xi}). (Zobacz G.7 w załączniku).	X_{talk}		-45		dB	V_{INA} = fala sinusoidalna 2Vpp f = 10MHz, R_L = 75Ω.
				-90		dB	V_{INA} = fala sinusoidalna 2Vpp f = 10kHz, R_L = 600Ω.
				-85		dB	V_{INA} = fala sinusoidalna 2Vpp f = 10kHz, R_L = 1kΩ.
				-80		dB	V_{INA} = fala sinusoidalna 2Vpp f = 1kHz, R_L = 10kΩ. Zobacz dodatek, rys. A.5 dla test circuit.
7	Przełącznik opóźnienia przez propagacji	t_{PS}			30	ns	R_L = 1kΩ; C_L = 50pF

† Timing jest powyżej zalecanego zakresu temperatur. Zobacz rys. 2 dla kontroli I/O timing details.
‡ Podane wartości typowe przy 25°C mają charakter wyłącznie pomocniczy przy projektowaniu. Nie są gwarantowane i nie podlegają testom produkcyjnym.
Przesłuch w zestawie dotyczy wyłącznie obudów Plastic DIPS, wartość przesłuchu dla obudów PLCC są o około 5 dB lepsze.

AC Elektryczny Charakterystyka† - Kontrola I/O Timings. Napięcia względem $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, chyba że podano inaczej.

	Charakterystyka	Sym	Min	Typ‡	Maksymalna liczba jednostek	Jednostki	Warunki testowe
1	Przełącznik przesłuchu wejściowy sterujący (dla CS, DATA, STROBE, Adres)	CX_{talk}		30		mVpp	V_{IN} = fala prostokątna 3V; R_{IN} = 1kΩ, R_L = 10kΩ. Zobacz załącznik, rys. A.6
2	Wejście cyfrowe Pojemność	C_{DI}		10		pF	f = 1MHz
3	Częstotliwość przełączania	F_O			20	MHz	
4	Konfiguracja czasu DATA do STROBE	t_{DS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
5	Czas trzymania DATA do STROBE	t_{DH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
6	Ustaw adres czasu na STROBE	t_{AS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
7	Czas podtrzymania adresu STROBE	t_{AH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
8	Czas konfiguracji CS do STROBE	t_{CSS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
9	Czas podtrzymania CS do STROBE	t_{CSH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
10	Szerokość impulsu STROBE	t_{SPW}	20			ns	R_L = 1kΩ, C_L = 50pF ①
11	RESET Szerokość impulsu	t_{RPW}	40			ns	R_L = 1kΩ, C_L = 50pF ①
12	STROBE do opóźnienia stanu przełącznika	t_S		40	100	ns	R_L = 1kΩ, C_L = 50 pF ①
13	DATA do opóźnienia stanu przełącznika	t_D		50	100	ns	R_L = 1kΩ, C_L = 50 pF ①
14	RESET do opóźnienia stanu przełącznika	t_R		35	100	ns	R_L = 1kΩ, C_L = 50 pF ①

† Timing jest powyżej zalecanego zakresu temperatur. Zobacz rys. 2, aby uzyskać szczegóły dotyczące sterowania I/O timing.
Czas narastania (tr) i czas spadku (tf) sygnału wejściowego cyfrowego = 5ns.
‡ Typowe wartości wynoszą 25°C i służą jedynie celom projektowym. Nie są gwarantowane i nie podlegają testom produkcyjnym.
① Zobacz Załącznik, rys. A.7 dla obwodu testowego.

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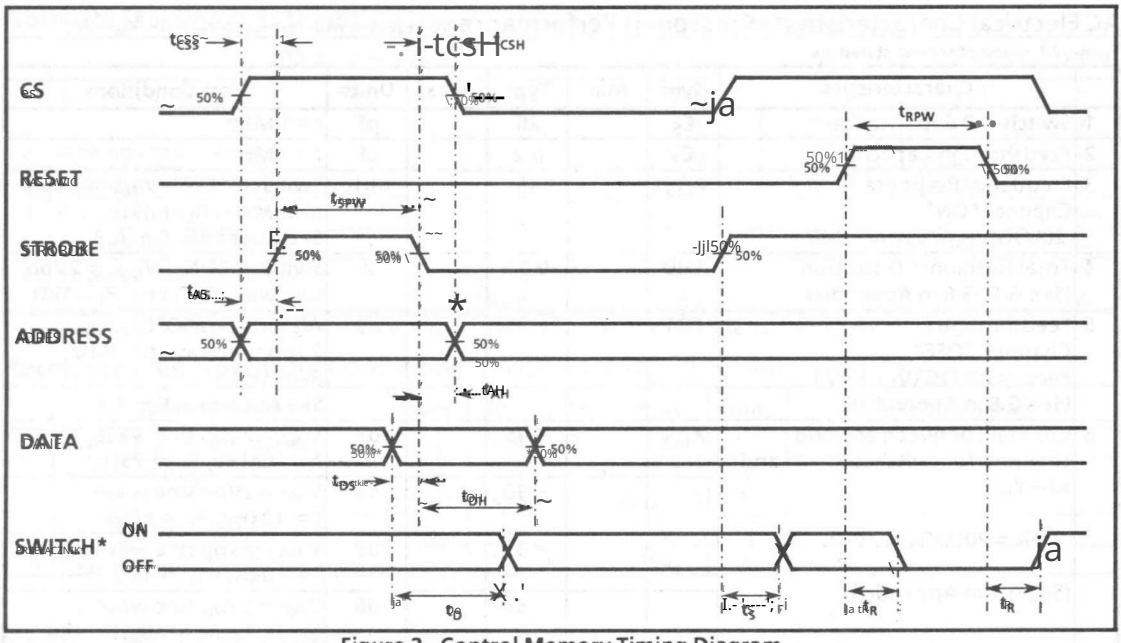

Figure 2 - Control Memory Timing Diagram

Rysunek 2 - Kontrola pamięci czasowej - Diagram

*See Appendix A, Fig. A-7 for switching waveform

AX0	AX1	AY0	AY1	AY2	Connection
0	0	0	0	0	X0-Y0
0	0	1	0	0	X0-Y1
0	0	0	1	0	X0-Y2
0	0	1	1	0	X0-Y3
0	0	0	0	1	X0-Y4
0	0	1	0	1	X0-Y5
0	0	0	1	1	X0-Y6
0	0	1	1	1	X0-Y7
1	0	0	0	0	X1-Y0
↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	X1-Y7
0	1	0	0	0	X2-Y0
↓	↓	↓	↓	↓	↓ ↓
0	1	1	1	1	X2-Y7
1	1	0	0	0	X3-Y0
↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	X3-Y7

Table 1 - Address Decode Truth Table

Tabela 1 - Tabela dekodowania adresu

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Pin Description

Pin #*	Name	Description
1-3	Y2-Y0	**Y2-Y0 Analog (Inputs/Outputs):** these are connected to the Y2-Y0 columns of the switch array.
4	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	X0	**X0 Analog (Input/Output):** this is connected to the X0 row of the switch array.
6	AX0	**X0 Address Line (Input).**
7	X1	**X1 Analog (Input/Output):** this is connected to the X1 row of the switch array.
8	AX1	**X1 Address Line (Input).**
9	X2	**X2 Analog (Input/Output):** this is connected to the X2 row of the switch array.
10	CS	**Chip Select (Input):** this is used to select the device. Active High.
11	X3	**X3 Analog (Input/Output):** this is connected to the X3 row of the switch array.
12	V_{SS}	**Digital Ground Reference.**
13	V_{EE}	**Negative Power Supply.**
14-16	AY0-AY2	**Y0-Y2 Address Lines (Inputs).**
17	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable during falling edge of STROBE. Active High.
18	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of CS. Active High.
19-23	Y7-Y3	**Y7-Y3 Analog (Inputs/Outputs):** these are connected to the Y7-Y3 columns of the switch array.
24	V_{DD}	**Positive Power Supply.**

* Plastic DIP and CERDIP only

Functional Description

The MT8806 is an analog switch matrix with an array size of 8 x 4. The switch array is arranged such that there are 8 columns by 4 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of 32 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0 & AX1). Data is presented to the DATA input and is asynchronously written into memory whenever both the CS (Chip Select) and the STROBE inputs are high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of the state of CS. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8806 to enable switching of negative analog signals. The range for digital signals is from V_{SS} to V_{DD} while the range for analog signals is from V_{EE} to V_{DD}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The five address inputs along with the STROBE and CS (Chip Select) inputs are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low, causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

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NOTES:

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9161-002-008-NA ISSUE 2 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage 4.5V to 13.2V
- 12Vpp analog signal capability
- Ron = 650Ω max. @ VDD - VEE = 12V, 25°C
- ΔRON = 100Ω @ VDD - VEE = 12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

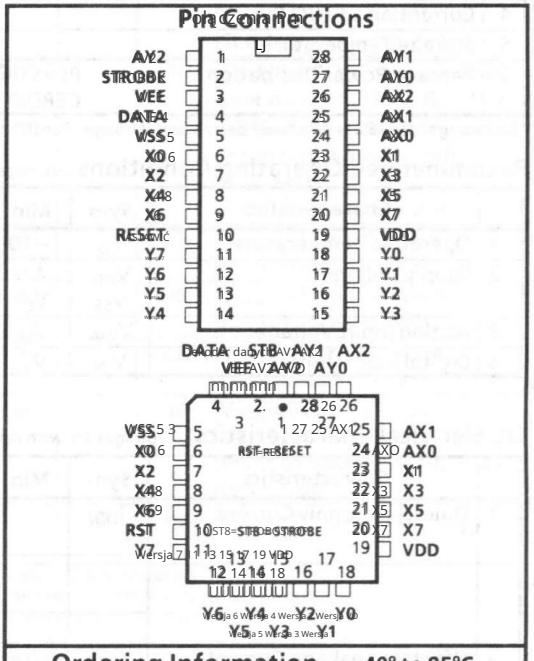
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The MT8808 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 8 array of cross-point CMOS switches along with a 6 to 64 line decoder and latch circuitry. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input during the strobe. A logical reference of the digital inputs. The range of the analog signal is from V_{EE} to V_{DD}.

Pin Connections



Ordering Information

MT8808AC	28 Pin CERDIP	−40° to 85°C
MT8808AE	28 Pin PLASTIC DIP	
MT8808AP	28 Pin PLCC	

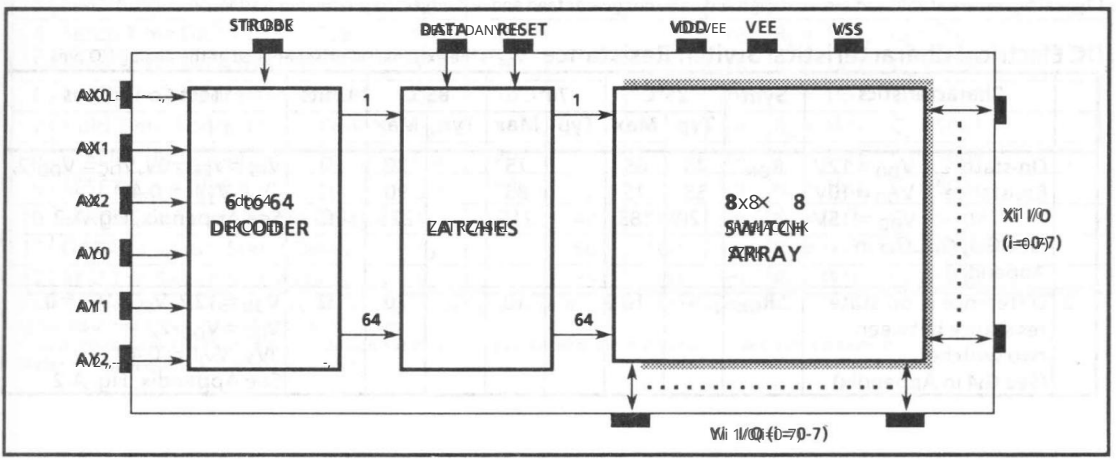


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD}	-0.3	15.0	V
			V_{SS}	-0.3	V_{DD}+0.3	V
2	Analog Input Voltage		V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P_D		0.6	W
		CERDIP	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	-40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
		V_{SS}	V_{EE}		V_{DD}-4.5	V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to V_{EE} = V_{SS} = 0V, V_{DD} = 12V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	µA	All digital inputs at V_{IN} = V_{SS} or V_{DD}
				0.4	1.5	mA	All digital inputs at V_{IN} = 2.4 + V_{SS}; V_{SS} = 7.0V
				5	15	mA	All digital inputs at V_{IN} = 3.4V
2	Off-state Leakage Current (See G9 in Appendix)	I_{OFF}		±1	±500	nA	$\|V_{Xi} - V_{Yj}\|$ = V_{DD} - V_{EE} See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			0.8+V_{SS}	V	V_{SS} = 7.5V; V_{EE} = 0V
4	Input Logic "1" level	V_{IH}	2.0+V_{SS}			V	V_{SS} = 6.5V; V_{EE} = 0V
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	µA	All digital inputs at V_{IN} = V_{SS} or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics		Sym	25°C		70°C		85°C		Units	Test Conditions
				Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance (See G1, G2, G3 in Appendix)	V_{DD} = 12V	R_{ON}	45	65		75		80	Ω	V_{SS} = V_{EE} = 0V, V_{DC} = V_{DD}/2,
		V_{DD} = 10V		55	75		85		90	Ω	$\|V_{Xi} - V_{Yj}\|$ = 0.4V
		V_{DD} = 5V		120	185		215		225	Ω	See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G4 in Appendix)		ΔR_{ON}	5	10		10		10	Ω	V_{DD} = 12V, V_{SS} = V_{EE} = 0, V_{DC} = V_{DD}/2, $\|V_{Xi} - V_{Yj}\|$ = 0.4V See Appendix, Fig. A.2

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AC Electrical Characteristics† - Crosspoint Performance

Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi}) = -3dB$	F_{3dB}		45		MHz	Switch is "ON"; $V_{INA} = 2Vpp$ sine wave; $R_L = 1k\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA} = 2Vpp$ sine wave f = 1kHz; $R_L = 1k\Omega$
5	Feedthrough Channel "OFF" $Feed = 20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; $V_{INA} = 2Vpp$ sine wave f = 1kHz; $R_L = 1k\Omega$. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi – Yi and Xj – Yj. $Xtalk = 20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		-45		dB	$V_{INA} = 2Vpp$ sine wave f = 10MHz; $R_L = 75\Omega$.
				-90		dB	$V_{INA} = 2Vpp$ sine wave f = 10kHz; $R_L = 600\Omega$.
				-85		dB	$V_{INA} = 2Vpp$ sine wave f = 10kHz; $R_L = 1k\Omega$.
				-80		dB	$V_{INA} = 2Vpp$ sine wave f = 1kHz; $R_L = 10k\Omega$. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	$R_L = 1k\Omega$; $C_L = 50pF$

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC package are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		30		mVpp	$V_{IN} = 3V$ squarewave; $R_{IN} = 1k\Omega$, $R_L = 10k\Omega$. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
8	STROBE Pulse Width	t_{SPW}	20			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
9	RESET Pulse Width	t_{RPW}	40			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
10	STROBE to Switch Status Delay	t_S		40	100	ns	$R_L = 1k\Omega$, $C_L = 50 pF$ ①
11	DATA to Switch Status Delay	t_D		50	100	ns	$R_L = 1k\Omega$, $C_L = 50 pF$ ①
12	RESET to Switch Status Delay	t_R		35	100	ns	$R_L = 1k\Omega$, $C_L = 50 pF$ ①

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5 ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

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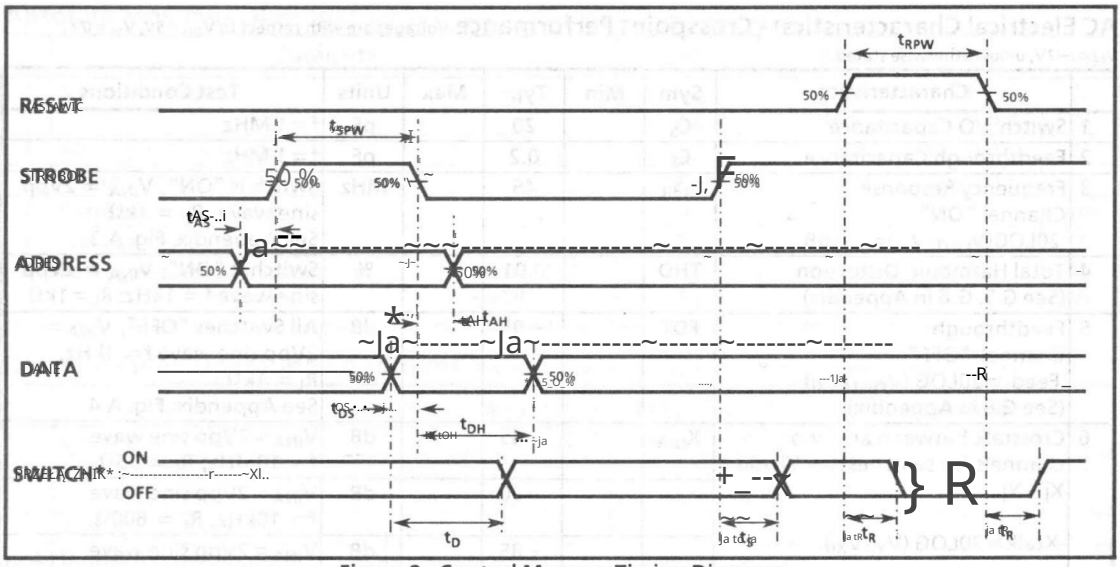

Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A-7 for switching waveform

AX2	AX1	AX0	Connection	AX2	AX1	AX0	Connection
0	0	0	X0-Y0	1	0	0	X0-Y4
0	0	1	X1-Y0	1	0	1	X1-Y4
0	1	0	X2-Y0	1	1	0	X2-Y4
0	1	1	X3-Y0	1	1	1	X3-Y4
1	0	0	X4-Y0	1	0	0	X4-Y4
1	0	1	X5-Y0	1	0	1	X5-Y4
1	1	0	X6-Y0	1	1	0	X6-Y4
1	1	1	X7-Y0	1	1	1	X7-Y4
0	0	0	X0-Y1	1	0	0	X0-Y5
0	0	1	X1-Y1	1	0	1	X1-Y5
0	1	0	X2-Y1	1	1	0	X2-Y5
0	1	1	X3-Y1	1	1	1	X3-Y5
1	0	0	X4-Y1	1	0	0	X4-Y5
1	0	1	X5-Y1	1	0	1	X5-Y5
1	1	0	X6-Y1	1	1	0	X6-Y5
1	1	1	X7-Y1	1	1	1	X7-Y5
0	0	0	X0-Y2	1	0	0	X0-Y6
0	0	1	X1-Y2	1	0	1	X1-Y6
0	1	0	X2-Y2	1	1	0	X2-Y6
0	1	1	X3-Y2	1	1	1	X3-Y6
1	0	0	X4-Y2	1	0	0	X4-Y6
1	0	1	X5-Y2	1	0	1	X5-Y6
1	1	0	X6-Y2	1	1	0	X6-Y6
1	1	1	X7-Y2	1	1	1	X7-Y6
0	0	0	X0-Y3	1	0	0	X0-Y7
0	0	1	X1-Y3	1	0	1	X1-Y7
0	1	0	X2-Y3	1	1	0	X2-Y7
0	1	1	X3-Y3	1	1	1	X3-Y7
1	0	0	X4-Y3	1	0	0	X4-Y7
1	0	1	X5-Y3	1	0	1	X5-Y7
1	1	0	X6-Y3	1	1	0	X6-Y7
1	1	1	X7-Y3	1	1	1	X7-Y7

Table 1 - Address Decode Truth Table

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Pin Description

Pin #	Name	Description
1	AY2	**AY2 Address Line (Input).**
2	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
3	VEE	**Negative Power Supply.**
4	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	VSS	**Digital Ground Reference .**
6-9	X0, X2, X4, X6	**X0, X2, X4 and X6 Analog (Inputs/Outputs):** these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	RESET	**Master RESET (Input):** this is used to turn off all switches. Active High.
11-18	Y7, Y0	**Y7, Y0 Analog (Inputs/Outputs):** these are connected to the Y0 - Y7 columns of the switch array.
19	VDD	**Positive Power Supply.**
20-23	X7, X5, X3, X1	**X7, X5, X3 and X1 Analog (Inputs/Outputs):** these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	**AX0-AX2 Address Lines (Inputs).**
27,28	AY0, AY1	**AY0 and AY1 Address Lines (Inputs).**

Functional Description

The MT8808 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AX0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint switch off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET line will asynchronously return all memory locations to a logical "0" turning off all crosspoint switches. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8808 to enable switching of negative analog signals. The range for digital signals is from V_{SS} to V_{DD}, while the range for analog signals is from V_{EE} to V_{DD}. V_{SS} and V_{EE} pins can be tied together if single voltage reference is needed.

Address Decode

The six address inputs along with the STROBE are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off according to the DATA input. DATA must be stable at the falling edge of STROBE in order for correct data to be written to the latch.

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NOTES:

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9161-002-099-NA ISSUE 2 November 1988

Features

- Internal control latches and address decoder
- Short setup and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ $V_{CC} - V_{EE}$ = 12V, 25°C
- ΔR_{ON} 5Ω @ $V_{CC} - V_{EE}$ = 12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology
- Internal pull up resistor for $\overline{RESET}$ pin

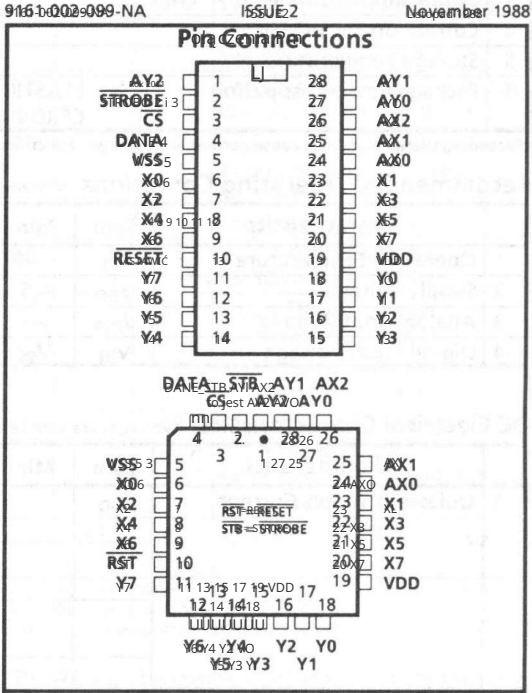
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8809 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. Chip Select ($\overline{CS}$) allows the crosspoint array to be cascaded for matrix expansion.

Pin Connections



Ordering Information

MT8809AC	28 Pin CERDIP	-40° to 85°C
MT8809AE	28 Pin PLASTIC DIP	
MT8809AP	28 Pin PLCC	

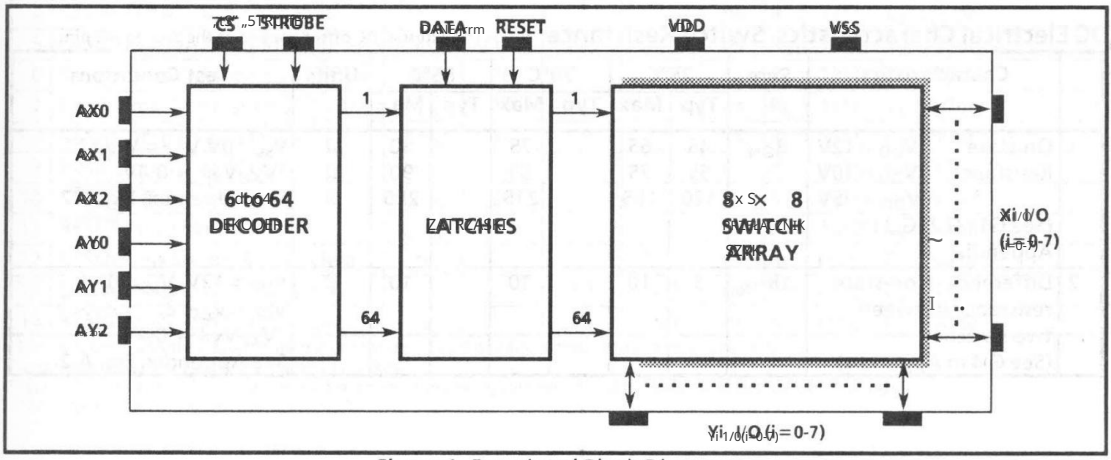


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne wartości graniczne* - Napięcia podawane są względem V_{SS}, chyba że podano inaczej. - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Napięcie zasilania - Supply Voltage	V_{DD}	-0.3	15.0	V
		V_{SS}	-0.3	V_{DD} + 0.3	V
2	Analogowe napięcie wejściowe - Analog Input Voltage	V_{INA}	-0.3	V_{DD} + 0.3	V
3	Cyfrowe napięcie wejściowe - Digital Input Voltage	V_{IN}	V_{SS} - 0.3	V_{DD} + 0.3	V
4	Prąd udarowy w dowolnym pinie - Current on any I/O Pin	I		±15	mA
5	Temperatura przechowywania - Storage Temperature	T_S	-65	+150	°C
6	Maksymalna rozpraszana moc - Package Power Dissipation PLASTIC DIP	P_D		0.6	W
	CERDIP	P_D		1.0	W

*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Normalne działanie w tych warunkach nie jest gwarantowane. - Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Zalecane warunki pracy - Napięcia podawane są względem V_{SS}, chyba że podano inaczej. - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Temperatura pracy - Operating Temperature	T_O	-40	25	85	°C	
2	Napięcie zasilania - Supply Voltage	V_{DD}	4.5		13.2	V	
3	Analogowe napięcie wejściowe - Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Cyfrowe napięcie wejściowe - Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics†

Charakterystyki dynamiczne - Napięcia podawane są względem V_{SS}, chyba że podano inaczej. - Voltages are with respect to V_{SS} = 0V, V_{DD} = +12V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Prąd zasilania spoczynkowego - Quiescent Supply Current	I_{DD}		1	100	µA	Wszystkie wejścia cyfrowe przy V_{IN} = V_{SS} lub V_{DD} wyjście aktywne RESET = V_{DD} - All digital inputs at V_{IN} = V_{SS} or V_{DD} except RESET = V_{DD}.
				120	400	µA	Wszystkie wejścia cyfrowe przy V_{IN} = V_{SS} lub V_{DD} wyjście aktywne RESET = V_{SS} - All digital inputs at V_{IN} = V_{SS} or V_{DD} except RESET = V_{SS}.
				0.5	1.6	mA	1,6mA wejścia cyfrowe przy V_{IN} = 2,4V, V_{DD} = 5,0V - All digital inputs at V_{IN} = 2.4V, V_{DD} = 5.0V
				5	15	mA	15 mA Wejścia cyfrowe przy V_{IN} = 3,4V - All digital inputs at V_{IN} = 3.4V
2	Częstość wyciekania przy wyłączonym zasilaniu (patrz rys. 9 w załączniku) - Off-state Leakage Current (See Fig. 9 in Appendix)	I_{OFF}		±1	±500	nA	V_{IN} = V_{DD} - V_{SS} - V_{IN} = V_{DD} - V_{SS} See Appendix, Fig. A.1
3	Wejście logiczne „0” - Input Logic “0” level	V_{IL}			0.8	V	
4	Wejście logiczne „1” - Input Logic “1” level	V_{IH}	3.0			V	
5	Upływność wejścia (tylko piny cyfrowe) - Input Leakage (digital pins)	I_{LEAK}		0.1	10	µA	Wszystkie wejścia cyfrowe przy V_{IN} = V_{SS} lub V_{DD} RESET = V_{DD} - All digital inputs at V_{IN} = V_{SS} or V_{DD} RESET = V_{DD}

†Charakterystyki elektryczne są ponad zalecanym zakresem temperatur roboczych. - Electrical characteristics are over recommended temperature range.
‡Typowe liczby są przy 25°C i są tylko do celów projektowych. - Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

DC Electrical Characteristics-Switch Resistance

Charakterystyki dynamiczne - Napięcia podawane są względem V_{SS}, chyba że podano inaczej. - Voltages are with respect to V_{SS} = 0V, V_{DD} = +12V unless otherwise stated. Rezystancja przełączania DC mierzona między dowolnymi dwoma analogowymi pinami I/O. - DC switch resistance measured between any two analog I/O pins.

	Characteristics	Sym	25°C		70°C		85°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	Włączony stan rezystancji - On-state Resistance V_{DD} = 12V (patrz rys. 6, 7, 8, 9 w załączniku) - See Fig. 6, 7, 8, 9 in Appendix) V_{DD} = 10V (patrz rys. 5, 6, 7, 8 w załączniku) - See Fig. 5, 6, 7, 8 in Appendix) V_{DD} = 5V (patrz rys. 4, 5, 6, 7 w załączniku) - See Fig. 4, 5, 6, 7 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω	V_{SS} = 0V, V_{DD} = V_{DC} = V_{DD}/2, V_{XI}-V_{YI} = 0.4V See Appendix, Fig. A.2
2	Różnica rezystancji w stanie włączonym między dwoma przełącznikami (patrz rys. 4 w załączniku) - Difference in on-state resistance between two switches (See Fig. 4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	V_{DD} = 12V, V_{SS} = 0, V_{DC} = V_{DD}/2, V_{XI}-V_{YI} = 0.4V See Appendix, Fig. A.2

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AC Electrical Characteristics† - Crosspoint Performance

V_{DC} is the external DC offset at the analog I/O pins. Voltages are with respect to V_{DD}=5V, V_{SS}=0V, V_{EE}=-7V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi}) = -3dB$	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sinewave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f=1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed = $20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA} = 2Vpp sine wave f=1kHz; R_L=1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk = $20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		-45		dB	V_{INA}=2Vpp sine wave f=10MHz; R_L = 75Ω.
				-90		dB	V_{INA}=2Vpp sine wave f=10kHz; R_L = 600Ω.
				-85		dB	V_{INA}=2Vpp sine wave f=10kHz; R_L = 1kΩ.
				-80		dB	V_{INA}=2Vpp sine wave f=1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD}=5V, V_{SS}=0V, V_{EE}=-7V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN}=3V+V_{DC} squarewave; R_{IN}=1kΩ, R_L=1kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L=1kΩ, C_L=50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L=1kΩ, C_L=50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L=1kΩ, C_L=50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L=1kΩ, C_L=50pF ①
8	Setup Time CS to STROBE	t_{CSS}	10			ns	R_L=1kΩ, C_L=50pF ①
9	Hold Time CS to STROBE	t_{CSH}	10			ns	R_L=1kΩ, C_L=50pF ①
10	STROBE Pulse Width	t_{SPW}	20			ns	R_L=1kΩ, C_L=50pF ①
11	RESET Pulse Width	t_{RPW}	40			ns	R_L=1kΩ, C_L=50pF ①
12	STROBE to Switch Status Delay	t_S		40	100	ns	R_L=1kΩ, C_L=50 pF ①
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L=1kΩ, C_L=50 pF ①
14	RESET to Switch Status Delay	t_R		35	100	ns	R_L=1kΩ, C_L=50 pF ①

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

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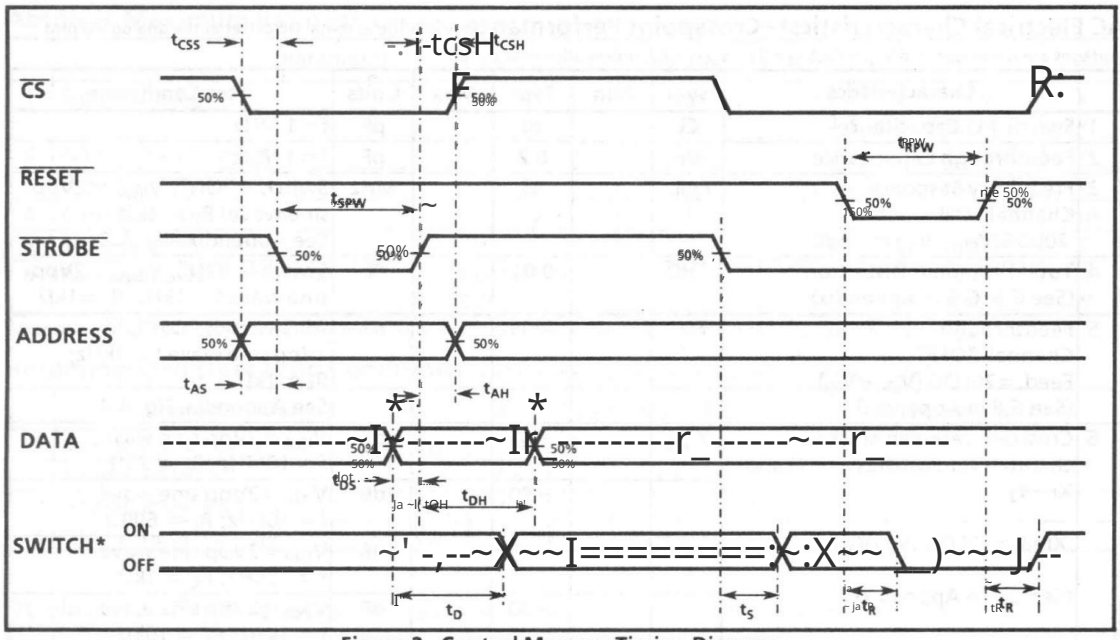

Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A-7 for switching waveform

AX2	AX1	AX0	Connection	AX2	AX1	AX0	Connection
0	0	0	X0 Y0	1	0	0	X0 Y4
0	0	1	X1 Y0	1	0	1	X1 Y4
0	1	0	X2 Y0	1	1	0	X2 Y4
0	1	1	X3 Y0	1	1	1	X3 Y4
0	0	0	X4 Y0	1	0	0	X4 Y4
0	0	1	X5 Y0	1	0	1	X5 Y4
0	1	0	X6 Y0	1	1	0	X6 Y4
0	1	1	X7 Y0	1	1	1	X7 Y4
0	0	0	X0 Y1	1	0	0	X0 Y5
0	0	1	X1 Y1	1	0	1	X1 Y5
0	1	0	X2 Y1	1	1	0	X2 Y5
0	1	1	X3 Y1	1	1	1	X3 Y5
0	0	0	X4 Y1	1	0	0	X4 Y5
0	0	1	X5 Y1	1	0	1	X5 Y5
0	1	0	X6 Y1	1	1	0	X6 Y5
0	1	1	X7 Y1	1	1	1	X7 Y5
0	0	0	X0 Y2	1	0	0	X0 Y6
0	0	1	X1 Y2	1	0	1	X1 Y6
0	1	0	X2 Y2	1	1	0	X2 Y6
0	1	1	X3 Y2	1	1	1	X3 Y6
0	0	0	X4 Y2	1	0	0	X4 Y6
0	0	1	X5 Y2	1	0	1	X5 Y6
0	1	0	X6 Y2	1	1	0	X6 Y6
0	1	1	X7 Y2	1	1	1	X7 Y6
0	0	0	X0 Y3	1	0	0	X0 Y7
0	0	1	X1 Y3	1	0	1	X1 Y7
0	1	0	X2 Y3	1	1	0	X2 Y7
0	1	1	X3 Y3	1	1	1	X3 Y7
0	0	0	X4 Y3	1	0	0	X4 Y7
0	0	1	X5 Y3	1	0	1	X5 Y7
0	1	0	X6 Y3	1	1	0	X6 Y7
0	1	1	X7 Y3	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table

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Pin Description

Pin #	Name	Description
1	AY2	**AY2 Address Line (Input).**
2	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes low and DATA must be stable on the rising edge of STROBE. Active Low.
3	CS	**Chip Select (Input):** this is used to select the device. Active Low.
4	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	VSS	**Ground Reference.**
6-9	X0, X2, X4, X6	**X0, X2, X4 and X6 Analog Inputs/Outputs:** these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of DATA, CS or STROBE. It can be used in conjunction with a power-on reset pulse (connected to RESET pin) to perform power-on reset of the device. Active Low.
11-18	Y7 - Y0	**Y7 - Y0 Analog Inputs/Outputs:** these are connected to the Y0 - Y7 columns of the switch array.
19	VDD	**Positive Power Supply.**
20-23	X7, X5, X3, X1	**X7, X5, X3 and X1 Analog Inputs/Outputs:** these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0, AX1, AX2	**AX0, AX1, AX2 Address Lines (Inputs).**
27,28	AY0, AY1	**AY0 and AY1 Address Lines (Inputs).**

Functional Description

The MT8809 is a analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns and 8 rows. The columns are referred to as the X inputs/outputs and the rows are the Y inputs/outputs. The crosspoint analog switch array will interconnect any X with any Y I/O when turned on by the proper control inputs. The control memory consists of a 64 bit addressable RAM in which each bit is selected by the address inputs (AX0, AX1, AX2, AY0, AY1, AY2). Data is presented to the memory on the DATA input and is asynchronously written into the memory whenever both the CS (Chip Select) and STROBE inputs are low and are latched on the rising edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "0" on the RESET input will asynchronously cause all memory locations to a logical "0", turning off all crosspoint switches regardless of whether CS is high or low.

Address Decode

The six address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the data latches. The DATA input is buffered and presented to all latches. To write to a location, RESET must be high and CS must go low while the address and data are set up. Then the STROBE input is set low and then high causing the data to be latched. The data can be changed while STROBE is low, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the rising edge of STROBE in order for correct data to be written to the latch.

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NOTES:

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MITEL

ISO-CMOS MT8812

8 x 12 tablica przełączników analogowych

9161-002-059-NA ISSUE 1 Listopad 1988

Cechy

- Wewnętrzne zatrzaski sterujące i dekoder adresów
- Krótki czas przygotowania i utrzymania
- Szeroki zakres napięć dla roboczego: 4.5V do 14.5V
- Możliwość obsługi sygnału analogowego 14 Vpp
- RON 65Ω maks. @VDD= 14V, 25°C
- ΔRON ≤ 10Ω @VDD= 14V, 25°C
- Przełącznik Fully CMOS zapewniający niskie zniekształcenia
- Minimalne przebicie i przesłuchy
- Niskie zużycie energii dzięki technologii ISO-CMOS

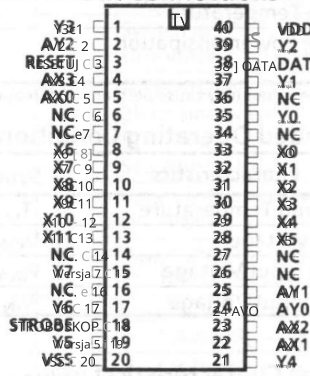
Aplikacje

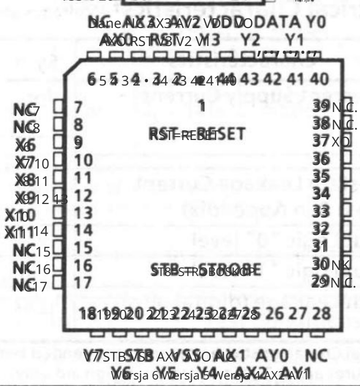
- Systemy PBX
- Radio mobilne
- Sprzęt testowy /instrumentacja
- Multipleksery analogowo-cyfrowe
- Przełączanie Audio/Video

Opis

The MT8812 jest wytwarzany w normie ISO-CMOS firmy MITEL technologia zapewniająca niskie rozpraszanie mocy i wysoka niezawodność. Urządzenie zawiera tablicę 8X12 of przełączniki krzyżowe wraz z linią 7 do 96 obwody dekodera i zatrzasku. Każdy z 96 przełączniki można adresować poprzez wybranie odpowiednie siedem bitów wejściowych. Wybrany przełącznik można włączyć lub wyłączyć, stosując logiczną 1 lub zero do wejścia DATA.

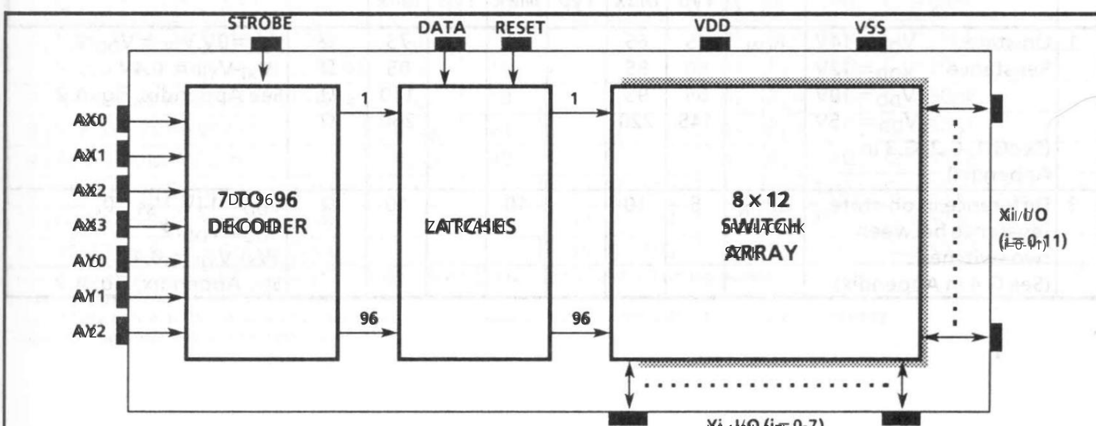
Połączenia Pin





Informacje o zamówieniu 0° do 70°C

MT8812AC 40-stykowy CERDIP
MT8812AE 40-stykowy PLASTIC DIP
MT8812AP 44-stykowy PLCC



Rysunek 1 - Schemat blokowy funkcji

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Absolute Maximum Ratings*

Absolute Maximum Ratings - Napięcie odniesione do V_{SS} chyba że podano inaczej. Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage Napięcie zasilania	V_{DD}	-0.3	16.0	V
		V_{SS}	-0.3	V_{DD} + 0.3	V
2	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	-0.3	V_{DD} + 0.3	V
3	Digital Input Voltage Wejściowe napięcie cyfrowe	V_{IN}	V_{SS} - 0.3	V_{DD} + 0.3	V
4	Current on any I/O Pin Prąd na dowolnym pinie I/O	I		±15	mA
5	Storage Temperature Temperatura przechowywania	T_S	-65	+150	°C
6	Package Power Dissipation Pakiet rozpraszanej mocy	PLASTIC DIP P_D		0.6	W
		CERDIP P_D		1.0	W

* Przekroczenie tych wartości może spowodować uszkodzenie. Funkcjonowanie w tych warunkach nie jest domyślnie zamierzone. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Zalecane warunki pracy - Napięcia podane są w odniesieniu do V_{SS}, chyba że podano inaczej. Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature Temperatura robocza	T_O	0	25	70	°C	
2	Supply Voltage Napięcie zasilania	V_{DD}	4.5		14.5	V	
3	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage Cyfrowe napięcie wejściowe	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics*

Charakterystyki elektryczne prądu stałego* - Napięcia są względem V_{SS} = 0V i V_{DD} = 14V, chyba że podano inaczej. Voltages are with respect to V_{SS} = 0V and V_{DD} = 14V unless otherwise stated.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Quiescent Supply Current Prąd zasilania spoczynkowego	I_{DD}		1	100	µA	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} Wszystkie wejścia cyfrowe przy $V_{IN} = V_{SS}$ lub V_{DD}
				7	15	mA	All digital inputs at $V_{IN} = 2.4V$ Wszystkie wejścia cyfrowe przy $V_{IN} = 2.4$
2	Off-state Leakage Current Prąd upływu w stanie wyłączonym (See G.9 in Appendix) (Zobacz G.9 w załączniku)	I_{OFF}		±1	±500	nA	$V_{Xi} = V_{DD} - V_{SS}$ See Appendix, Fig. A.1 Zobacz załącznik, rys. A.1
3	Input Logic "0" level Wejściowy poziom "0"	V_{IL}			0.8	V	
4	Input Logic "1" level Wejściowy poziom "1"	V_{IH}	2.4			V	
5	Input Leakage (digital pins) Upływ wejściowy (piny cyfrowe)	I_{INLEAK}		0.1	10	µA	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} Wszystkie wejścia cyfrowe przy $V_{IN} = V_{SS}$ lub V_{DD}

* DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
Charakterystyki elektryczne prądu stałego* - Charakterystyki elektryczne prądu stałego są w zalecanym zakresie temperatur roboczych i zalecanych napięciach zasilania.
† Typical figures are at 25°C and are for design aid only - not guaranteed and not subject to production testing.
† Typowe wartości są w temperaturze 25°C i służą jedynie jako pomoc projektowa - nie są gwarantowane i nie podlegają testowaniu produkcyjnemu.

DC Electrical Characteristics - Switch Resistance

Charakterystyki elektryczne prądu stałego - Rezystancja przełącznika - Przy V_{DC}, chyba że podano inaczej. Zewnętrzne napięcie DC offset zastosowane do pinów analogowych I/O. Characteristics are at V_{DD} = 14V, V_{SS} = 0V unless otherwise stated. V_{DC} is the external DC offset applied to the analog I/O pins.

	Characteristics	Sym	25°C		60°C		70°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance Rezystancja w stanie przewodzenia V_{DD} = 14V V_{DD} = 12V V_{DD} = 10V V_{DD} = 5V (See G.1, G.2, G.3 in Appendix) (Zobacz G.1, G.2, G.3 w załączniku)	R_{ON}	45 60 85 145	65 85 95 220				75 95 110 260	Ω Ω Ω Ω	V_{SS} = 0V, V_{DC} = V_{DD}/2, V_{Xi} - V_{Yj} = 0.4V See Appendix, Fig. A.2 Zobacz załącznik, rys. A.2
2	Difference in on-state resistance between two switches Różnica rezystancji w stanie przewodzenia między dwoma przełącznikami (See G.4 in Appendix) (Zobacz G.4 w załączniku)	ΔR_{ON}	5	10		10		10	Ω	V_{DD} = 14V, V_{SS} = 0, V_{DC} = V_{DD}/2, $\lvert V_{Xi} - V_{Yj} \rvert$ = 0.4V See Appendix, Fig. A.2 Zobacz załącznik, rys. A.2

AC Charakterystyka elektryczna† - Wydajność punktu przecięcia. V_{DC} to zewnętrzny offset DC stosowany w analogowym I/O piny. Napięcia są podane względem $V_{DD} = 7V$, $V_{DC} = 0V$, $V_{SS} = -7V$, chyba że podano inaczej.

	Charakterystyka	Sym	Min	Typ‡	Maks	Jednostki	Warunki testowe
1	Przełącznik I/O Pojemność	C_S		20		pF	f = 1 MHz
2	Przepust Pojemność	C_F		0.2		pF	f = 1 MHz
3	Odpowiedź częstotliwościowa Kanał „WŁ." $20LOG(V_{Yi}/V_{Xi}) = -3dB$	F_{3dB}		45		MHz	Przełącznik jest w pozycji „ON"; $V_{INA} = 2Vpp$ fala sinusoidalna; $R_L = 1k\Omega$ Zobacz załącznik, rys. A.3
4	Całkowite zniekształcenie harmoniczne (patrz G.5, G.6 w załączniku)	THD		0.01		%	Przełącznik jest „WŁ."; $V_{INA} = 2Vpp$ sinusoida f = 1kHz; $R_L = 1k\Omega$
5	Przepust Kanał „WYŁ" Podawanie = $20LOG(V_{OUT}/V_{Xi})$ (Zobacz G.8 w załączniku)	FDT		-95		dB	Wszystkie przełączniki „WYŁ"; V_{INA} = Fala sinusoidalna 2Vpp f = 1kHz; $R_L = 1k\Omega$. Zobacz załącznik, rys. A.4
6	Przesłuch między dowolnymi dwoma kanałami dla przełączników Xi - Yi i Xj - Yj. $Xtalk = 20LOG(V_{Yj}/V_{Xi})$. (Zobacz G.7 w załączniku).	X_{talk}		-45		dB	V_{INA} = fala sinusoidalna 2Vpp f = 10MHz; $R_L = 75\Omega$.
				-90		dB	V_{INA} = fala sinusoidalna 2Vpp f = 10kHz; $R_L = 600\Omega$.
				-85		dB	V_{INA} = fala sinusoidalna 2Vpp f = 10kHz; $R_L = 1k\Omega$.
				-80		dB	V_{INA} = 2Vpp fala sinusoidalna f = 1kHz; $R_L = 10k\Omega$. Zobacz załącznik, rys. A.5, aby uzyskać więcej informacji. obwód testowy.
7	Przełącznik opóźnienie przez propagacji	t_{PS}			30	ns	$R_L = 1k\Omega$; $C_L = 50pF$

† Timing jest powyżej zalecanego zakresu temperatur. Zobacz rys. 2, aby uzyskać szczegóły dotyczące kontroli i I/O timingu.
‡ Podane wartości typowe odnoszą się do temperatury 25°C i służą wyłącznie celom projektowym. Nie są gwarantowane i nie podlegają testom produkcyjnym.
Pomiary przesłuchów dotyczą wyłącznie obudów DIPS z tworzywa sztucznego. Wartości przesłuchów dla obudów PLCC są około 5 dB lepsze.

AC Charakterystyka elektryczna† - Sterowanie i I/O Timings. V_{DC} to zewnętrzny offset DC stosowany w analogowym I/O piny. Napięcia są podane względem $V_{DD} = 7V$, $V_{DC} = 0V$, $V_{SS} = -7V$, chyba że podano inaczej.

	Charakterystyka	Sym	Min	Typ‡	Maks	Jednostki	Warunki testowe
1	Przesłuch wejściowy sterujący do przełącznika (dla DANYCH, STROBU, Adres)	CX_{talk}		30		mVpp	$V_{IN} = 3V + V_{DC}$ fala prostokątna; $R_{IN} = 1k\Omega$, $R_L = 10k\Omega$. Zobacz załącznik, rys. A.6
2	Wejście cyfrowe Pojemność	C_{DI}		10		pF	f = 1MHz
3	Częstotliwość przełączania	F_O			20	MHz	
4	Konfiguracja czasu DATA do STROBE	t_{DS}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
5	Czas trzymania DANE do STROBU	t_{DH}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
6	Ustaw adres czasu na STROBE	t_{AS}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
7	Czas podtrzymania adresu STROBE	t_{AH}	10			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
8	Szerokość impulsu STROBE	t_{SPW}	20			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
9	RESET Szerokość impulsu	t_{RPW}	40			ns	$R_L = 1k\Omega$, $C_L = 50pF$ ①
10	STROBE do opóźnienia stanu przełączania	t_S		40	100	ns	$R_L = 1k\Omega$, $C_L = 50 pF$ ①
11	DANE do opóźnienia stanu przełącznika	t_D		50	100	ns	$R_L = 1k\Omega$, $C_L = 50 pF$ ①
12	RESET do opóźnienia stanu przełącznika	t_R		35	100	ns	$R_L = 1k\Omega$, $C_L = 50 pF$ ①

† Timing jest powyżej zalecanego zakresu temperatur. Zobacz rys. 2 dla kontroli i I/O timingu.
Czas narastania (tr) i czas spadku (tf) sygnału wejściowego cyfrowego = 5ns.
‡ Typowe wartości podano w temperaturze 25°C i służą wyłącznie celom projektowym. Nie są gwarantowane i nie podlegają testom produkcyjnym.
① Zobacz Załącznik, rys. A.7 dla obwodu testowego.

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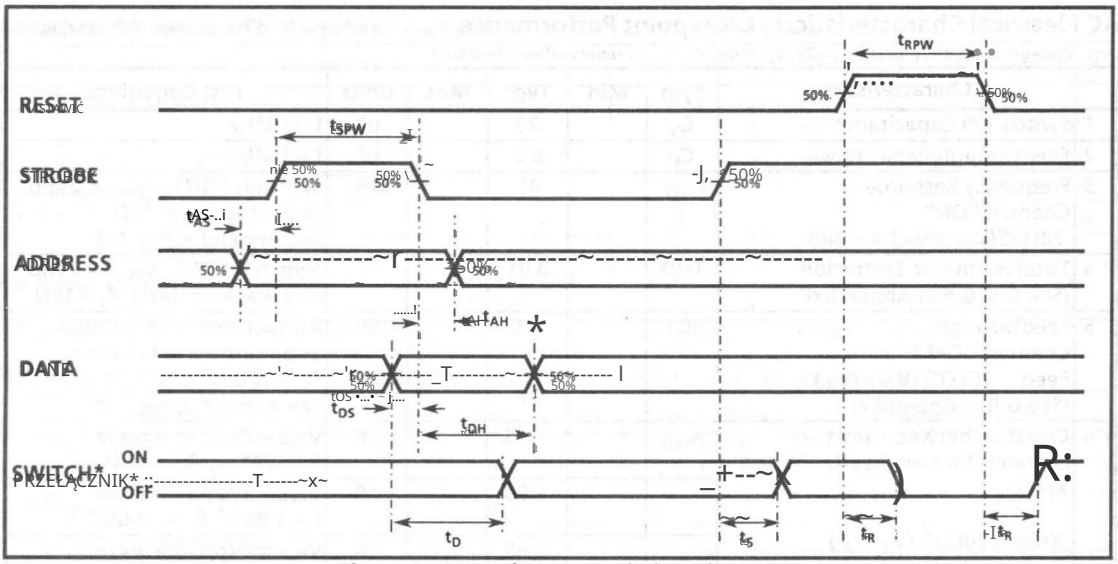

Figure 2 - Control Memory Timing Diagram

Rysunek 2 — Diagram czasowy pamięć sterującej

*See Appendix, Fig. A-7 for switching waveform

Zobacz załącznik, Rys. A-7 dla przełączania

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	0	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	0	1	0	0	0	0	No Connection ①
1	1	1	0	0	0	0	No Connection ①
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
0	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection ①
1	1	1	1	0	0	0	No Connection ①
0	0	0	0	1	0	0	X0-Y1
1	0	0	0	1	0	0	X1-Y1
0	0	0	0	0	1	0	X0-Y2
1	0	0	0	0	1	0	X1-Y2
0	0	0	0	1	1	0	X0-Y3
1	0	0	0	1	1	0	X1-Y3
0	0	0	0	0	0	1	X0-Y4
1	0	0	0	0	0	1	X1-Y4
0	0	0	0	1	0	1	X0-Y5
1	0	0	0	1	0	1	X1-Y5
0	0	0	0	0	1	1	X0-Y6
1	0	0	0	0	1	1	X1-Y6
0	0	0	0	1	1	1	X0-Y7
1	0	0	0	1	1	1	X1-Y7

Table 1 - Address Decode Truth Table

Tabela 1 - Tabela prawdy dekodowania adresów

① This address has no effect on device status.

① Ten adres nie ma wpływu na stan urządzenia.

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Pin Description

Opis wyprowadzeń

Pin #* Numer	Name Nazwa	Description Opis
1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array. Y3 Analogowe (wejście/wyjście): jest on podłączony do modułu Y3 tablicy przełączników.
2	AX2	X2 Address Line (Input). Wiersz adresu X2 (wejścia).
3	RESET	Master RESET (Input): this is used to turn off all switches. Active High. RESET Master RESET (wejście): służy do wyłączania wszystkich przełączników. Aktywny wysoki.
4,5	AX3,AX0	X3 and X0 Address Lines (Inputs). Linie adresowe AX3, AX0 X3 i X0 (wejścia).
6,7	NC	No Connection. NC Brak połączenia.
8-13	X6-X11	X6-X11 Analog (Inputs/Outputs): these are connected to the X6-X11 rows of the switch array. X6-X11 Analogowe (wejścia/wyjścia): tablica są one podłączone do rzędów X6-X11 przełączników.
14	NC	No Connection. NC Brak połączenia.
15	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array. Y7 Analog (wejście/wyjście): jest on podłączony do kolumny Y7 tablicy przełączników.
16	NC	No Connection. NC Brak połączenia.
17	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array. Y6 Analog wejście/wyjście): jest on podłączony do kolumny Y6 tablicy przełączników.
18	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High. STROBE STROBE (wejście): włącza funkcję wybraną przez adres i dane. Adres musi być stabilny przed osiągnięciem przez STROBE stanu wysokiego, a DATA musi być stabilny na opadającym zboczu STROBE. Aktywny wysoki.
19	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array. Y5 Analogowe wejście/wyjście): jest on podłączony do modułu Y5 tablicy przełączników.
20	VSS	Ground Reference. Punkt odniesienia masy.
21	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array. Y4 Analogowe wejście/wyjście): jest on podłączony do kolumny Y4 tablicy przełączników.
22,23	AX1,AX2	X1 and X2 Address Lines (Inputs). Linie adresowe AX1, AX2 X1 i X2 (wejścia).
24,25	AY0,AY1	Y0 and Y1 Address Lines (Inputs). 24,25 AY0,AY1 vO i Y1 Linie adresowe (wejścia).
26,27	NC	No Connection. Brak połączenia.
28-33	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array. X5-XO X5-XO Analogowe (wejścia/wyjścia): są one podłączone do rzędów X5-XO przełącznika szyk.
34	NC	No Connection. NC Brak połączenia.
35	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array. YO YO Analogowe (wejście/wyjście): jest on podłączony do kolumny YO tablicy przełączników.
36	NC	No Connection. NC Brak połączenia.
37	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array. Y1 Analog (wejście/wyjście): jest on podłączony do kolumny Y1 tablicy przełączników.
38	DATA	DATA (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High. DANE DANE (wejście): wejście logiczne o wysokiej wartości włączy wybrany przełącznik, a wejście logiczne o niskiej wartości wyłącz wybrany przełącznik. Active High.
39	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array. Y2 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y2 tablicy przełączników.
40	VDD	Positive Power Supply. Zasilanie VDD dodatnie.

* Plastic DIP and CERDIP only.
Tylko plastik DIP i CERDIP.

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Functional Description

Opis funkcjonalny

The MT8812 is an analog switch matrix with an array size of 8 X 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y input/output lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned on and provide a high degree of isolation when turned off. The control memory consists of 96 bit words (8 bits by 12 bits) in which the bits are selected by the address input lines (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input line. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input line will asynchronously return all memory locations to logical "0" turning off all crosspoint switches.

Matryca przełączników 8 x 12 ma rozmiar 8 kolumn na 12 wierszy. Kolumny są określane jako linie wejścia/wyjścia Y, a wiersze jako linie wejścia/wyjścia X. Każde połączenie przełącznika krzyżowego łączy dowolną linię X z dowolną linią Y po wprowadzeniu odpowiednich słów do pamięci RAM sterującej. Pamięć sterująca składa się z 96 słów (8 bitów na 12 bitów), w której wybierane są bity, w których wybierane są linie wejściowe adresu (AY0-AY2, AX0-AX3). Dane są prezentowane w pamięci na linii wejściowej DANE. Dane są asynchronicznie zapisywane w pamięci, gdy wejście STROBE jest wysokie, i są zatrzaskiwane na opadającym zboczu STROBE. Logiczne „1” zapisane w komórce pamięci powoduje odpowiedni przełącznik krzyżowego, a logiczne „0” wyłącza punkt krzyżowy. Tylko przełączniki krzyżowe odpowiadające adresowanej pamięci ulegają zmianie, gdy dane są zapisywane w pamięci. Pozostałe przełączniki zachowują swój poprzedni stan. Dowolna kombinacja linii X i Y może być połączona poprzez ustawienie odpowiednich wzorców w pamięci sterującej. Logiczne „1” na wejściu RESET asynchronicznie zwraca wszystkie lokalizacje pamięci do logicznego „0”, wyłączając wszystkie przełączniki krzyżowe.

Address Decode

Dekodowanie adresów

The seven address lines, along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

Siedem linii adresowych wraz z wejściem STROBE są logicznie AND-owanych, aby utworzyć sygnał włączający dla resetowalnych przezroczystych zatrzasków. Wejście DANE jest buforowane i jest używane jako wejście do wszystkich zatrzasków. Aby zapisać do lokalizacji, RESET musi być niski, podczas gdy linie adresu i danych są ustawione. Następnie wejście STROBE jest ustawiane wysoko, a następnie nisko, powodując zatrzaśnięcie danych. Dane można zmieniać, gdy STROBE jest wysoki, jednak odpowiedni przełącznik będzie włączany i wyłączany zgodnie z danymi. Dane muszą być stabilne na opadającym zboczu STROBE, aby poprawne dane zostały zapisane do zatrzasku.

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Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage 4.5V to 14.5V
- 3.5Vpp analog signal capability
- 8ns 650 max @ V_{DD} = 14V, 25°C
- R_{ON} = 100 @ V_{DD} = 14V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology

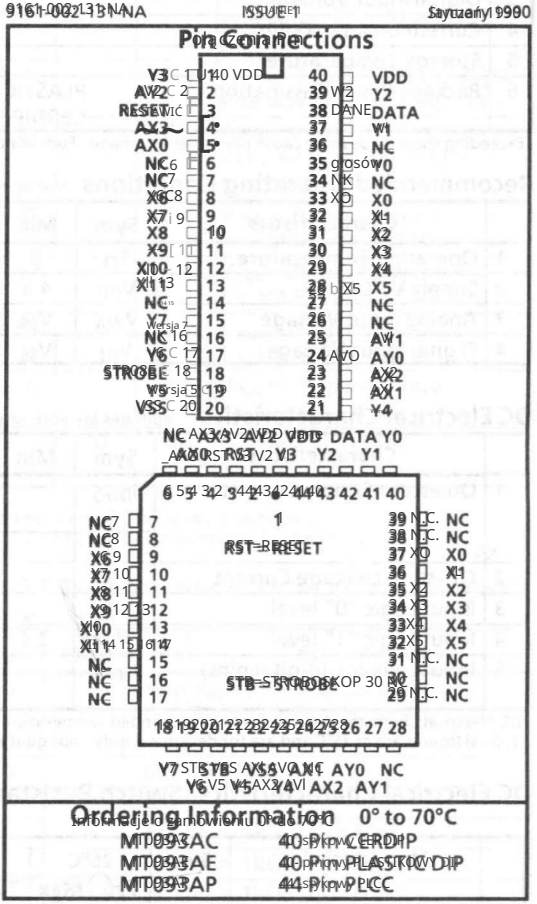
Applications

- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT093 is fabricated in Mitel's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuitry. Any one of the 96 switches can be addressed by selecting the appropriate seven input bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.

Pin Connections



Ordering Information

MT093AC	40 Pin CERDIP
MT093AE	40 Pin PLASTIC DIP
MT093AP	44 Pin PLCC

0° to 70°C

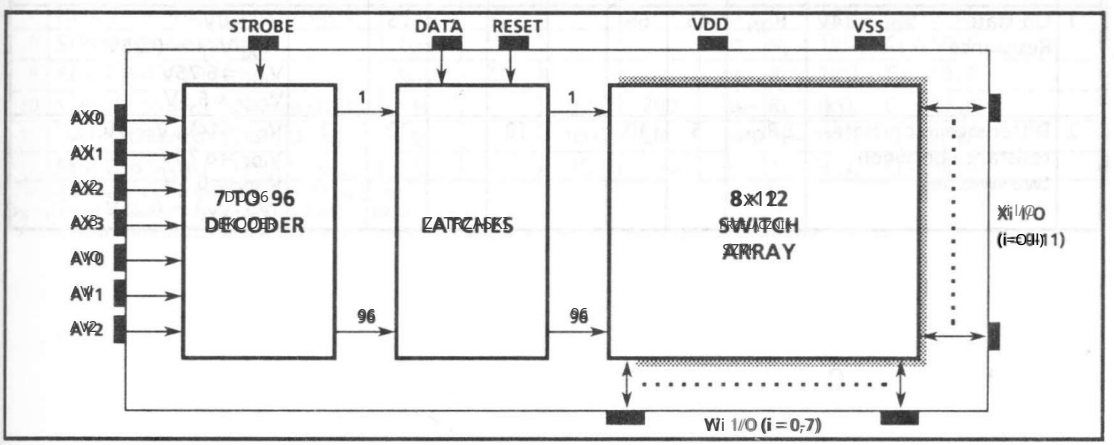


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne napięcie wynosi 0 V. Napięcia podane są względem napięcia ujemnego, chyba że podano inaczej.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	16.0	V
		V_{SS}	-0.3	V_{DD}+0.3	V
2	Analog Input Voltage	V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin	I		±15	mA
5	Storage Temperature	T_{ST}	-65	+150	°C
6	Package Power Dissipation PLASTIC DIP	P_D		0.6	W
	CERDIP	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Funkcjonalne działanie w tych warunkach nie jest domniemane.

Recommended Operating Conditions

Voltages are with respect to V_{SS} unless otherwise stated

Zalecane warunki pracy - napięcia podane są w odniesieniu do Vssuny, chyba że podano inaczej.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	0	25	70	°C	
2	Supply Voltage	V_{DD}	4.5		14.5	V	
3	Analog Input Voltage	V_{INA}	kontra V_{SS}		3.5	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics†

Charakterystyka elektryczna - napięcia odnoszą się do Vss=0V i Voo=+4V, chyba że zaznaczono inaczej

Voltages are with respect to V_{SS} = 0V and V_{DD} = +4V, unless otherwise stated . = 14V unless otherwise stated .

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DDQ}		1	100	µA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				7	15	mA	All digital inputs at $V_{IN}=2.4V$
2	Off-state Leakage Current	I_{OFF}			±1	µA	$\|V_X-V_Y\|=V_{DD}-V_{SS}$
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V_{IH}	2.4			V	
5	Input Leakage (digital pins)	I_{LEAK}			10	µA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Parametry elektryczne przekraczają zalecany zakres temperatur. Zalecane napięcie zasilania.

Typowe wartości podano w temperaturze 25°C i mają one jedynie charakter pomocniczy przy projektowaniu. Nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics - Switch Resistance

Charakterystyka elektryczna DC - rezystancja przełączania - V_{OO} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		60°C		70°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance	R_{ON}	45	65				75	Ω	$V_{SS}=0V$, $\|V_X-V_Y\|=0.25V$ $V_{DD}=6.75V$ $V_{DD}=6.5V$
2	Difference in on-state resistance between two switches	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=14V$, $V_{SS}=0$, $V_{DD}=6.75V$ $V_{DD}=6.5V$ $\|V_X-V_Y\|=0.25V$

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AC Electrical Characteristics† - Crosspoint Performance - V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD}=7V, V_{DC}=0V, V_{SS}=-7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" 20LOG(V_{OUT}/V_{Xi}) = -3dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ
4	Total Harmonic Distortion	THD		0.05		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ
5	Feedthrough Channel "OFF" Feed. = 20LOG(V_{OUT}/V_{Xi})	FDT		-95		dB	All Switches "OFF"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ.
6	Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk = 20LOG(V_{Yj}/V_{Xi}).	X_{talk}		-45		dB	V_{INA} = 2Vpp sine wave f = 10MHz; R_L = 75Ω.
				-90		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 600Ω.
				-85		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 1kΩ.
				-80		dB	V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 10kΩ.
7	Propagation delay through switch	t_{PS}			50	ns	R_L = 1kΩ; C_L = 50pF

† Timing is over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIP only, crosstalk values for PLCC package are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings - V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD}=7V, V_{DC}=0V, V_{SS}=-7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		50		mVpp	V_{IN} = 3V + V_{DC} squarewave; R_{IN} = 1kΩ, R_L = 10kΩ.
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1MHz
3	Switching Frequency	F_O			10	MHz	
4	Setup Time DATA to STROBE	t_{DS}	20			ns	R_L = 1kΩ, C_L = 50pF
5	Hold Time DATA to STROBE	t_{DH}	20			ns	R_L = 1kΩ, C_L = 50pF
6	Setup Time Address to STROBE	t_{AS}	20			ns	R_L = 1kΩ, C_L = 50pF
7	Hold Time Address to STROBE	t_{AH}	20			ns	R_L = 1kΩ, C_L = 50pF
8	STROBE Pulse Width	t_{SPW}	40			ns	R_L = 1kΩ, C_L = 50pF
9	RESET Pulse Width	t_{RPW}	80			ns	R_L = 1kΩ, C_L = 50pF
10	STROBE to Switch Status Delay	t_S		80	200	ns	R_L = 1kΩ, C_L = 50 pF
11	DATA to Switch Status Delay	t_D		100	200	ns	R_L = 1kΩ, C_L = 50 pF
12	RESET to Switch Status Delay	t_R		70	200	ns	R_L = 1kΩ, C_L = 50 pF

† Timing is over recommended temperature range.
Digital Input rise time (tr) and fall time (tf) = 10ns.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

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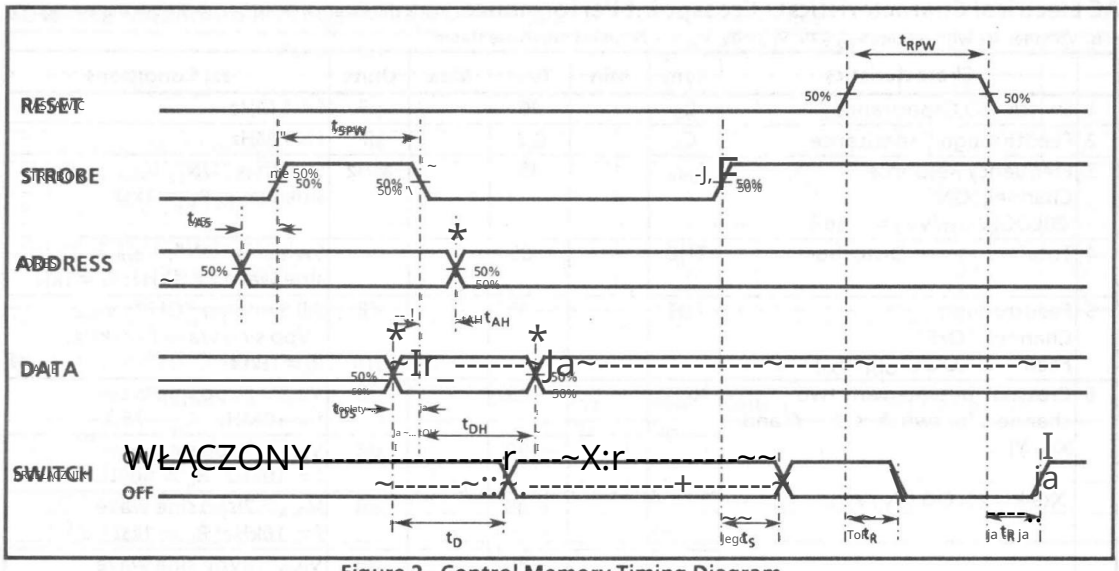

Figure 2. Control Memory Timing Diagram

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection ①
1	1	1	0	0	0	0	No Connection ①
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection ①
1	1	1	1	0	0	0	No Connection ①
0	0	0	0	1	0	0	X0-Y1
1	0	1	0	1	0	0	X11-Y1
0	0	0	0	0	1	0	X0-Y2
1	0	1	0	0	1	0	X11-Y2
0	0	0	0	1	1	0	X0-Y3
1	0	1	0	1	1	0	X11-Y3
0	0	0	0	0	0	1	X0-Y4
1	0	1	0	0	0	1	X11-Y4
0	0	0	0	1	0	1	X0-Y5
1	0	1	0	1	0	1	X11-Y5
0	0	0	0	0	1	1	X0-Y6
1	0	1	0	0	1	1	X11-Y6
0	0	0	0	1	1	1	X0-Y7
1	0	1	0	1	1	1	X11-Y7

Table 1. Address Decoder Truth Table

① This address has no effect on device status.

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Pin Description
Opis pinezek

Pin #* Patka #*	Name Nazwa	Description Opis
1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array. Y3 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y3 tablicy przełączników.
2	AX2	**X2 Address Line (Input).** X2 Linia adresu (wejście).
3	RESET	**Master RESET (Input):** this is used to turn off all switches. Active High. RESET Główny RESET (wejście): służy do wyłączania wszystkich przełączników. Aktywny wysoki.
4,5	AX3 AX0	**X3 and X0 Address Lines (Inputs).** Linie adresowe AX3, AX0 X3 i X0 (wejścia).
6,7	NC	**No Connection.** NC Brak połączenia.
8-13	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array. X6-X11 Analogowe (wejścia/wyjścia): są one połączone z rzędami X6-X11 tablicy przełączników.
14	NC	**No Connection.** NC Brak połączenia.
15	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array. Y7 Analog (wejście/wyjście): jest on podłączony do kolumny Y7 tablicy przełączników.
16	NC	**No Connection.** NC Brak połączenia.
17	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array. Y6 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y6 tablicy przełączników.
18	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High. STROBE STROBE (Wejście): włącza funkcję wybraną przez adres i dane. Adres musi być stabilny zanim STROBE przejdzie w stan wysoki, a DATA musi być stabilny na górnej krawędzi STROBE. Aktywny wysoki.
19	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array. Y5 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y5 tablicy przełączników.
20	VSS	**Ground Reference.** Punkt odniesienia masy.
21	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array. Y4 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y4 tablicy przełączników.
22,23	AX1 AX2	**X1 and X2 Address Lines (Inputs).** 22,23 AX1, AX2 Linie adresowe X1 i X2 (wejścia).
24,25	AY0 AY1	**Y0 and Y1 Address Lines (Inputs).** 24,25 AY0, AY1 Y0 i Y1 linie adresowe (wejścia).
26,27	NC	**No Connection.** 26,27 NC Brak połączenia.
28-33	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array. X5-X0 X5-X0 Analogowe (wejścia/wyjścia): są one połączone z rzędami X5-X0 przełącznika czyk.
34	NC	**No Connection.** NC Brak połączenia.
35	Y0	**Y0 Analog (Input/Output):** this is connected to the Y0 column of the switch array. Y0 Y0 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y0 tablicy przełączników.
36	NC	**No Connection.** NC Brak połączenia.
37	Y1	**Y1 Analog (Input/Output):** this is connected to the Y1 column of the switch array. Y1 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y1 tablicy przełączników.
38	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High. DANE DANE (Wejście): logiczny wysoki stan wejściowy włączy wybrany przełącznik, a logiczny niski stan wejściowy wyłącz wybrany przełącznik. Aktywny wysoki.
39	Y2	**Y2 Analog (Input/Output):** this is connected to the Y2 column of the switch array. Y2 Analogowe (wejście/wyjście): jest on podłączony do kolumny Y2 tablicy przełączników.
40	VDD	**Positive Power Supply.** Zasilanie VDD dodatnie.

* Plastic DIP and CERDIP only.
* Tylko plastik DIP i CERDIP.

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Functional Description

Opis funkcjonalny

The MT093 is an analog switch matrix with an array size of 8 × 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referenced as the Y input lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned on and provide a high degree of isolation when turned off. The control memory consists of 96 bit word by 1 bit RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data presented to the memory, at the DATA input line, is written into the memory when the STROBE input is high and latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input line will asynchronously return all memory locations to logical "0" turning off all crosspoint switches.

MT093 to analogowa macierz przełączników o rozmiarze tablicy 8 × 12. Macierz przełączników jest tworzona tak, jak jest ułożona. Oznacza to, że kolumn jest 8, a wierszy 12. Kolumny są oznaczane jako wejściowe linie Y, a wiersze jako wejściowe/wyjściowe linie X. Analogowa macierz przełączników przełączy dowolną linię X z dowolną linią Y, gdy zostanie włączona, i zapewni wysoki stopień izolacji, gdy zostanie wyłączona. Pamięć sterująca składa się z 96 słów po 1 bicie RAM, do których zapisywane są wybrane przez linie wejściowe adresu (AY0-AY2, AX0-AX3). Dane są prezentowane pamięci na linii wejściowej DATA. Dane są zapisywane do pamięci, gdy wejście STROBE jest wysokie, i jest blokowane na opadającym zboczu STROBE. Dane, które mają zostać zapisane w pamięci, należy przedstawić na linii DATA. Dane muszą być stabilne na opadającym zboczu STROBE, aby dane zostały poprawnie zapisane do pamięci. Pozostałe przełączniki zachowują swoje poprzednie stany. Dowolna kombinacja linii X i Y może być połączona poprzez ustanowienie odpowiednich wzorców w pamięci sterującej. Logiczna „1" na wejściu RESET asynchronicznie zwróci wszystkie lokalizacje pamięci do logicznego „0", wyłączając wszystkie przełączniki krzyżowe.

Address Decode

Dekodowanie adresu

The seven address lines, along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

Siedem linii adresowych wraz z wejściem STROBE jest logicznie AND w celu utworzenia sygnału włączającego dla resetowalnych przezroczystych zatrzasków. Wejście DATA jest buforowane i jest używane jako wejście do wszystkich zatrzasków. Aby zapisać do lokalizacji, RESET musi być niski, podczas gdy linie adresowe i danych są ustawione. Następnie wejście STROBE jest ustawiane wysoko, a następnie nisko, powodując zatrzaśnięcie danych. Dane można zmieniać, gdy STROBE jest wysoki, jednak odpowiedni przełącznik będzie włączany i wyłączany zgodnie z danymi. Dane muszą być stabilne na opadającym zboczu STROBE, aby dane zostały poprawnie zapisane do zatrzasku.

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MITEL®

8 x 12 tablica przełączników analogowych

9161-002-100-NA | WYDANIE 2 | Listopad 1988

Cechy

- Wewnętrzne zatrzaski sterujące i dekoder adresowy
- Krótki czas przygotowania i utrzymania
- Szeroki zakres napięcia roboczego: 4,5 V do 13,2 V
- Możliwość obsługi sygnału analogowego 12 Vpp
- R_{ON} 65Ω maks. @ V_{DD} = 12V, 25°C
- ΔR_{ON} ≤ 10Ω @ V_{DD} = 12V, 25°C
- Pełny przełącznik CMOS zapewniający niskie zniekształcenia
- Minimalny przepust i przesłuchy
- Oddzielne źródła zasilania analogowego i cyfrowego
- Technologia ISO-CMOS o niskim zużyciu energii

Aplikacje

- Systemy kluczowe
- Systemy PBX
- Radio mobilne
- Sprzęt testowy / instrumentacja
- Multipleksery analogowo-cyfrowe
- Przełączanie Audio/Wideo

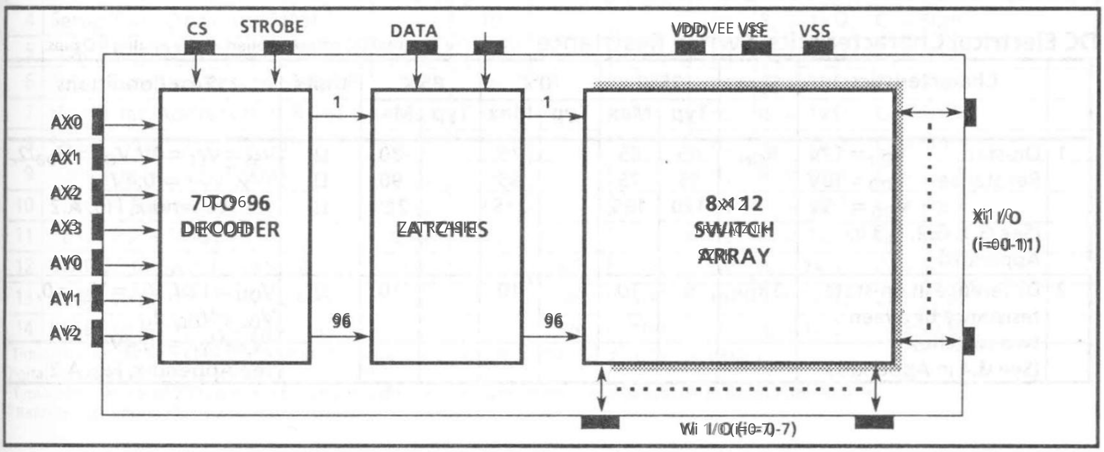
Opis

Mitel MT8814 jest wykonany w technologii ISO-CMOS firmy MITEL, technologia zapewniająca niskie rozpraszanie mocy i wysoką niezawodność. Urządzenie zawiera 8 x 12 tablic przełączniki krzyżowe wraz z linią 7 do 96 obwody dekodera i zatrzasku. Każdy z 96 przełączników można adresować poprzez wybranie odpowiedniego siedmiobitowego adresu. Wybrany przełącznik można włączyć lub wyłączyć, stosując logiczną jedynkę lub zero do wejścia DATA. V_{SS} jest odniesieniem masy wejść cyfrowych. Zakres analogowego sygnał pochodzi z V_{DD} do V_{EE}. Chip Select (CS) umożliwia tablicę punktów krzyżowych do kaskadowania dla macierzy rozszerzenie.

Połączenia pinowe

Informacje o zamówieniu -40° do 85°C

MT8814AC	40-stykowy CERDIP
MT8814AE	40-pinowy PLASTIKOWY DIP
MT8814AP	44-stykowy PLCC



Rysunek 1 - Schemat blokowy funkcji

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Absolute Maximum Ratings*

Maksymalne wartości bezwzględne* – Napięcia odniesione do V_{EE}, chyba że podano inaczej

Voltages are with respect to V_{EE} unless otherwise stated

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage (Napięcie zasilania)	V_{DD}	-0.3	15.0	V
		V_{SS}	-0.3	V_{DD}+0.3	V
2	Analog Input Voltage (Napięcie wejściowe analogowe)	V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage (Napięcie wejściowe cyfrowe)	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin (Prąd przez dowolny pin wyjściowy)	I		±15	mA
5	Storage Temperature (Temperatura przechowywania)	T_S	-65	+150	°C
6	Package Power Dissipation (Pakiet rozpraszania mocy) PLASTIC DIP (Plastikowa obudowa DIP)	P_D		0.6	W
	CERDIP	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Funkcjonalne działanie w tych warunkach nie jest domyślne.

Recommended Operating Conditions

Zalecane warunki pracy – Napięcia podano w odniesieniu do V_{EE}, chyba że podano inaczej

Voltages are with respect to V_{EE} unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature (Temperatura robocza)	T_O	-40	25	85	°C	
2	Supply Voltage (Napięcie zasilania)	V_{DD}	V_{SS}+4.5		13.2	V	
		V_{SS}	V_{EE}		V_{DD}-4.5	V	
3	Analog Input Voltage (Napięcie wejściowe analogowe)	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage (Cyfrowe napięcie wejściowe)	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics†

DC Charakterystyka elektryczna – Napięcia odniesione są do V_{EE} = V_{SS} = 0V, V_{DD} = zadane, chyba że podano inaczej

Voltages are with respect to V_{EE} = V_{SS} = 0V, V_{DD} = as given, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current (Prąd zasilania spoczynkowego)	I_{DD}		1	100	µA	All digital inputs at V_{IN} = V_{SS} or V_{DD} (Wszystkie wejścia cyfrowe na V_{IN} = V_{SS} lub V_{DD})
				0.4	1.5	mA	All digital inputs at V_{IN} = 2.4 + V_{SS} (V_{SS} = 7.0V) (Wejścia cyfrowe na V_{IN} = 2,4 + V_{SS} (V_{SS} = 7,0V))
				5	15	mA	All digital inputs at V_{IN} = 3.4V (Wejścia cyfrowe na V_{IN} = 3,4V)
2	Off-state Leakage Current (See Fig. G.9 in Appendix) (Prąd upływu w stanie wyłączonym (Zobacz rys. G.9 w Dodatku))	I_{OFF}		±1	±500	nA	V_{IN} = V_{DD} − V_{EE} (See Appendix, Fig. A.1) (V_{IN} = V_{DD} − V_{EE} (Zobacz Dodatek, rys. A.1))
3	Input Logic "0" Level (Poziom logiczny wejściowej "0")	V_{IL}			0.8+V_{SS}	V	V_{SS} = 7.5V; V_{EE} = 0V (V_{SS} = 7,5 V; V_{EE} = 0V)
4	Input Logic "1" Level (Poziom logiczny wejściowej "1")	V_{IH}	2.0+V_{SS}			V	V_{SS} = 6.5V; V_{EE} = 0V (V_{SS} = 6,5V; V_{EE} = 0V)
5	Input Logic "1" Level (Poziom logiczny wejściowej "1")	V_{IH}	3.3			V	
6	Input Leakage (Digital pins) (Upływ sygnału wejściowego (cyfrowe piny))	I_{IN}		0.1	10	µA	All digital inputs at V_{IN} = V_{SS} or V_{DD} (Wszystkie wejścia cyfrowe przy V_{IN} = V_{SS} lub V_{DD})

†DC Electrical Characteristics are over recommended temperature range.
†Charakterystyka elektryczna prądu stałego w zalecanym zakresie temperatur.
‡Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
‡Typowe wartości w temperaturze 25°C służą jedynie jako pomoc projektowa, nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics: Switch Resistance

DC Charakterystyka elektryczna – rezystancja przełącznika (Typowe wartości w temperaturze 25°C. Zewnętrzne napięcie V_{DE} jest przyłożone do analogowych pinów I/O.)

Typical figures at 25°C. External voltage V_{DE} is applied to the analog I/O pins.

	Characteristics	Sym	25°C		70°C		85°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	ON-state Resistance (Rezystancja w stanie ON) V_{DD} = 12V (See Fig. G.2, G.3 in Appendix) (V_{DD} = 12V (Zobacz rys. G.2, G.3 w Dodatku))	R_{ON}	45	65	75		80		Ω	V_{SS} = 0V, V_{DC} = V_{DD}/2, V_{IN} = 0.4V (V_{SS} = 0V, V_{DC} = V_{DD}/2, V_{IN} = 0,4V) See Appendix, Fig. A.2 (Zobacz Dodatek, rys. A.2)
	V_{DD} = 10V		55	75	85		90		Ω	
	V_{DD} = 5V		120	185	215		225		Ω	
2	Difference in ON-state resistance between two switches (See Fig. G.4 in Appendix) (Różnica w rezystancji w stanie ON między dwoma przełącznikami (Zobacz rys. G.4 w Dodatku))	ΔR_{ON}	5	10	10		10		Ω	V_{DD} = 12V, V_{SS} = V_{EE} = 0, V_{DC} = V_{DD}/2, V_{IN} = 0.4V (V_{DD} = 12V, V_{SS} = V_{EE} = 0, V_{DC} = V_{DD}/2, V_{IN} = 0,4V) See Appendix, Fig. A.2 (Zobacz Dodatek, rys. A.2)

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AC Electrical Characteristics† - Crosspoint Performance

Voltages are with respect to V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi}) = -3dB$	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ
5	Feedthrough Channel "OFF" $Feed. = 20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi - Yi and Xj - Yj. $Xtalk = 20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		-45		dB	V_{INA} = 2Vpp sine wave f = 10MHz; R_L = 75Ω.
				-90		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 600Ω.
				-85		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 1kΩ.
				-80		dB	V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L = 1kΩ; C_L = 50pF

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIP only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

Voltages are with respect to V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN} = 3V squarewave; R_{IN} = 1kΩ, R_L = 10kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
8	Setup Time CS to STROBE	t_{CSS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
9	Hold Time CS to STROBE	t_{CSH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
10	STROBE Pulse Width	t_{SPW}	20			ns	R_L = 1kΩ, C_L = 50pF ①
11	RESET Pulse Width	t_{RPW}	40			ns	R_L = 1kΩ, C_L = 50pF ①
12	STROBE to Switch Status Delay	t_S		40	100	ns	R_L = 1kΩ, C_L = 50 pF ①
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L = 1kΩ, C_L = 50 pF ①
14	RESET to Switch Status Delay	t_R		35	100	ns	R_L = 1kΩ, C_L = 50 pF ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

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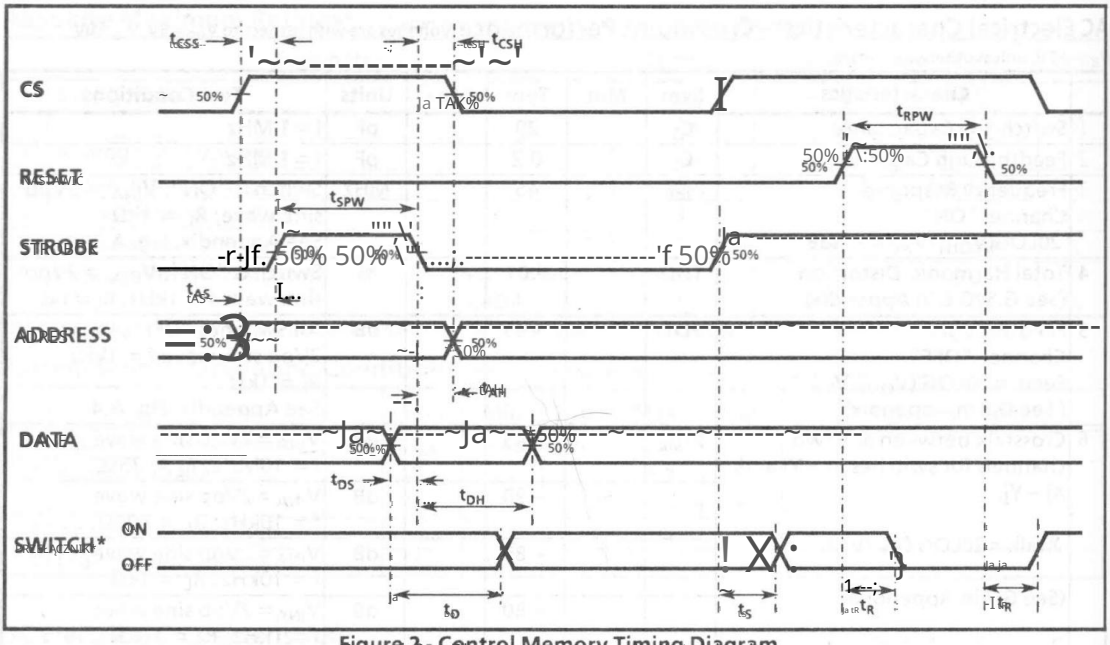

Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection
1	1	1	0	0	0	0	No Connection
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection
1	1	1	1	0	0	0	No Connection
0	0	0	0	1	0	0	X0-Y1
1	0	1	1	1	0	0	X11-Y1
0	0	0	0	0	1	0	X0-Y2
1	0	1	1	0	1	0	X11-Y2
0	0	0	0	1	1	0	X0-Y3
1	0	1	1	1	1	0	X11-Y3
0	0	0	0	0	0	1	X0-Y4
1	0	1	1	0	0	1	X11-Y4
0	0	0	0	1	0	1	X0-Y5
1	0	1	1	1	0	1	X11-Y5
0	0	0	0	0	1	1	X0-Y6
1	0	1	1	0	1	1	X11-Y6
0	0	0	0	1	1	1	X0-Y7
1	0	1	1	1	1	1	X11-Y7

Table 1 - Address Decode Truth Table

This address has no effect on device status

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Pin Description

Opis pinów

Pin #*	Name	Description
1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array.
2	AY2	Y2 Address Line (Input).
3	RESET	Master RESET (Input): this is used to turn off all switches regardless of the condition of CS. Active High.
4,5	AX3,AX0	X3 and X0 Address Lines (Inputs).
6,7	NC	No Connection.
8-13	X6-X11	X6-X11 Analog (Inputs/Outputs): these are connected to the X6-X11 rows of the switch array.
14	NC	No Connection
15	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array.
16	VSS	Digital Ground Reference .
17	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array.
18	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array.
20	VEE	Negative Power Supply.
21	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array.
22,23	AX1,AX2	X1 and X2 Address Lines (Inputs).
24,25	AY0,AY1	Y0 and Y1 Address Lines (Inputs).
26,27	NC	No Connection.
28-33	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array.
34	NC	No Connection.
35	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array.
36	CS	Chip Select (Input): this is used to select the device. Active High.
37	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array.
38	DATA	DATA (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array.
40	VDD	Positive Power Supply.

* Plastic DIP and CERDIP only

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Functional Description

The MT8814 is an analog switch matrix with an array size of 8 x 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be connected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0", turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8814 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must be high while the address and data are set up. Then the STROBE input is set high and then low, causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

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Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ $V_{DD} - V_{EE}$ = 12V, 25°C
- ΔR_{ON} = 10Ω @ $V_{DD} - V_{EE}$ = 12V, 25°C
- Full CMOS switches for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

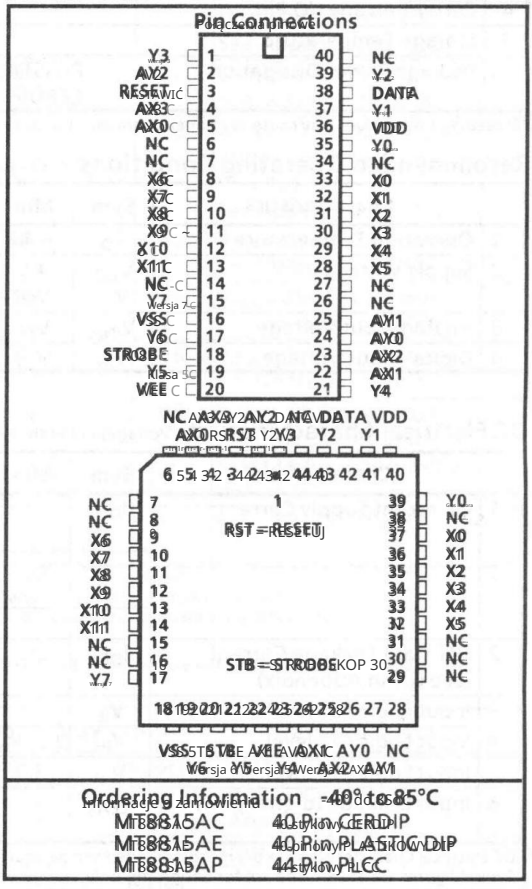
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8815 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 × 12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}.

Pin Connections



Ordering Information

−40°C to 85°C

MT8815AC	40 Pin CERDIP
MT8815AE	40 Pin PLASTIC DIP
MT8815AP	44 Pin PLCC

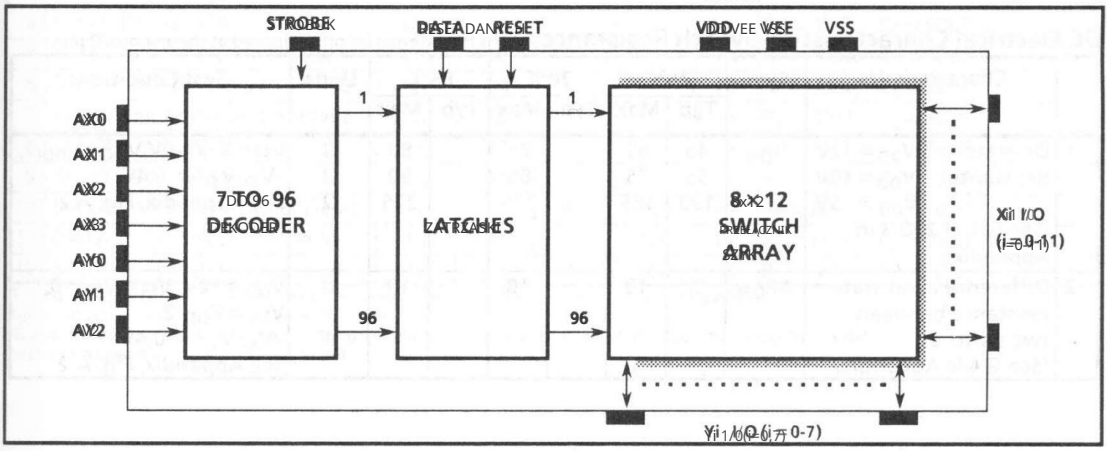


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne wartości bezwzględne* Voltages are with respect to V_{SS} unless otherwise stated. Napięcia odniesione do V_{SS}, chyba że podano inaczej.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage Napięcie zasilania	V_{DD} V_{SS}	-0.3 -0.3	15.0 V_{DD}+0.3	V V
2	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage Wejściowe napięcie cyfrowe	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin Prąd na dowolnym pinie I/O	I		±15	mA
5	Storage Temperature Temperatura przechowywania	T_S	-65	+150	°C
6	Package Power Dissipation Moc rozpraszana przez obudowę	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Działanie funkcjonalne w tych warunkach nie jest domniemane.

Recommended Operating Conditions

Zalecane warunki pracy* Voltages are with respect to V_{EE} unless otherwise stated. Napięcia odniesione do V_{EE}, chyba że podano inaczej.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature Temperatura pracy	T_O	-40	25	85	°C	
2	Supply Voltage Napięcie zasilania	V_{DD} V_{SS} V_{EE}	4.5 V_{EE}		13.2 V_{EE}+5.5	V V	
3	Analog Input Voltage Analogowe napięcie wejściowe	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage Cyfrowe napięcie wejściowe	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics†

Charakterystyka elektryczna DC† Voltages are with respect to V_{EE} unless otherwise stated. Napięcia odniesione do V_{EE}, chyba że podano inaczej.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current Prąd zasilania spoczynkowego	I_{DD}		1	100	µA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD} Wszystkie wejścia cyfrowe przy $V_{IN}=V_{SS}$ lub V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4$ + V_{SS} Cyfrowe wejścia przy $V_{IN}=2.4$ + V_{SS}
				5	15	mA	All digital inputs at $V_{IN}=5.0$ + V_{SS} Wejścia cyfrowe przy $V_{IN}=5.0$ + V_{SS}
2	Off-state Leakage Current Prąd upływu w stanie wyłączonym (See G.9 in Appendix) (Patrz G.9 w Aneksie)	I_{OFF}	±1	±500	nA	$V_{IN}=V_{DD}-V_{EE}$ $V_{IN}=V_{DD}-V_{EE}$ See Appendix, Fig. A.1 Patrz Aneks, Rys. A.1
3	Input Logic "0" level Wejściowy poziom "0"	V_{IL}			$0.8+V_{SS}$	V	$V_{SS}=0$ V; $V_{SS}=7.5$ V; $V_{EE}=0$ V $V_{SS}=6.5$ V; $V_{EE}=-6.5$ V; $V_{EE}=0$ V
4	Input Logic "1" level Wejściowy poziom "1"	V_{IH}	$2.0+V_{SS}$			V	
5	Input Logic "1" level Wejściowy poziom "1"	V_{IH}	3.3			V	
6	Input Leakage (digital pins) Upływ prądu wejściowego (wyjścia cyfrowe)	I_{IN} I_{CLK}		0.1	10	µA	All digital inputs at $V_{IN}=V_{SS}$ to V_{DD} Wszystkie wejścia cyfrowe przy $V_{IN}=V_{SS}$ do V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
† Charakterystyka elektryczna DC jest podana w zalecanym zakresie temperatur.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
‡ Typowe wartości przy 25°C są podane jedynie jako pomoc projektowa; nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics: Switch Resistance

Charakterystyka elektryczna DC: rezystancja przełącznika Unless otherwise noted, $V_{SS}=5$ V, $V_{EE}=-5$ V. Chyba że podano inaczej, $V_{SS}=5$ V, $V_{EE}=-5$ V. Values are measured with external DC probes applied to the analog I/O pins. Wartości są mierzone przy zewnętrznych sondach DC podłączonych do analogowych pinów I/O.

	Characteristics	Sym	25°C		70°C		85°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	Switch on-state Resistance Rezystancja w stanie włączonym $V_{DD}=12$ V $V_{DD}=5$ V $V_{DD}=5$ V (See G.1, G.2, G.3 in Appendix) (Patrz G.1, G.2, G.3 w Aneksie)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=0$ V, $V_{EE}=-6$ V, $V_{DC}=V_{DD}/2$, $V_{SS}=0$ V, $V_{EE}=-5$ V, $|V_{IN}|=0.4$ V See Appendix, Fig. A.2 Patrz Aneks, Rys. A.2
2	Difference in on-state resistance between two switches Różnica rezystancji w stanie włączonym między dwoma przełącznikami (See G.4 in Appendix) (Patrz G.4 w Aneksie)	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12$ V, $V_{SS}=0$ V, $V_{EE}=0$, $V_{DC}=V_{DD}/2$, $|V_{IN}|=0.4$ V See Appendix, Fig. A.2 Patrz Aneks, Rys. A.2

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AC Electrical Characteristics† - Crosspoint Performance

AC Elektryczne charakterystyki† - Charakterystyka przełączania - Voltages are with respect to V_{DD} = 5V, V_{SS} = 0V, względem V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V, chyba że podano inaczej.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
	Charakterystyka	Sym	Min	Typ	Maksymalna liczba punktów	Jednostki	Warunki testowe
1	Switch I/O Capacitance Pojemność wejścia/wyjścia przełącznika	C_{SS}		20		pF	f = 1 MHz
2	Feedthrough Capacitance pojemność przesłuchowa	C_{IF}		0,2		pF	f = 1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{IN}) = -3dB$ 20LOG(VOUT/VIN) = - 3dB	F_{-3dB}		45		MHz	Przełącznik MHz jest w pozycji „ON”, V_{INA} = 2Vpp fala sinusoidalna, R_L = 1kΩ See Appendix Fig. A.3 zobacz załącznik, rys. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix) (zobacz G.5, G.6 w załączniku)	THD		0,01		%	Przełącznik jest „WŁ.”, V_{INA} = 2Vpp fala sinusoidalna f = 1kHz, R_L = 1kΩ
5	Feedthrough Channel "OFF" Feed = 20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix) (zobacz G.8 w załączniku)	FDT		-95		dB	All Switches "OFF"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ. See Appendix Fig. A.4 zobacz załącznik, rys. A.4
6	Crosstalk between any two channels switches Xi – Yi and Xj – Yj. Xtalk = 20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix). (zobacz G.7 w załączniku).	X_{talk}		-45		dB	V_{INA} = 2Vpp sine wave f = 10MHz, R_L = 75Ω.
				-90		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 600Ω.
				-85		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 1kΩ.
				-80		dB	V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 10kΩ. Refer to Appendix Fig. A.5 for test circuit. Zobacz załącznik, rys. A.5, aby uzyskać więcej informacji.
7	Propagation delay through switch Opóźnienie propagacji przez przełącznik	t_{pS}		30	50	ns	R_L = 1kΩ, C_L = 50pF

†Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Typowe wartości podane dla 25°C służą wyłącznie do projektowania, nie są gwarantowane i nie podlegają testom produkcyjnym.
Crosstalk measurements are for Plastic DIPS only. crosstalk values for PLCC packages are approximately 5dB better.
Pomiary przesłuchów dotyczą wyłącznie obudów plastikowych DIP-ów, natomiast wartości przesłuchowania obudów PLCC są o około 5 dB lepsze.

AC Electrical Characteristics† - Control and I/O Timings

Charakterystyka elektryczna prądu przemiennego - Sterowanie i czasy - Napięcia są względem V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V, chyba że podano inaczej.

Voltages are with respect to V_{DD} = 5V, V_{SS} = 0V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
	Charakterystyka	Sym	Min	Typ	Maksymalna liczba punktów	Jednostki	Warunki testowe
1	Control Input crosstalk to switch (for DATA, STROBE, Address) Przełącznik wejściowy sterujący (DATA, STROBE, Adres)	CX_{talk}		30		mVpp	V_{IN} = fala prostokątna 3V; R_{IN} = 1kΩ, R_L = 10kΩ. See Appendix Fig. A.6 zobacz załącznik, rys. A.6
2	Digital Input Capacitance Wejście cyfrowe - Pojemność	C_{DI}		10		pF	f = 1MHz
3	Switching Frequency Częstotliwość przełączania	F_{CD}			20	MHz	
4	Setup Time DATA to STROBE Konfiguracja czasu DATA do STROBE	t_{DS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
5	Hold Time DATA to STROBE Czas trzymania DATA do STROBE	t_{DH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
6	Setup Time Address to STROBE Ustaw adres czasu na STROBE's A5	t_{AS}	10			ns	R_L = 1kΩ, C_L = 50pF ①
7	Hold Time Address to STROBE Czas podtrzymania adresu do STROBE	t_{AH}	10			ns	R_L = 1kΩ, C_L = 50pF ①
8	STROBE Pulse Width Szerokość impulsu STROBE	t_{SPW}	20			ns	R_L = 1kΩ, C_L = 50pF ①
9	RESET Pulse Width Reset Szerokość impulsu	t_{RPW}	40			ns	R_L = 1kΩ, C_L = 50pF ①
10	STROBE to Switch Status Delay STROBE do opóźnienia statusu przełącznika	t_{SS}		40	100	ns	R_L = 1kΩ, C_L = 50 pF ①
11	DATA to Switch Status Delay Opóźnienie w przesyłaniu danych do przełącznika	t_{DD}		50	100	ns	R_L = 1kΩ, C_L = 50 pF ①
12	RESET to Switch Status Delay RESET do opóźnienia statusu przełącznika	t_{RS}		35	100	ns	R_L = 1kΩ, C_L = 50 pF ①

†Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Timing jest powyżej zalecanego zakresu temperatur. Zobacz Rysunek 2 dla sterowania i I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
Czas narastania wejścia cyfrowego (tr) i czas opadania sygnału wejściowego (tf) = 5ns.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Typowe wartości podane dla 25°C służą wyłącznie do projektowania, nie są gwarantowane i nie podlegają testom produkcyjnym.
① Refer to Appendix Fig. A.7 for test circuit.
① Obwód testowy patrz załącznik, rys. A.7.

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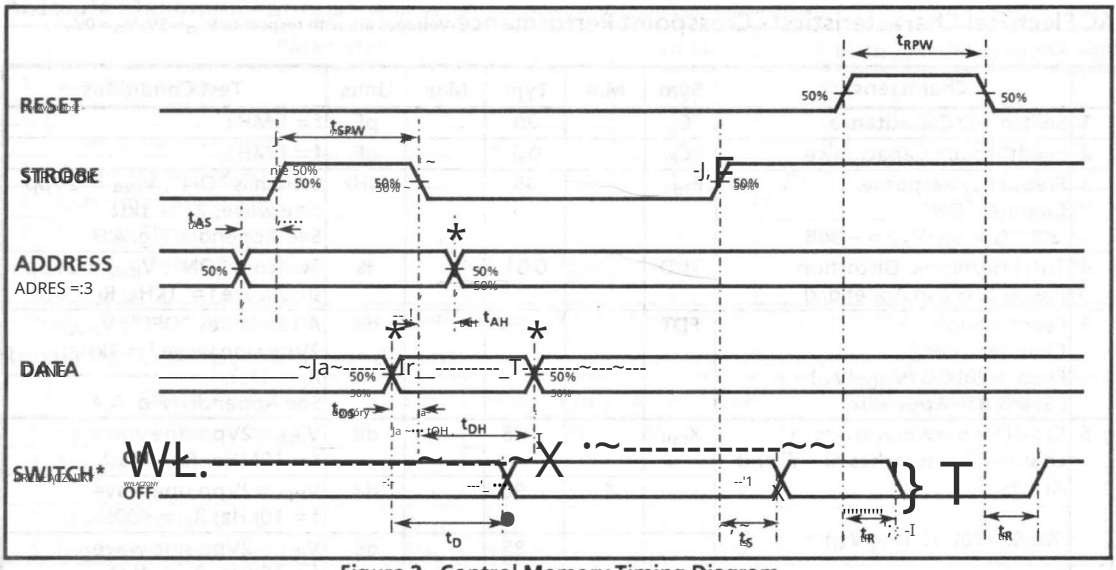

Figure 2 - Control Memory Timing Diagram

Rysunek 2 - Kontrola pamięci Diagram czasowy

*Zobacz Załącznik, Rys. A.7 dla przełączania zwarcia

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection ①
1	1	1	0	0	0	0	No Connection ①
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection ①
1	1	1	1	0	0	0	No Connection ①
0	0	0	0	1	0	0	X0-Y1
1	0	1	1	1	0	0	X11-Y1
0	0	0	0	1	1	0	X0-Y2
1	0	1	1	1	1	0	X11-Y2
0	0	0	0	1	1	0	X0-Y3
1	0	1	1	1	1	0	X11-Y3
0	0	0	0	0	0	1	X0-Y4
1	0	1	1	0	0	1	X11-Y4
0	0	0	0	1	0	1	X0-Y5
1	0	1	1	1	0	1	X11-Y5
0	0	0	0	0	1	1	X0-Y6
1	0	1	1	0	1	1	X11-Y6
0	0	0	0	1	1	1	X0-Y7
1	0	1	1	1	1	1	X11-Y7

Table 1 - Address Decode Truth Table

Tabela 1 - Tabela prawdy dekodowania adresu

① This address has no effect on device status.

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Pin Description

Pin #	Name	Description
1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array.
2	AY2	Y2 Address Line (Input).
3	RESET	Master RESET (Input): this is used to turn off all switches. Active High.
4,5	AX3,AX0	X3 and X0 Address Lines (Inputs): these are used to select X3 and X0 rows of switches.
6,7	NC	No Connection.
8-13	X6-X11	X6-X11 Analog (Inputs/Outputs): these are connected to the X6-X11 rows of the switch array.
14	NC	No Connection
15	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array.
16	VSS	Digital Ground Reference (Input).
17	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array.
18	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array.
20	VEE	Negative Power Supply.
21	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array.
22, 23	AX1,AX2	X1 and X2 Address Lines (Inputs).
24, 25	AY0,AY1	Y0 and Y1 Address Lines (Inputs).
26, 27	NC	No Connection.
28 - 33	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array.
34	NC	No Connection.
35	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array.
36	VDD	Positive Power Supply.
37	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array.
38	DATA	DATA (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array.
40	NC	No Connection.

* Plastic DIP and CERDIP only.

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Functional Description

Opis funkcjonalny

The MT8815 is an analog switch matrix with an array size of 8 X 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of 96 bit write-only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint switch off. Only the crosspoint switches corresponding to the addressed memory location are altered by the data written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8815 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if single voltage reference is needed.

Address Decode

Dekodowanie adresów

The seven address inputs along with the STROBE are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

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MITEL®

ISO-CMOS MT8816
8 x 16 Analog Switch Array

9161-002-101-NA Issue 2 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- Ron 650 max. @ VDD – VEE = 12V, 25°C
- RON matching 100 @ VDD – VEE = 12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

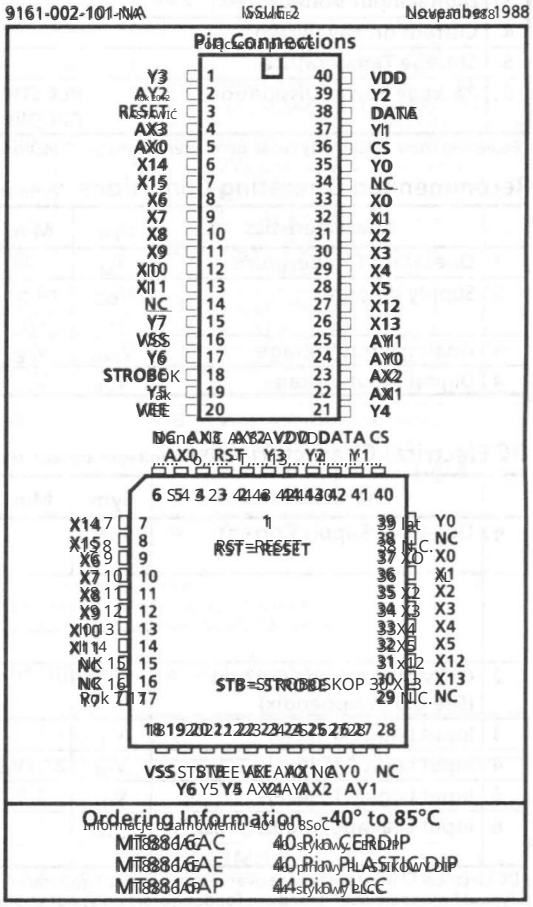
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8816 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 16 array of crosspoint switches along with a 7 to 128 line decoder and latch circuitry. Any one of the 128 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. VSS is the ground reference of the digital inputs. The range of the analog signal is from VEE to VDD. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

Pin Connections



Ordering Information

MT8816AC	40 Pin CERDIP
MT8816AE	40 Pin PLASTIC DIP
MT8816AP	44 Pin PLCC

-40° to 85°C

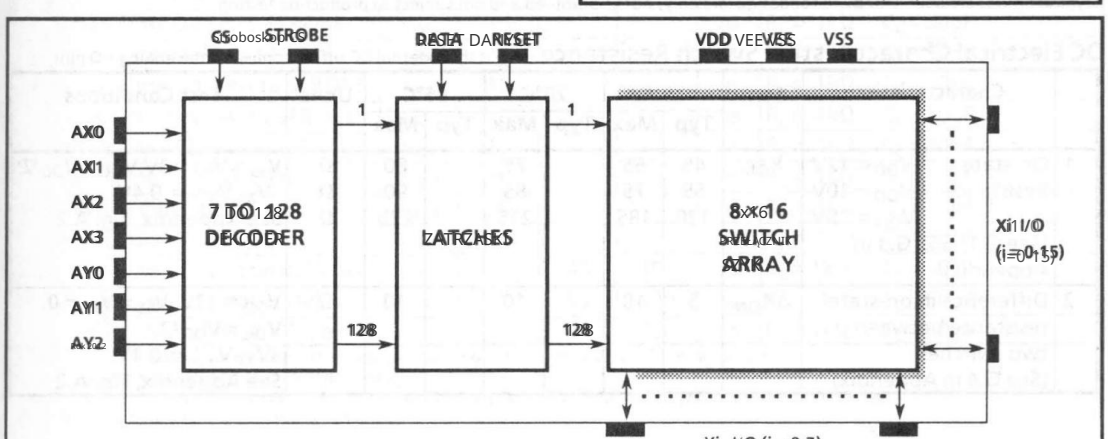


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings* Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD}	-0.3	15.0	V
			V_{SS}	-0.3	V_{DD}+0.3	V
2	Analog Input Voltage		V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P_D		0.6	W
		CERDIP	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	-40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
		V_{SS}	V_{EE}		V_{DD}-4.5	V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4+V_{SS}$; $V_{SS}=7.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert=V_{DD}-V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			0.8+V_{SS}	V	$V_{SS}=7.5V$; $V_{EE}=0V$
4	Input Logic "1" level	V_{IH}	2.0+V_{SS}			V	$V_{SS}=6.5V$; $V_{EE}=0V$
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics		Sym	25°C		70°C		85°C		Units	Test Conditions
				Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance (See G.1, G.2, G.3 in Appendix)	$V_{DD}=12V$	R_{ON}	45	65		75		80	Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert=0.4V$ See Appendix, Fig. A.2
		$V_{DD}=10V$		55	75		85		90	Ω	
		$V_{DD}=5V$		120	185		215		225	Ω	
2	Difference in on-state resistance between two switches (See G.4 in Appendix)		ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert=0.4V$ See Appendix, Fig. A.2

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AC Electrical Characteristics† - Crosspoint Performance

Voltages are with respect to $V_{SS} = 0V$, $V_{EE} = -7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{IN}) = -3dB$	F_{3dB}		45		MHz	Switch is "ON", $V_{INA} = 2Vpp$ sine wave, $R_L = 1k\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON", $V_{INA} = 2Vpp$ sine wave $f = 1kHz$, $R_L = 1k\Omega$
5	Feedthrough Channel "OFF" Feed = $20LOG(V_{OUT}/V_{IN})$ (See G.8 in Appendix)	FDT		-95		dB	All switches "OFF"; $V_{INA} = 2Vpp$ sine wave $f = 1kHz$; $R_L = 1k\Omega$. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi – Yi and Xj – Yj. Xtalk = $20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		-45		dB	$V_{INA} = 2Vpp$ sine wave $f = 10MHz$, $R_L = 75\Omega$.
				-90		dB	$V_{INA} = 2Vpp$ sine wave $f = 10kHz$, $R_L = 600\Omega$.
				-85		dB	$V_{INA} = 2Vpp$ sine wave $f = 10kHz$, $R_L = 1k\Omega$.
				-80		dB	$V_{INA} = 2Vpp$ sine wave $f = 1kHz$, $R_L = 10k\Omega$. Refer to Appendix Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	$R_S = 1k\Omega$, $C_L = 50pF$

† Timings over recommended temperature range, see Fig. 2, see also Fig. 3 for general test and timing details.
‡ Typical figures are at 25°C, and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements apply for plastic DIP and PLCC packages. Crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

Voltages are with respect to $V_{SS} = 0V$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{EE} = -7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	$V_{IN} = 3V$ squarewave; $R_{IN} = 1k\Omega$, $R_L = 10k\Omega$. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1MHz 1MHz
3	Switching Frequency	F_D			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
5	Hold Time DATA to STROBE	t_{DH}	10			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
6	Setup Time Address to STROBE	t_{AS}	10			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
7	Hold Time Address to STROBE	t_{AH}	10			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
8	Setup Time CS to STROBE	t_{CSS}	10			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
9	Hold Time CS to STROBE	t_{CSH}	10			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
10	STROBE Pulse Width	t_{SPW}	20			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
11	RESET Pulse Width	t_{RPW}	40			ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50pF$
12	STROBE to Switch Status Delay	t_S		40	100	ns	$R_L = 1k\Omega$, $C_L = 50$ pF
13	DATA to Switch Status Delay	t_D		50	100	ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50$ pF
14	RESET to Switch Status Delay	t_R		35	100	ns	$R_L = R_{DEL} = 1k\Omega$, $C_L = 50$ pF

† Timings over recommended temperature range, see Fig. 2, see also Fig. 3 for general test and timing details.
‡ Typical figures are at 25°C, and are for design aid only; not guaranteed and not subject to production testing.
§ Refer to Appendix Fig. A.7 for test circuit.

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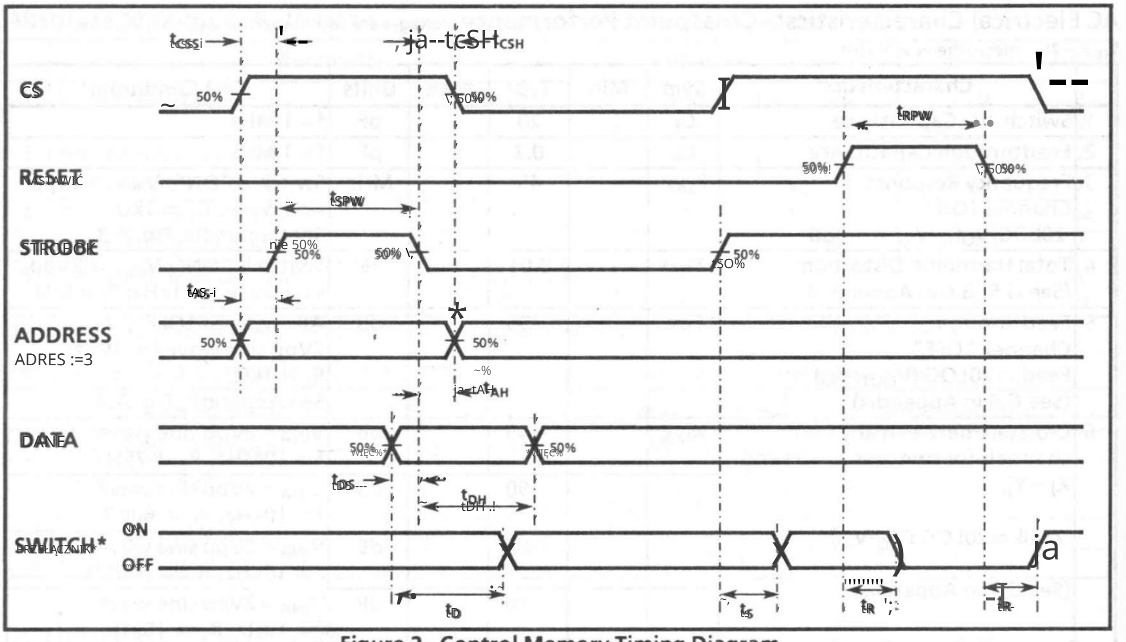

Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A-1 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection*
0	0	0	0	0	0	0	X0 Y0
1	0	0	0	0	0	0	X1 Y0
0	1	0	0	0	0	0	X2 Y0
1	1	0	0	0	0	0	X3 Y0
0	0	1	0	0	0	0	X4 Y0
1	0	1	0	0	0	0	X5 Y0
0	1	1	0	0	0	0	X12 Y0
1	1	1	0	0	0	0	X13 Y0
0	0	0	1	0	0	0	X6 Y0
1	0	0	1	0	0	0	X7 Y0
0	1	0	1	0	0	0	X8 Y0
1	1	0	1	0	0	0	X9 Y0
0	0	1	1	0	0	0	X10 Y0
1	0	1	1	0	0	0	X11 Y0
0	1	1	1	0	0	0	X14 Y0
1	1	1	1	0	0	0	X15 Y0
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0 Y1 ↓ X15 Y1
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0 Y2 ↓ X15 Y2
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0 Y3 ↓ X15 Y3
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0 Y4 ↓ X15 Y4
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0 Y5 ↓ X15 Y5
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0 Y6 ↓ X15 Y6
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0 Y7 ↓ X15 Y7

Figure 3 - Address Decode Truth Table

*Switch connections are not in ascending order

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Pin Description

Opis pin

Pin # * Bank#	Name Nazwa	Description Opis
1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array. Y3 Analogowe (wejście/wyjście) jest on połączony do orbity Y3 układu przełączników.
2	AY2	Y2 Address Line (Input). Wiersz adresu Y2 (wejście).
3	RESET	Master RESET (Input): this is used to turn off all switches regardless of the condition of CS. Active High. RESET Master RESET (wejście). Jest Active High. służy do wyłączania wszystkich przełączników niezależnie od stanu High.
4,5	AX3 AX0	X3 and X0 Address Lines (Inputs). 4,5 AX3, AX0 X3 i linie adresowe X0 (wejścia).
6,7	X14, X15	X14 and X15 Analog (Inputs/Outputs): these are connected to the X14 and X15 rows of the switch array. X14, X15 X14 i X15 Analogowe (wejście/wyjście) tablicy przełączników. są one połączone z wierszami X14 i X15
8-13	X6-X11	X6-X11 Analog (Inputs/Outputs): these are connected to the X6-X11 rows of the switch array. X6-X11 Analogowe (wejścia/wyjścia). są one połączone z wierszami X6-X11 tablica przełączników.
14	NC	No Connection Brak połączenia.
15	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array. Y7 Analog (wejście/wyjście). jest on połączony z kolumną Y7 tablicy przełączników.
16	VSS	Digital Ground Reference . Oryginalny są dla naziemny VSS .
17	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array. Y6 Analogowe (wejście/wyjście) jest on połączony do kolumny Y6 tablicy przełączników.
18	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High. STROBE STROBE (wejście). Włącza funkcję wybraną przez adres i dane. Adres musi być stabilny przed osiągnięciem przez STROBE wysokiego poziomu, a DATA musi być stabilny na opadającym zboczu strobo. światło elektryczne wysokie.
19	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array. Y5 Analog (wejście/wyjście). jest on połączony z jednostką czasową Y5 tablicy przełączników.
20	VEE	Negative Power Supply. Zasilanie ujemne .
21	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array. Y4 Analogowe (wejście/wyjście) jest on połączony do orbity Y4 układu przełączników.
22,23	AX1, AX2	X1 and X2 Address Lines (Inputs). 22,23 AX1, AX2 , X1 i X2 linie adresowe (wejścia).
24,25	AY0, AY1	Y0 and Y1 Address Lines (Inputs). 24,25 AY0, AY1 Y0 i Y1 Linie adresowe (wejścia).
26,27	X13, X12	X13 and X12 Analog (Inputs/Outputs): these are connected to the X13 and X12 rows of the switch array. X13, X12 X13 i X12 Analogowe (wejście/wyjście) tablicy przełączników. są one połączone z wierszami X13 i X12
28-33	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array. X5-X0 X5-X0 Analog (wejścia/wyjścia). są one połączone z wierszami X5-X0 tablica przełączników.
34	NC	No Connection. NC Brak połączenia.
35	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array. Y0 Y0 Analogowe (wejście/wyjście). jest on połączony z ramką Y0 tablicy przełączników.
36	CS	Chip Select (Input): this is used to select the device. Active High. Wybór układu (wejście). służy do wybierania urządzenia. Active High.
37	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array. Y1 Analogowe (wejście/wyjście) jest to powiązane z kolumną Y1 tablicy przełączników.
38	DATA	DATA (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High. DANE DANE (wejście). wejście logicznego wysokiej wartości spowoduje włączenie wybranego przełącznika, a prawo logiczne spowoduje wyłącz wybrany przełącznik. Active High.
39	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array. Y2 Analogowe (wejście/wyjście) jest on połączony z orbitą Y2 tablicy przełączników.
40	VDD	Positive Power Supply. Zasilanie VDD dodatnie .

* Plastic DIP and CERDIP only
Tylko plastikowe DIP i CERDIP

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Functional Description

The MT8816 is an analog switch matrix with an array size of 8×16. The switch array is arranged such that there are 8 columns by 16 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on, and provide a high degree of isolation when turned off. The control memory consists of a 128 bit write only RAM in which the bits are selected by the address inputs (AX0-AX2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be used to configure by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8816 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

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MT8806/08/09/12/14/15/16 ANALOG SWITCH ARRAY FAMILY:
MT8806/08/09/12/14/15/16 RODZINA ANALOGOWYCH PRZEŁĄCZALNYCH MACIERZY:

TEST CIRCUITS FOR KEY PARAMETER MEASUREMENTS
OBWODY TESTOWE DO POMIARÓW KLUCZOWYCH PARAMETRÓW

A.1 Off-State Leakage Current (I_{OFF}) Measurement
Pomiar prądu upływu w stanie wyłączonym (I_{OFF})

A.2 R_{ON}, ΔR_{ON} vs V_{DC} Measurements
A.2 Pomiary R_{ON}, ΔR_{ON} w porównaniu z V_{DC}

A.3 Frequency Response (F_{req}) Measurement
A.3 Pomiar częstotliwości (częstotliwości)

A.4 Feedthrough (FDT) Measurement
A.4 Pomiar przepustu (FDT)

A.5 Crosstalk (X_{talk}) Measurement
Pomiar przesłuchu (X_{talk})

A.6 Control Input Crosstalk (CX_{talk}) Measurement
A.6 Pomiar przesłuchu wejściowego (CX_{talk})

A.7 Control Memory Timing Measurements
A.7 Pomiary czasu pamięci sterującej

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Appendix: Analog Switch Array Measurements

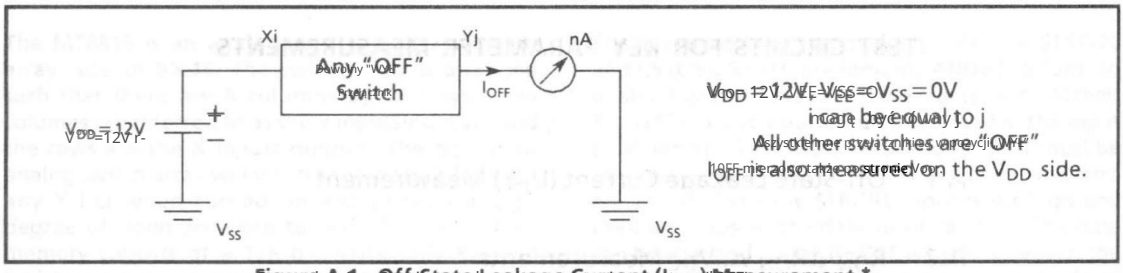

Figure A.1 – Off State Leakage Current (I_{OFF}) Measurement *

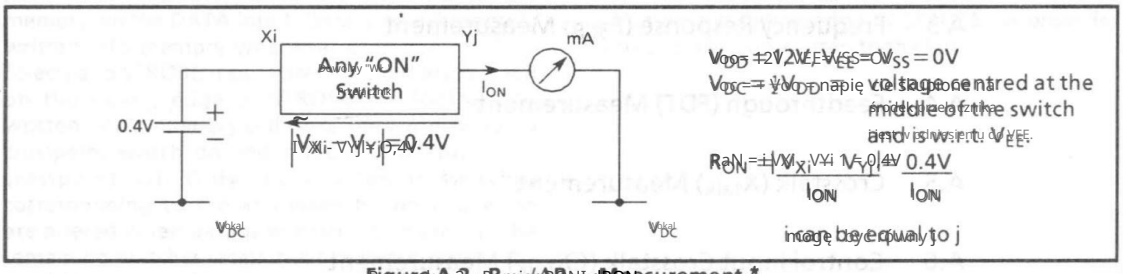

Figure A.2 – R_{ON} / ΔR_{ON} Measurement *

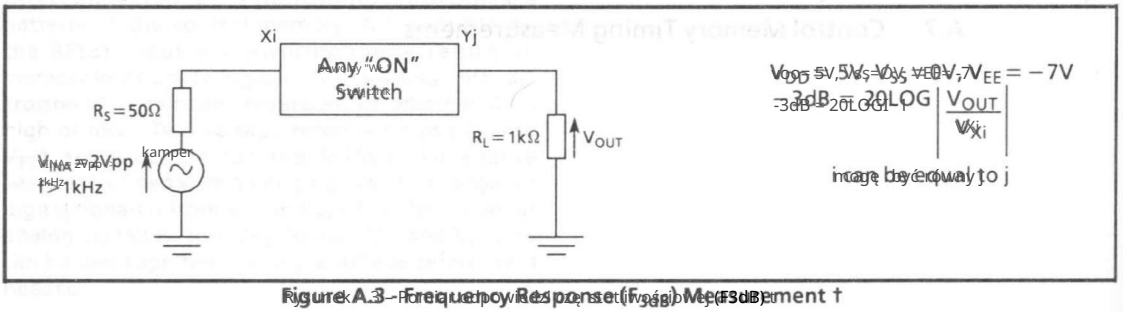

Figure A.3 – Frequency Response (Frequency Bandwidth) Measurement †

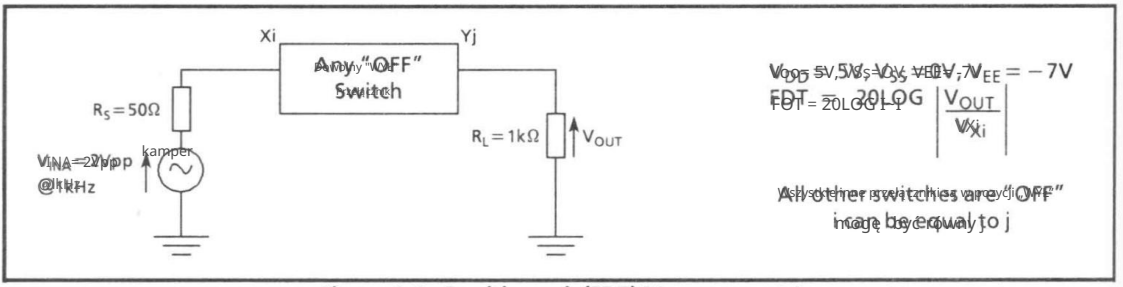

Figure A.4 – Feedthrough (FDT) Measurement †

Notes:

*Test Conditions for MT8809 and MT8812 are respectively: V_{DD} = +12V, V_{SS} = 0V and V_{DD} = 14V, V_{SS} = 0V.
Test Conditions for MT8809 and MT8812 are respectively: V_{DD} = +5V, V_{DC} = 0V, V_{SS} = −7V and V_{DD} = 5V, V_{DC} = 0V, V_{SS} = −7 V.
Any X and Y analog I/Os can be interchanged for all measurements.

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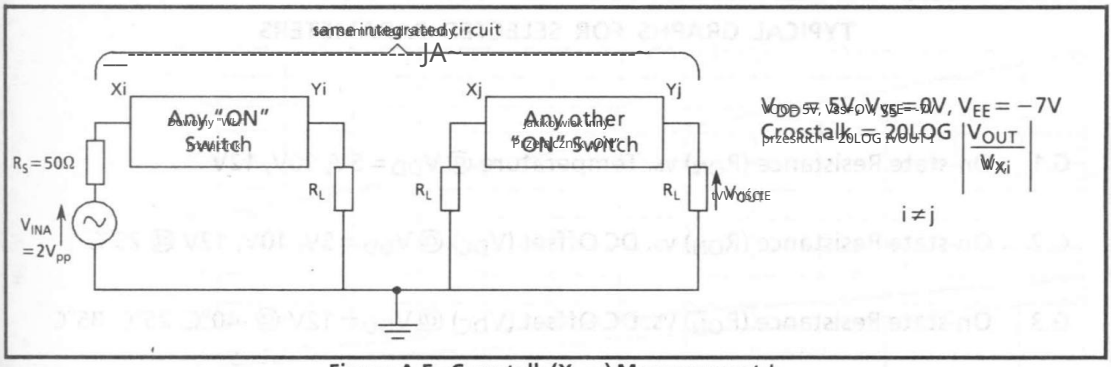

Figure A.5 - Crosstalk (X_{talk}) Measurement †

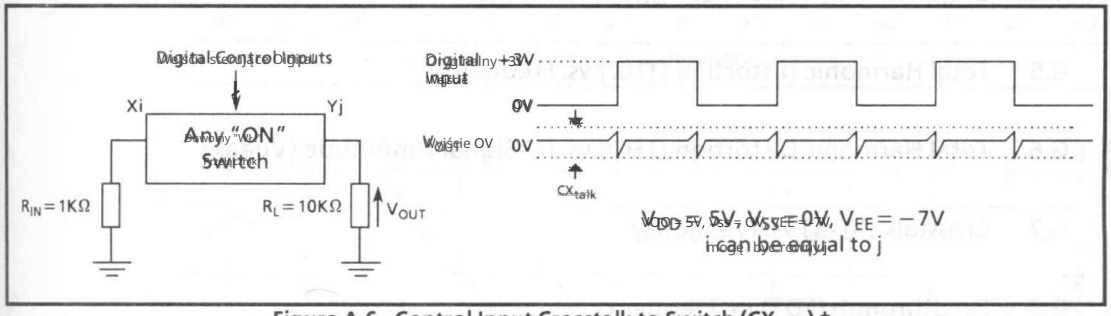

Figure A.6 - Control Input Crosstalk to Switch (CX_{talk}) †

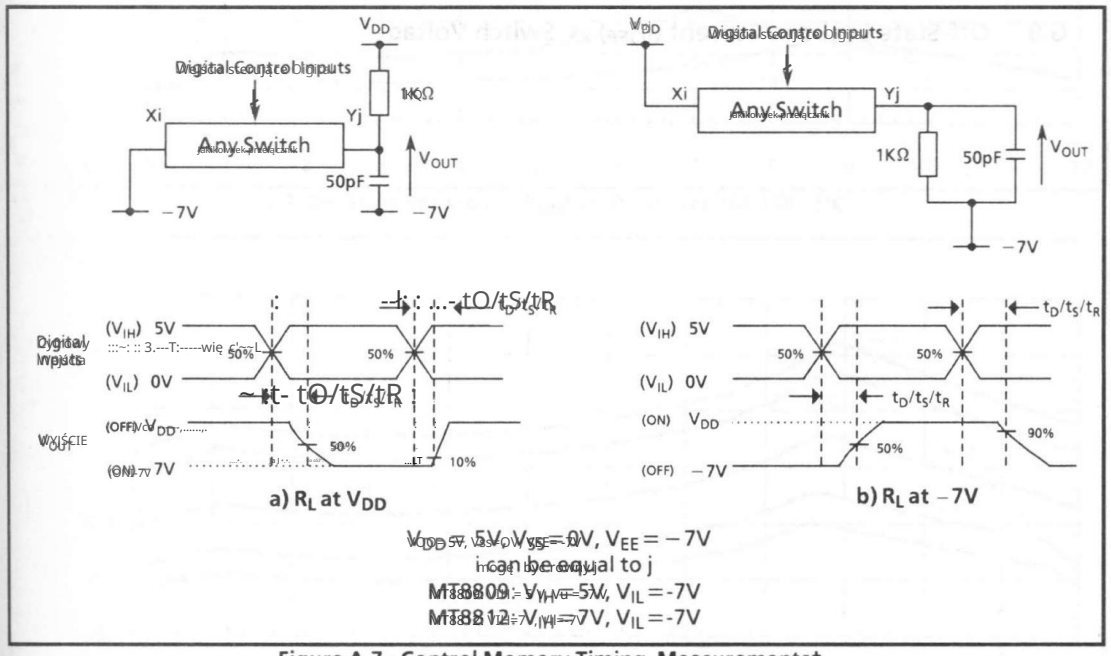

Figure A.7 - Control Memory Timing Measurements†

Notes:

† Test Conditions for MT8809 and MT8812 are respectively V_{DD} = 5V, V_{SS} = -7V, V_{EE} = 0V, V_{IH} = 5V, V_{IL} = -7V and V_{DD} = 7V, V_{SS} = -7V, V_{EE} = 0V, V_{DC} = 0V, V_{SS} = −7 V.

All analog inputs and outputs can be interchanged for bi-directional switches.

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MT8806/08/09/12/14/15/16 ANALOG SWITCH ARRAY FAMILY:

TYPICAL GRAPHS FOR SELECTED PARAMETERS

G.1 On-state Resistance (R_{ON}) vs. Temperature @ V_{DD} = 5V, 10V, 12V

G.1 Rezystancja w stanie włączonym (R_{ON}) w zależności od temperatury przy V_{DD} = 5 V, 10 V, 12 V

G.2 On-state Resistance (R_{ON}) vs. DC Offset (V_{DC}) @ V_{DD} = 5V, 10V, 12V @ 25°C

G.2 Rezystancja w stanie włączonym (R_{ON}) w stosunku do offsetu DC (V_{DD} @ V_{DD} = 5 V, 10 V, 12 V @ 25°C)

G.3 On-state Resistance (R_{ON}) vs. DC Offset (V_{DC}) @ V_{DD} = 12V @ -40°C, 25°C, 85°C

G.3 Rezystancja w stanie włączonym (R_{ON}) w stosunku do offsetu DC (V_{DD} @ V_{DD} = 12 V @ -40°C, 25°C, 85°C

G.4 ΔR_{ON} vs. Temperature @ V_{DD} = 5V, 10V, 12V

G.4 R_{ON} vs. Temperatura @ V_{DD} = 5 V

G.5 Total Harmonic Distortion (THD) vs. Frequency

G.5 Całkowite zniekształcenia harmoniczne (THD) w stosunku do częstotliwości

G.6 Total Harmonic Distortion (THD) vs. I/P Signal Amplitude (Vpeak)

G.6 Całkowite zniekształcenia harmoniczne (THD) w funkcji amplitudy sygnału wejściowego (Vpeak)

G.7 Crosstalk (X_{TALK}) vs. Frequency

Przesłuch G.7 (Xtalk) kontra częstotliwość)

G.8 Feedthrough (FDT) vs. Frequency

G.8 Przepustowość (FDT) w porównaniu z częstotliwością

G.9 Off-State Leakage Current (I_{OFF}) vs. Switch Voltage

G.9 Prąd upływu w stanie wyłączonym (I_{OFF}) w stosunku do napięcia przełącznika

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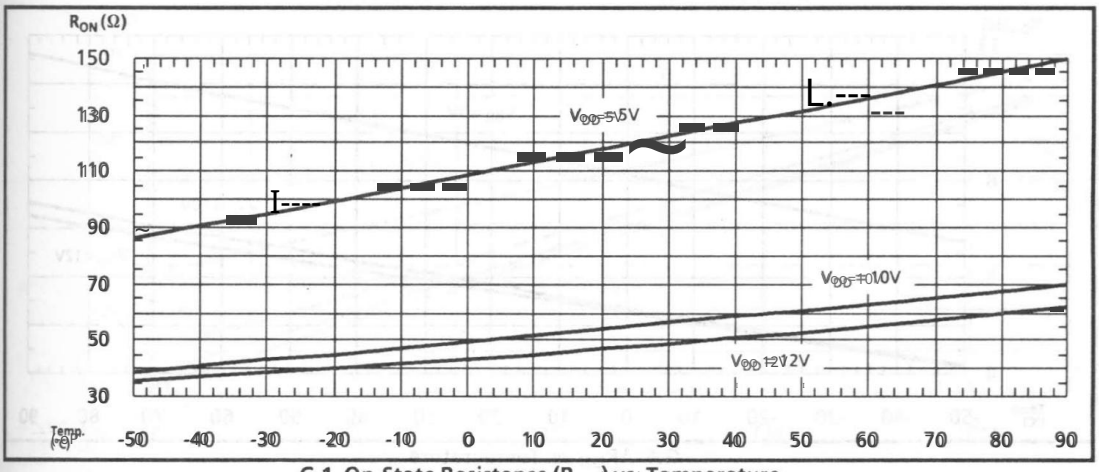
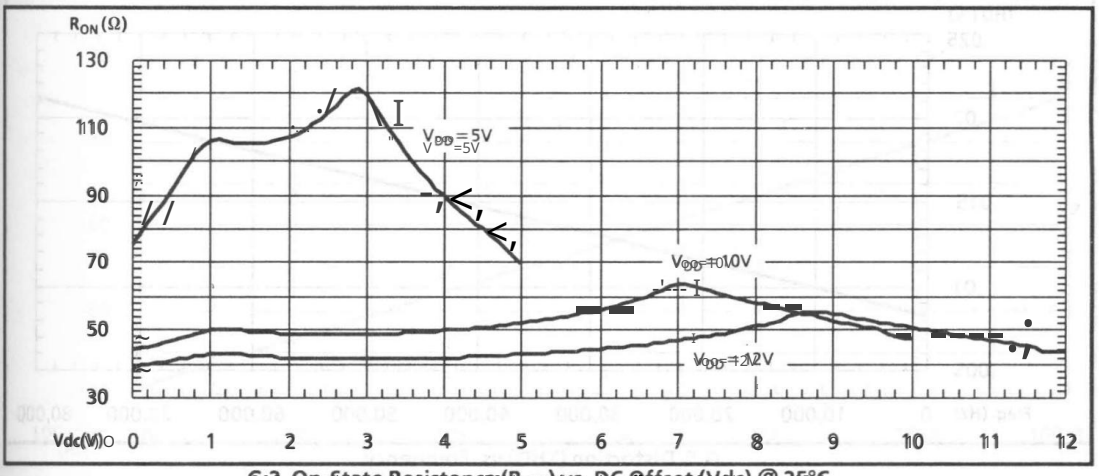
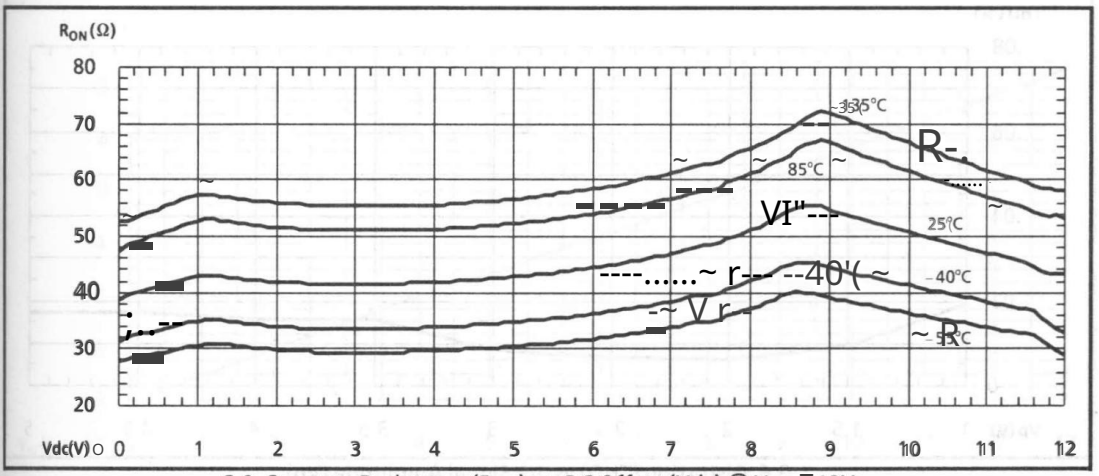


G1 On-State Resistance (R_{ON}) vs. Temperature



G2 On-State Resistance (R_{ON}) vs. DC Offset (Vdc) @ 25°C



G3 On-state Resistance (R_{ON}) vs. DC Offset (Vdc) @ V_{DD} = 12V

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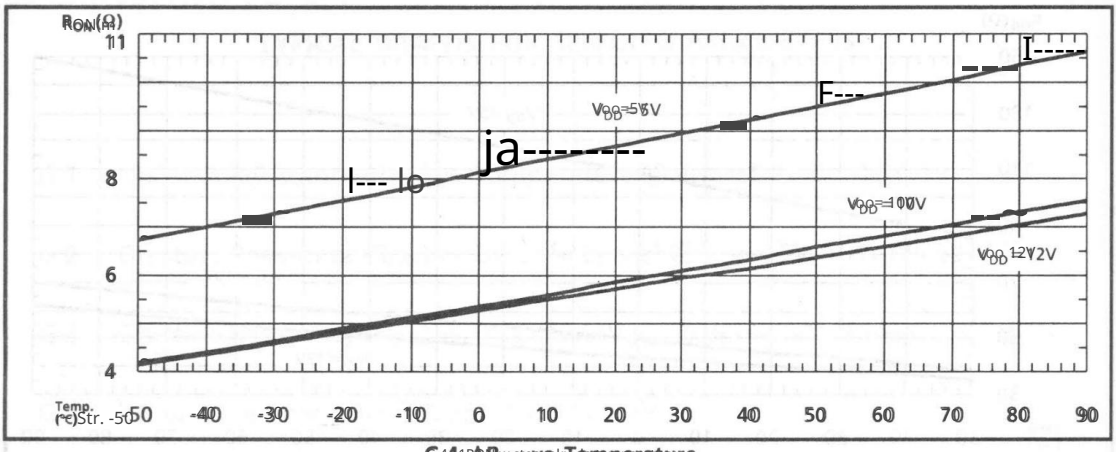
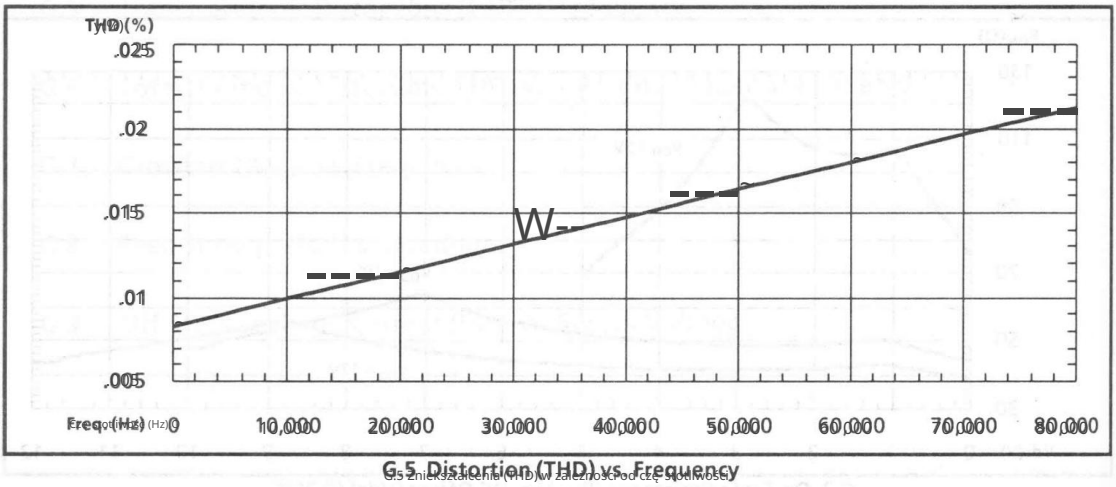
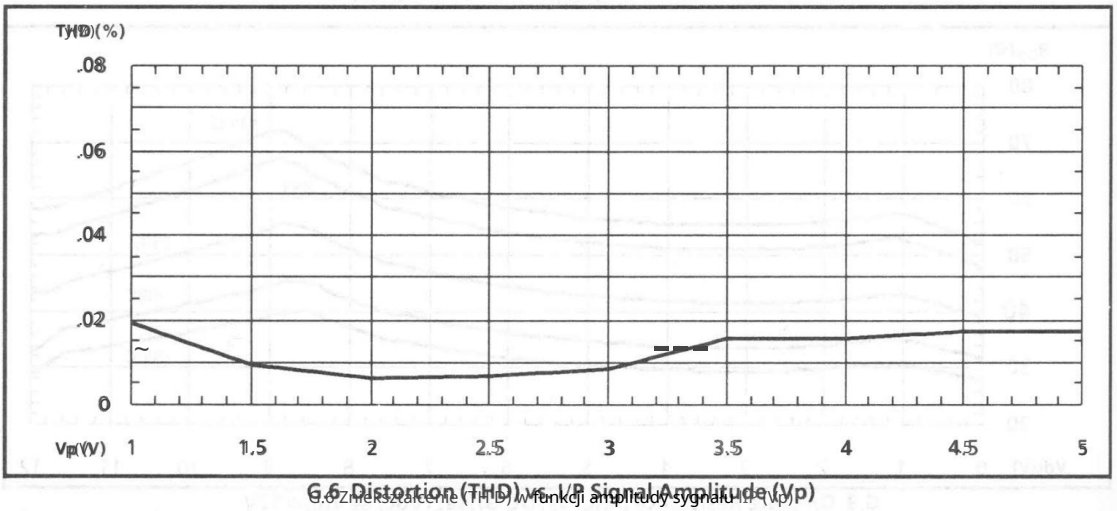


G4 RON vs. Temperature



G5 Distortion (THD) vs. Frequency



G6 Distortion (THD) vs. I/P Signal Amplitude (VP)

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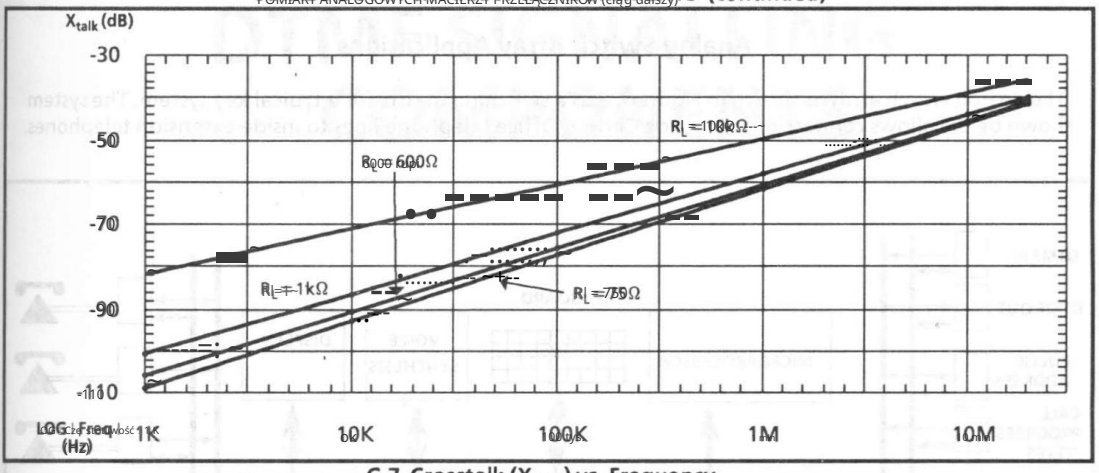
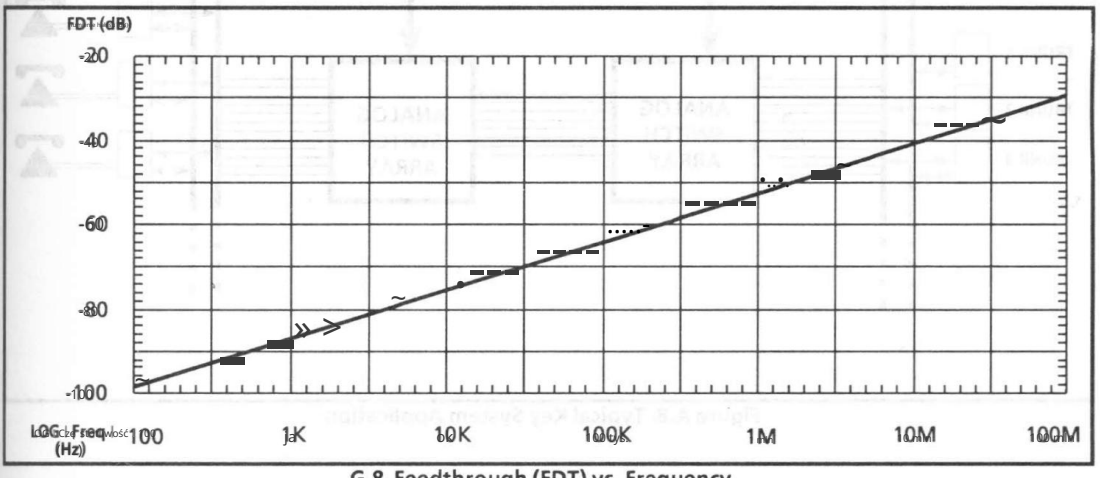
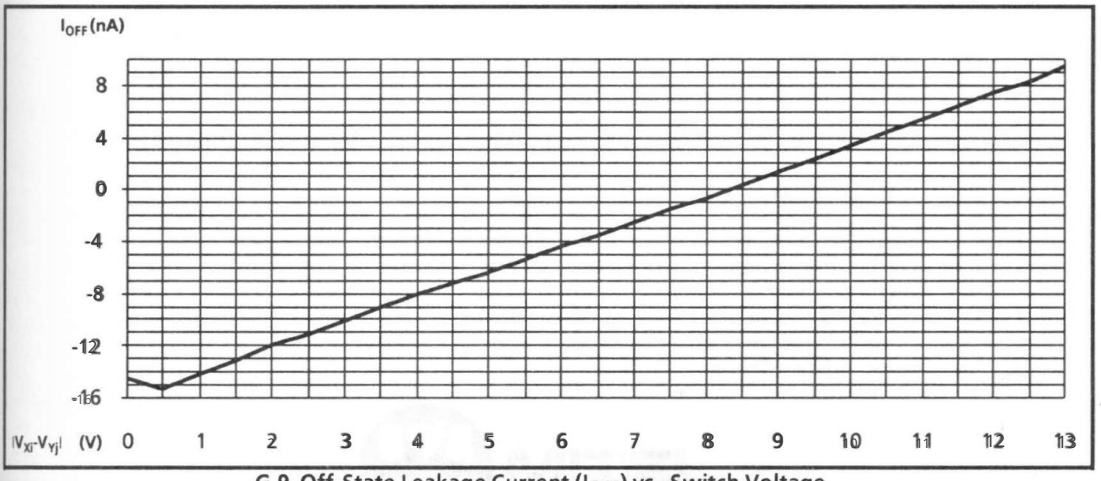
ANALOG SWITCH ARRAY MEASUREMENTS (continued)
POMIARY ANALOGOWYCH MACIERZY PRZEŁĄCZNIKÓW (ciąg dalszy)



G.7 Crosstalk (X_{talk}) vs. Frequency
Przesłuch G.7 (X_{talk}) w porównaniu z częstotliwością



G.8 Feedthrough (FDT) vs. Frequency
Przepustowość G.8 (FDT) w porównaniu z częstotliwością



G.9 Off State Leakage Current (I_{OFF}) vs. Switch Voltage
G.9 Prąd upływu w stanie wyłączonym (I_{OFF}) w zależności od napięcia przełączania

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Analog Switch Array Applications

The analog switch array is shown in Figure A.8 as a switching matrix for a typical key system. The system shown below allows connection of outside Central Office telephone lines to inside extension telephones.

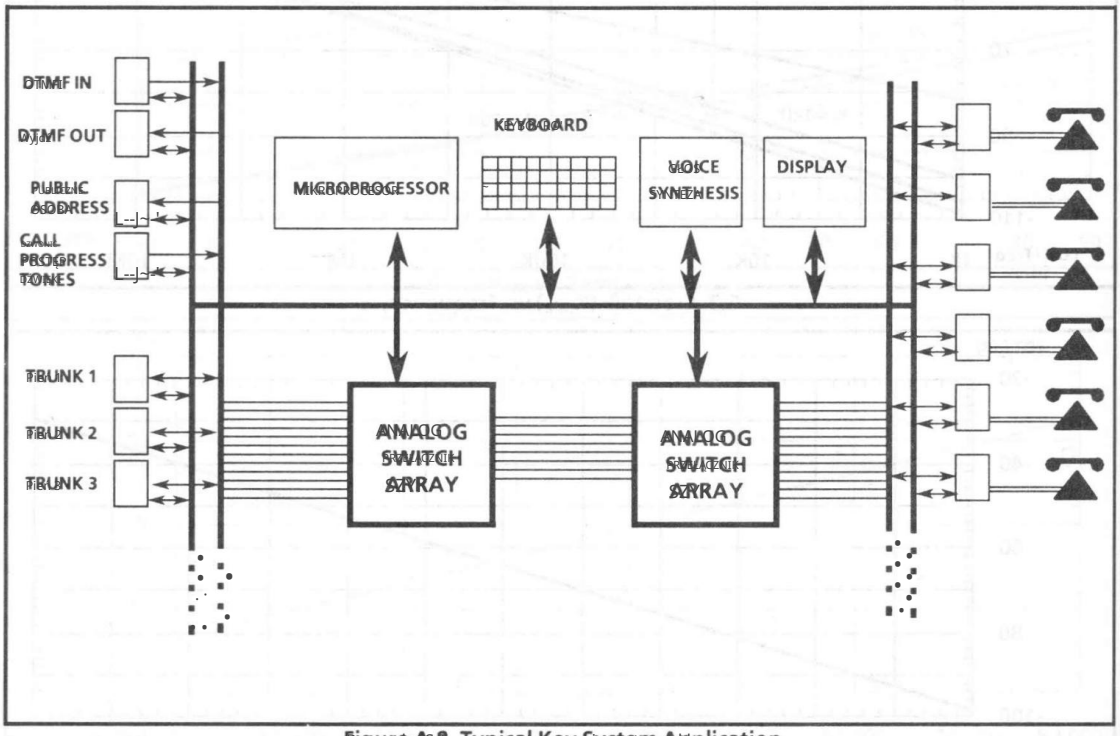

Figure A.8 Typical Key System Application

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DTMF SIGNALING COMPONENTS

SYGNALIZACJA DTMF

SKŁADNIKI

3

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ISSUE 3 September 1989

Features

Cechy

- Provides complete receiver evaluation in less than 60 minutes testing time.

  Zapewnia kompletną ocenę odbiornika trwającą poniżej 60 minut.

- Utilizes a condensed speech recording equivalent to many hours of receiver exposure via electronic talk-off rate.

  Wykorzystuje skondensowany zapis mowy równoważny wielu godzinom odbioru przy użyciu elektronicznego współczynnika talk-off.

- Checks receiver recognition bandwidths, center frequencies, maximum acceptable amplitude ratio, guard time, dynamic range, and acceptable signal to noise ratio.

  Sprawdza szerokości pasm rozpoznawania, częstotliwości środkowe, maksymalny dopuszczalny stosunek amplitud, czas ochrony, zakres dynamiki oraz dopuszczalny stosunek sygnału do szumu.

- Test equipment requirement consists of a digital counter, an ac voltmeter, and low cost cassette tape player. The tape player may require a small amplifier to achieve 2 V_{RMS} depending upon the receiver to be tested.

  Wymagania dotyczące sprzętu testowego: cyfrowy licznik, woltomierz prądu przemiennego i niedrogi odtwarzacz kaset. Odtwarzacz kasetowy może wymagać małego wzmacniacza w celu uzyskania 2 V_{RMS} w zależności od testowanego odbiornika.

- Compensation factors allow tape player speed inaccuracies of up to 2% without loss of measurement accuracy.

  Współczynniki kompensacji pozwalają na większe niedokładności prędkości taśmowego do 2% bez utraty dokładności pomiaru.

- Convenient C60 cassette format on low noise high bias chrome tape, recorded using Dolby B noise reduction.

  Wygodny format kasety C60 na taśmie chromowej o niskim poziomie szumów i wysokiej podatności, nagrywanej przy użyciu redukcji szumów Dolby B.

General Description

Ogólny opis

The Mitel CM7291 Tone Receiver Test Cassette cuts the total evaluation time of DTMF tone receivers to less than 60 minutes. Test equipment requirements are also minimized to a modest test setup.

Kaseta testowa CM7291 Tone Receiver Test Cassette skraca całkowity czas oceny odbiorników DTMF do mniej niż 60 minut. Wymagania dotyczące sprzętu testowego są również zminimalizowane do prostej konfiguracji testowej.

Test Content

Zawartość testu

Side one of the tape contains a series of tests involving recorded tone bursts with the parameters varied in a number of ways. Tests are performed by sending the tone bursts to the receiver and counting the number of bursts to which the receiver responds. The results from these tests provide direct indications of receiver performance.

Strona pierwsza taśmy zawiera serię testów dotyczących nagranych serii tonowych o zmienionych parametrach. Testy wykonywane są poprzez wysyłanie serii tonów do odbiornika i zliczanie liczby serii, na które odbiornik odpowiada. Wyniki tych testów dostarczają bezpośrednich wskazówek dotyczących wydajności odbiornika.

Side two of the tape contains a condensed speech recording which is used to evaluate the speech immunity of the receiver. Ideally a receiver's response to the speech recording should be zero, since no intentional tone bursts are present. In practice a small number of responses will vary from 2 to 100 depending on the receiver quality and dynamic range.

Strona druga taśmy zawiera skondensowany zapis mowy, który służy do oceny odporności odbiornika na mowę. Idealnie, w przypadku braku celowych serii tonowych, odpowiedź odbiornika na zapis mowy powinna wynosić zero. W praktyce niewielka liczba odpowiedzi będzie się wahać od 2 do 100 w zależności od jakości odbiornika i zakresu dynamiki.

Prompts and instructions are included on both sides of the tape to aid in receiver testing.

Po obu stronach taśmy znajdują się wskazówki i instrukcje ułatwiające testowanie odbiornika.

Test Setup

Konfiguracja testu

Two test setups using the same test equipment are used. The first, shown in Fig. 1, is used to perform a 1 kHz calibration test. The second, shown in Fig. 2, is used for the receiver dynamic tests.

Używane są dwa zestawy testowe z tym samym wyposażeniem testowym. Pierwszy, pokazany na rys. 1, służy do wykonywania testu kalibracji 1 kHz. Drugi, pokazany na rys. 2, służy do testów dynamiki odbiornika.

Calibration Test. The first test on both sides of the tape is a 1 kHz calibration test and is used to provide a correction factor for the playback inaccuracy of the tape player.

Test kalibracyjny. Pierwszy test na obu stronach taśmy jest testem kalibracji 1 kHz i służy do dostarczenia współczynnika korekcji niedokładności odtwarzania magnetofonu kasetowego.

Receiver Test. Once the calibration test has been performed the test setup is changed to that shown in Fig. 2 and remains the same that way for all other tests.

Test odbiornika. Po zakończeniu testu kalibracji wykonywana jest konfiguracja testowa pokazana na rysunku 2, która pozostaje taka sama dla wszystkich pozostałych testów.

Receiver Testing

Testowanie odbiornika

The following describes the recorded contents of both sides of the tape, and the tests provided.

Poniżej przedstawiono zawartość nagrania po obu stronach taśmy oraz przeprowadzone testy.

The 1 kHz reference signal level output from the cassette player which is adjusted to 2.0 V_{RMS} (5.656 V_{p-p}) is required for tone receiver systems capable of handling this level (i.e. this level won't cause internal clipping of the signal). All levels referred to in this document are referenced to the initial 2.0 V_{RMS} level setting.

Poziom sygnału odniesienia 1 kHz z odtwarzacza kasetowego, który jest wyregulowany do 2,0 V_{RMS} (5,656 V_{p-p}), jest wymagany dla systemów odbiorników tonowych zdolnych do obsługi tego poziomu (tj. ten poziom nie powoduje wewnętrznego ograniczania sygnału). Wszystkie poziomy odniesione w tym dokumencie odnoszą się do początkowego ustawienia poziomu 2,0 V_{RMS}.

Note: To use the CM7291 with tone receivers operating from a single 5 V supply, the 1 kHz reference signal output level of the cassette player must be reduced. For example, if using the MT8870 tone receiver, the 1 kHz reference signal level would be adjusted such that the signal observed at the device's G_S pin would be a maximum without clipping. This level would be 1.738 V_{RMS} (i.e. 4.91 V_{p-p}). Accordingly, the levels referred to in the test descriptions must be reduced proportionally. For example, each dual tone frequency at a 1.0 V_{RMS} level would now be 869 mV_{RMS} (+1 dBm) and 35 dB down from this level would be 20 mV_{RMS} (-34 dBm). A 200 mV_{RMS} level per frequency would now be 174 mV_{RMS} (-13 dBm).

Uwaga: Aby użyć CM7291 z tonowymi odbiornikami zasilanymi jednym zasilaczem 5 V, poziom sygnału odniesienia 1 kHz odtwarzacza kasetowego musi zostać zmniejszony. Na przykład, jeśli używany jest odbiornik tonowy MT8870, poziom sygnału odniesienia 1 kHz zostałby dostosowany tak, aby sygnał obserwowany na wyprowadzeniu G_S urządzenia był maksymalny bez obcinania. Ten poziom wynosiłby 1,738 V_{RMS} (tj. 4,91 V_{p-p}). Zgodnie z tym poziomy odniesione w opisach testów należy proporcjonalnie zmniejszyć. Na przykład każda częstotliwość dwutonowa przy poziomie 1,0 V_{RMS} wynosiłaby teraz 869 mV_{RMS} (+1 dBm), a poziom 35 dB niższy od tego poziomu wynosiłby 20 mV_{RMS} (-34 dBm). Poziom 200 mV_{RMS} na częstotliwość wynosiłby teraz 174 mV_{RMS} (-13 dBm).

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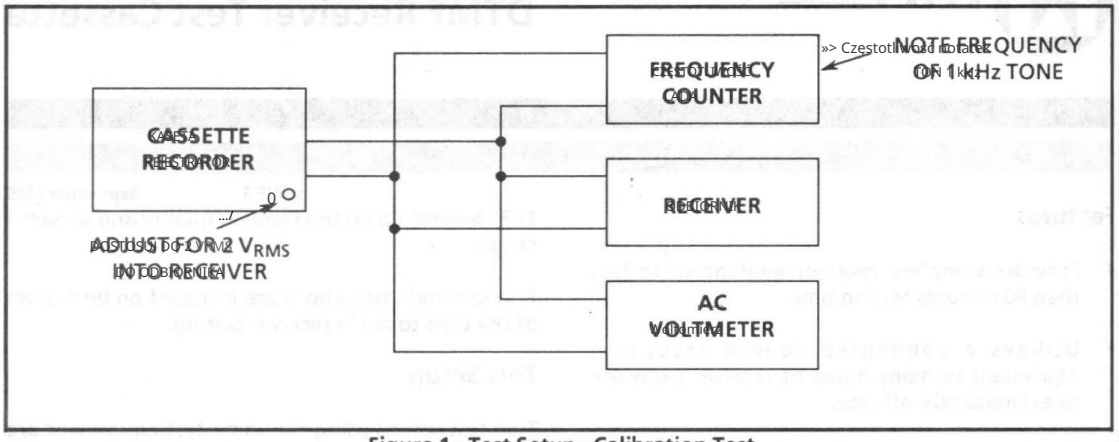

Figure 1. Test Setup - Calibration Test

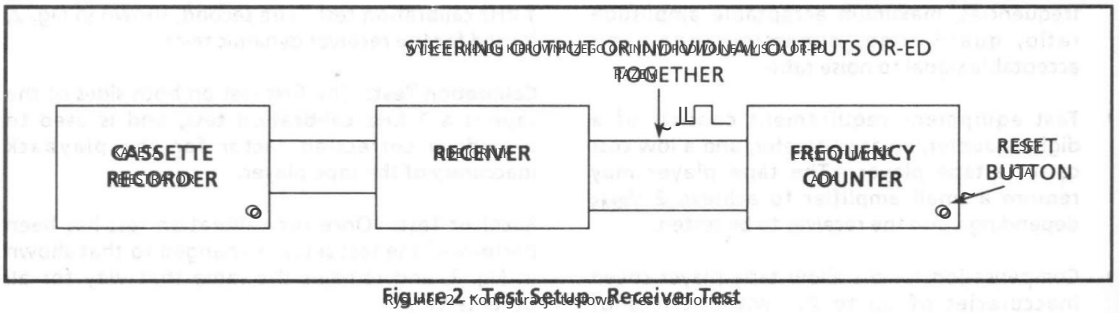

Figure 2. Test Setup - Receiver Test

SIDE 1 - TEST 1

Calibration Tone: Consists of a continuous 1 kHz tone, present for one minute. Used to provide a correction factor for tape playback speed inaccuracy using equation 1. The correction is employed when checking receiver channel center frequencies in test 3.

$$X(\%) = (1000/f_0 - 1000)/10 \quad \text{....Eqn. 1}$$

Frequency f_0 is measured as follows using the test setup shown in Fig. 1.

- Set the level of tone at the receiver input to 2 V_{RMS}. This setting must not be altered for the duration of the tests on side 1.
- Measure the frequency of the tone f_0 at the receiver input.

SIDE 1 - TEST 2

Decode Check: All tone pairs associated with standard 4 x 4 keypad digits (i.e. L1 H1 through L4 H4) are pulsed sequentially using 50 ms bursts at 1 V_{RMS} per frequency. Each tone pair is pulsed 10 times consecutively. The receiver should respond to all tone pairs it is designed to receive.

SIDE 1 - TEST 3

Recognition Bandwidth and Channel Center Frequency Check

This test utilizes the tone pairs L1, L2, L3, L2 H2, L3 H3, and L4 H4 (i.e. digits 1, 5, 9 and 16). Each tone pair requires four tests to complete the check, making 16 sections overall. Each section contains 40 pulses of 50 ms duration with an amplitude of 2 V_{RMS} per frequency.

Four sections covering the tests for one tone pair (1 digit) are:

(a) H frequency at 0% deviation from center, L frequency at +0.1%. L frequency is then incremented in 0.1% steps, up to +4%. The number of tone bursts is noted and designated N+.

(b) H frequency at 0% deviation, L frequency at -0.1%. L frequency is then decremented in -0.1% steps, up to -4%. The number of tone bursts is noted and designated N−.

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(c) The test in (a) is repeated with the L frequency at 0% and the H frequency varied up to +4%.

(d) The test in (b) is repeated with the L frequency at 0% and the H frequency varied up to -4%.

Receiver Recognition Bandwidth (RRB) is calculated as follows:

$$RRB\% = (N_+ + N_-)/10 \quad \text{....Eqn 2}$$

Receiver Center Frequency Offset (RCFO) is calculated as follows:

$$RCFO\% = (N_+ - N_-)/20 \quad \text{....Eqn 3}$$

SIDE 1 - TEST 4

Acceptable Amplitude Ratio (Twist)

This test utilizes tone pairs L1-H1, L2-H2, L3-H3, and L4-H4 (i.e. digits 1, 9, and 16). There are eight sections in this test, each section containing 200 pulses with a 50 ms duration for each pulse. Initially the amplitude of both tones is 1 V_{RMS}.

Two sections test one tone pair are:

(a) *Standard Twist*: H tone amplitude is maintained at 1 V_{RMS}, amplitude of L tone is attenuated gradually until the amplitude ratio is 20 dB. Note the number of responses from the receiver.

(b) *Reverse Twist*: L tone amplitude is maintained at 1 V_{RMS}, H tone amplitude is attenuated gradually until the amplitude ratio is 20 dB. Note the number of responses from the receiver.

The Acceptable Amplitude Ratio in dB for this test is equal to the number of responses registered in (a) or (b), divided by 10.

SIDE 1 - TEST 5

Dynamic Range

This test utilizes tone pair L1-H1 (digit 1). Thirty-five tone pairs (pulses) are transmitted, with both frequencies starting at 1 V_{RMS}. The amplitude of each is gradually attenuated to 1.35 dB at a rate of 1 dB per pulse. The Dynamic Range in dB is equal to the number of responses from the receiver during the test.

SIDE 1 - TEST 6

Guard Time

This test utilizes tone pair L1-H1 (digit 1). Four hundred pulses are transmitted at an amplitude of 1 V_{RMS} per frequency. Pulse duration starts at 40 ms and is gradually reduced to 10 ms. Guard time in ms is equal to (500 − number of responses) /10.

SIDE 1 - TEST 7

Acceptable Signal to Noise Ratio

This test utilizes tone pair L1-H1 transmitted on a noise background. The test consists of three sections in which the tone pair is transmitted 1000 times at an amplitude of 1 V_{RMS} per frequency, but with a different white noise level for each section. The first level is -24 dBV, the second -18 dBV, and the third -12 dBV. The Acceptable Signal to Noise Ratio is the lowest ratio of signal to noise in the test where the receiver responds to all 1000 pulses.

SIDE 2 - TEST 1

Calibration Tone

A repetition of Test 1, Side 1, at which time the signal level at the receiver input must be recalibrated to 2.0 V_{RMS}. This adjustment is entirely independent of the setting made at Test 1 - Side 1.

SIDE 2 - TEST 2

Talk-Off Test

This test consists of recordings of conversations on telephone trunks. Samples are taken over a long period of time and condensed into a 30 minute period. Receiver immunity to talk-off is determined by the number of responses occurring during this test. A receiver with an acceptable talk-off response should register less than 30.

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Summary of Cassette Content

The following table lists the contents of the cassette together with the playing time from the start of the tape. It is recommended that the tape counter reading for each test be recorded in the column provided. This will provide the most convenient method of test location.

TEST	DESCRIPTION			COUNTER	TIME Minutes: Seconds
Introduction					0
Side 1, 1	1 kHz at 2 V$_{RMS}$				0:20
Side 1, 2	Decode test digits 1 to 16 (10 pulses each)				2:00
Side 1, 3	Recognition bandwidth and centre frequency check (40 pulses each)				3:10
Side 1, 3a	Digit 1	697Hz	+0.1 to +4%		4:10
Side 1, 3b	Digit 1	697Hz	−0.1 to −4%		
Side 1, 3c	Digit 1	1209Hz	+0.1 to +4%		
Side 1, 3d	Digit 1	1209Hz	−0.1 to −4%		
Side 1, 3e	Digit 5	770Hz	+0.1 to +4%		
Side 1, 3f	Digit 5	770Hz	−0.1 to −4%		
Side 1, 3g	Digit 1	1336Hz	+0.1 to +4%		
Side 1, 3h	Digit 5	1336Hz	−0.1 to −4%		
Side 1, 3i	Digit 9	852Hz	+0.1 to +4%		
Side 1, 3j	Digit 9	852Hz	−0.1 to −4%		
Side 1, 3k	Digit 9	1477Hz	+0.1 to +4%		
Side 1, 3l	Digit 9	1477Hz	−0.1 to −4%		
Side 1, 3m	Digit 16	941Hz	+0.1 to +4%		
Side 1, 3n	Digit 16	941Hz	−0.1 to −4%		
Side 1, 3o	Digit 16	1633Hz	+0.1 to +4%		
Side 1, 3p	Digit 16	1633Hz	−0.1 to −4%		
Side 1, 4	Amplitude ratio (200 pluses each)				12:45
Side 1, 4a	Digit 1	L1/H1	0 to 20 dB		
Side 1, 4b	Digit 1	L1/H1	0 to 20 dB		
Side 1, 4c	Digit 5	L2/H2	0 to 20 dB		
Side 1, 4d	Digit 5	L2/H2	0 to 20 dB		
Side 1, 4e	Digit 9	L3/H3	0 to 20 dB		
Side 1, 4f	Digit 9	L3/H3	0 to 20 dB		
Side 1, 4g	Digit 16	L4/H4	0 to 20 dB		
Side 1, 4h	Digit 16	L4/H4	0 to 20 dB		
Side 1, 5	Dynamic Range (35 pulses) Digit 1	1 to −35 dBV/freq			19:20
Side 1, 6	Guard Time (400 pulses) Digit 1	49 to 10 ms			20:10
Side 1, 7	Signal to Noise (1000 pulses each)				21:50
Side 1, 7a	Digit 1	S/N	24 dB/freq		22:25
Side 1, 7b	Digit 1	S/N	18 dB/freq		24:15
Side 1, 7c	Digit 1	S/N	18 dB/freq		26:05
Side 2	Introduction				0
Side 2, 1	1 kHz at 2 V$_{RMS}$				0:30
Side 2, 2	Talk-off Test (Speech)				2:00

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Features

- 45 dB dynamic range
- Simultaneous DTMF and supervisory tone detection (MT3270/MT3271)
- 4-bit binary serial data output
- For use with microprocessor controlled guard time (MT3270/MT3274)
- Internal guard time circuitry (MT3271/MT3275)

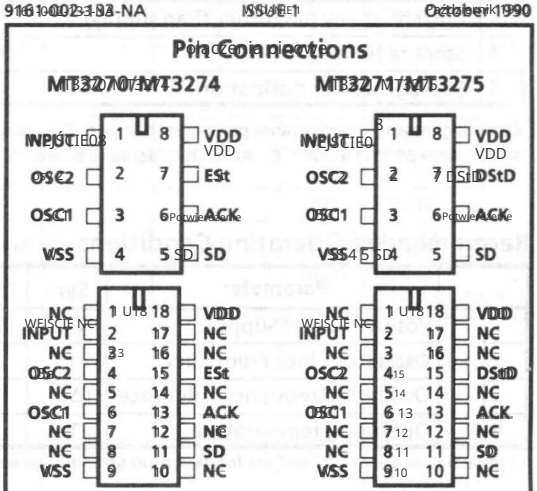
Applications

- Integrated telephone answering machine
- End-to-end signalling

Description

The MT3270/MT3271/MT3274/MT3275 is a high performance DTMF Receiver which decodes all 16 DTMF tone pairs into a 4-bit binary code. The device incorporates an AGC for wide dynamic range which is suitable for end-to-end signalling. The MT3270/MT3271 also indicates the presence of all supervisory tones using internal detection circuitry. The MT3274/MT3275 does not detect the presence of supervisory tones. The MT3270/MT3274 is useful in applications where DTMF validation period is determined by external control. The MT3271/MT3275 uses internal counters to provide a preset DTMF validation period. The MT3270/MT3271/MT3274/MT3275 uses a crystal or a ceramic resonator to complete the oscillator circuit.

Pin Connections



Ordering Information

0°C to +70°C

MT3270/71/74/75AE	8 pin Plastic DIP
MT3270/71/74/75AS	18 pin SOIC

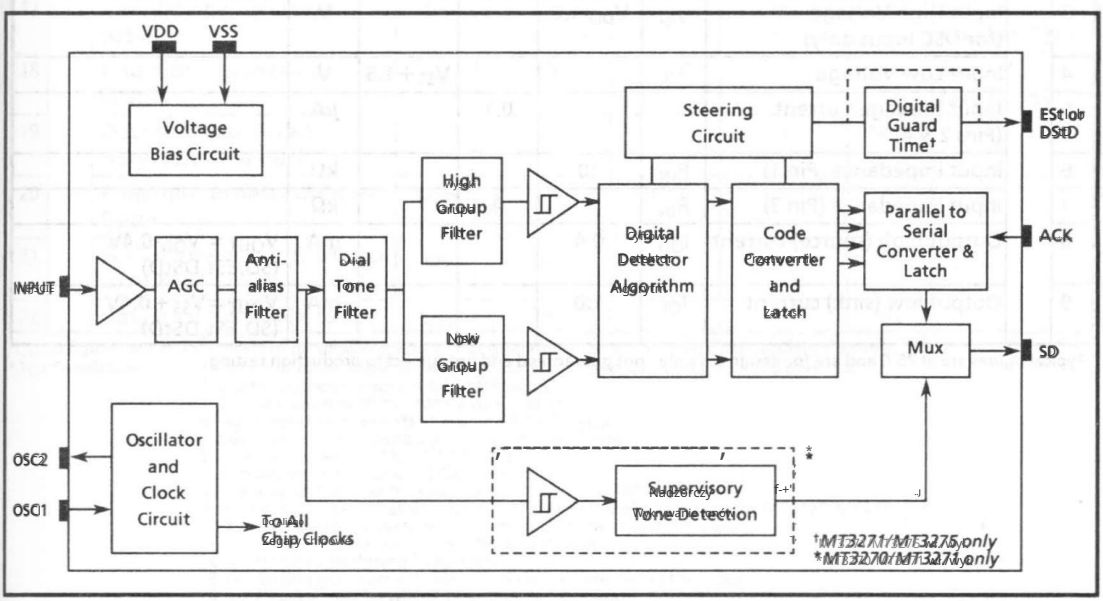


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	$V_{DD}-V_{SS}$		6	V
2	Voltage on any pin (other than supply)	$V_{I/O}$	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current at any pin (other than supply)	$I_{I/O}$		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Derate above 85°C at 9mW/°C. All leads soldered to board.

Recommended Operating Conditions

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive Power Supply	V_{DD}	4.75	5.0	5.25	V	$V_{SS}=0V$
2	Oscillator Clock Frequency	f_c		4.194304		MHz	
3	Oscillator Frequency Tolerance	Δfc		±0.1		%	
4	Operating temperature	To	0	25	+70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating supply current	I_{DD}		3.0		mA	
2	Input High Voltage (except OSC Input)	V_{IH}	$V_{DD}-1.5$			V	
3	Input High Voltage (for OSC Input only)	V_{IH}	$V_{DD}-1.0$			V	
4	Input Low Voltage	V_{IL}			$V_{SS}+1.5$	V	
5	Input Leakage Current (Pins 2 & 6)			0.1		µA	
6	Input impedance (Pin 1)	R_{IN}	10			kΩ	
7	Input impedance (Pin 3)	R_{IN}		4		kΩ	
8	Output high (source) current	I_{OH}	0.4			mA	$V_{OUT}=V_{DD}-0.4V$ (SD, ESt, DStD)
9	Output low (sink) current	I_{OL}	1.0			mA	$V_{OUT}=V_{SS}+0.4V$ (SD, ESt, DStD)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

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Charakterystyka elektryczna prądu przemiennego – powyżej zalecanych warunków pracy, o ile nie podano inaczej.

	Charakterystyka	Sym	Min	Typ‡	Max	Jednostki	Warunki testowe*
1	Prawidłowy poziom sygnału wejściowego (każdy ton sygnału kompozytowego)		-45		0	dBm	1,2,3,5,6,9
			4.36		775	mVRMS	1,2,3,5,6,9
2	Pozytywny zwrot akcji zaakceptuj				6	dB	1,2,3,4,9,14
3	Negatywny zwrot akcji zaakceptuj				6	dB	1,2,3,4,9,14
4	Odchylenie częstotliwości akceptowane		± 1,5% ± 2 Hz				1,2,3,5,9
5	Odrzucenie odchylenia częstotliwości		±3,5%				1,2,3,5,9
6	Tolerancja trzeciego tonu			-16		dB	1,2,3,4,5,9,12
7	Tolerancja hałasu			-12		dB	7,9,10
8	Tolerancja sygnału wybierania			+22		dB	8,9,11
9	3 dźwięków nadzorczych wykrywa poziom (moc całkowita)			-30		dBm	13 dla MT3270/3271
10	3 dźwięków nadzorczych nie wykrywa poziomu (moc całkowita)			-35		dBm	13 dla MT3270/3271
11	Nadzorujący integrator tonów czas ataku	t_{SA}		1.0		ms	dla MT3270/3271
12	Czas zaniku integratora tonów nadzorczych	t_{SD}		500		ms	dla MT3270/3271
13	Czas wykrycia obecności tonu (ESt)	t_{DP}	3		20	ms	dla MT3270/3274
14	Brak wykrycia tonu (ESt)	t_{DA}	0.5		20	ms	dla MT3270/3274
15	Czas trwania tonu akceptowany (DStD)	t_{REC}			40	ms	dla MT3271/3275
16	Odrzucenie czasu trwania tonu (DStD)	t_{REC}	20			ms	dla MT3271/3275
17	Pauza między palcami akceptuj (DStD)	t_{ID}			40	ms	dla MT3271/3275
18	Odrzucenie pauzy międzypalcowej (DStD)	t_{DO}	20			ms	dla MT3271/3275
19	Współczynnik wypełnienia współczynnika przesunięcia danych (ACK) 40%–60%				1	MHz	
20	Opóźnienie propagacji (ACK do Data)	t_{PAD}		100		ns	
21	Opóźnienie czasu konfiguracji (ESt/DStD do ACK)	t_{DL}	0			ns	
22	Czas utrzymywania danych (ACK do SD)	t_{DH}	30			ns	

‡ Typowe wartości podane są w temperaturze 25°C i mają charakter jedynie pomocniczy przy projektowaniu, nie są gwarantowane i nie podlegają testom produkcyjnym.

* Warunki testowe
1. dBm = decybele powyżej lub poniżej mocy odniesienia 1 mW przy obciążeniu 600 omów.
2. Sekwencja cyfr składa się ze wszystkich tonów DTMF.
3. Czas trwania tonu = 40 ms, tonu pauza = 40 ms.
4. Sygnał kondycjonowania składa się z nominalnych częstotliwości DTMF.
5. Oba tony w sygnale złożonym mają taką samą amplitudę.
6. Para tonów jest odchylona o ±1,5% ± 2 Hz.
7. Szum Gaussa o ograniczonym paśmie (3 kHz).
8. Dokładne częstotliwości sygnału wybierania to 350 Hz i 440 Hz (± 2 %).
9. Współczynnik błędów lepszy niż 1 na 10 000. Czas ochronny dla MT3270/MT3274 = 20 ms.
10. W odniesieniu do składowej o najniższej częstotliwości w sygnale DTMF.
11. W odniesieniu do minimalnego ważnego poziomu akceptacji.
12. Najgorsza częstotliwość zakłócająca.
13. W celach testowych na wejściu podłączono filtr kondycjonujący.
14. Oba tony muszą mieścić się w zakresie prawidłowego sygnału wejściowego.

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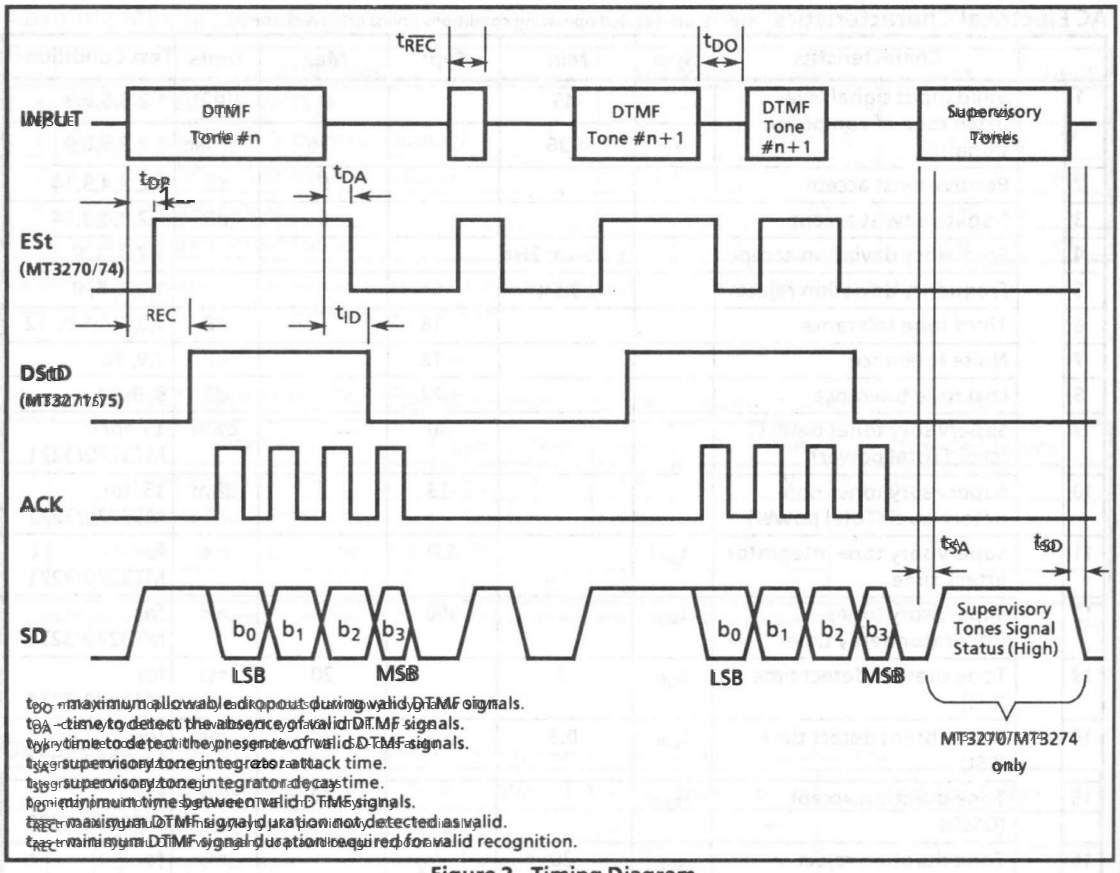

Figure 2 - Timing Diagram

Rysunek 2 – Diagram czasowy

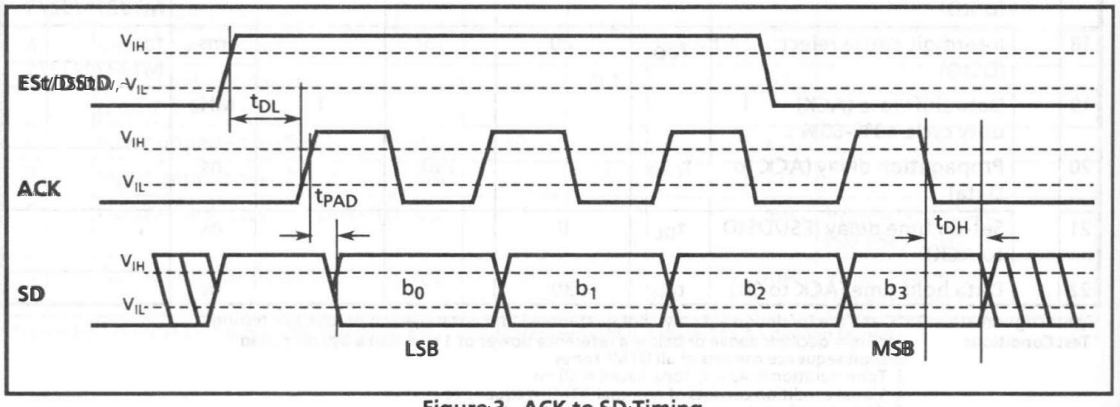

Figure 3 - ACK to SD Timing

Rysunek 3 – Czas ACK do SD

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Pin Description

Pin Description

Pin # / Numer wyprowadzenia		Name / Nazwa	Description / Opis
DIP	SOIC		
1	2	INPUT	**Audio Input.** Input signal must be AC coupled as shown in Fig.4. Wejście audio. Sygnał wejściowy musi być sprzężony prądem przemiennym, jak pokazano na rys.4.
2	4	OSC2	**Oscillator Output.** Wyjście oscylatora OSC2.
3	6	OSC1	**Oscillator Input.** This pin can either be driven by : 1) an external digital output with defined input logic levels. A coupling capacitor is required. 2) connecting a crystal between OSC1 and OSC2 pins. 3) connecting a ceramic resonator between OSC1 and OSC2 pins. Frequency of oscillation should be maintained at 4.194304 MHz ± 0.1%. Wejście oscylatora OSC1. Ten pin może być sterowany przez: 1) zewnętrzne cyfrowe wyjście sygnałowe z określonymi poziomami logiki wejściowej. Sprzęgło wymagany jest kondensator. 2) podłączenie kwarcu pomiędzy pinami OSC1 i OSC2. 3) podłączenie rezonatora ceramicznego pomiędzy pinami OSC1 i OSC2. Częstotliwość oscylacji powinna być utrzymywana na poziomie 4,194304 MHz ± 0,1%.
4	9	V_{SS}	**Ground, (0V)** Ziemia, (0V)
5	11	SD	**Serial Data Output.** In the absence of ACK input signal, a logic high output indicates the presence of tones. DTMF or supervisory tones (MT3270/MT3271 only). If ESt is high and the ACK pulse sequence is applied, the SD output provides a 4 bit binary code representing the decoded DTMF digit. Refer to Fig. 3. Wyjście danych szeregowych SD. W przypadku braku sygnału wejściowego ACK, wyjście logiczne wysokie wskazuje obecność tonów. DTMF lub tonów nadzorczych (MT3270/MT3271 tylko). Jeśli ESt jest wysoki i sekwencja impulsów ACK jest stosowana, wyjście SD zapewnia kod binarny 4-bitowy reprezentujący zdekodowaną cyfrę DTMF. Zobacz rys.3.
6	13	ACK	**Acknowledge Pulse Input.** After ESt or DStD goes high, applying a sequence of four pulses on this pin will shift out four bits on the SD pin representing the decoded DTMF digit. The rising edge of the first pulse will latch the data prior to shifting. Refer to Fig. 3. ACK Acknowledge Pulse Input. Po przejściu ESt or DStD w stan wysoki zastosowanie sekwencji czterech impulsów na tym pinie przesuwa cztery bity na pinie SD, reprezentując zdekodowaną cyfrę DTMF. Narastające zbocze pierwszego impulsu zabłokuje dane przed przesunięciem. Zobacz rysunek 3.
7	15	ESt (MT3270/ MT3274)	**Early Steering Output.** A logic high on ESt indicates that a DTMF signal is present. Wczesne wyjście sterujące. Wysoki poziom logiczny na ESt wskazuje, że sygnał DTMF jest obecny. (MT3270 obecnie (MT3274)
		DStD (MT3271/ MT3275)	**Delayed Steering Output.** A logic high on DStD indicates that a valid DTMF digit has been detected. Opóźnione wyjście sterujące. Logiczne wysoki na DStD wskazuje, że prawidłowa cyfra DTMF (wykryto MT3271. (MT3275)
8	18	V_{DD}	**Positive Power Supply.** (5V Typ.) Performance of the device can be optimized by minimizing noise on the supply rails. Decoupling capacitors across V_{DD} and V_{SS} are therefore recommended. Zasilanie dodatnie. (5 V typ.) Wydajność urządzenia można zoptymalizować poprzez minimalizowanie szumów na szynach zasilających. Kondensatory odsprzęgające w V_{DD} i V_{SS} są zatem zalecane.
	1,3,5, 7,8, 10,12, 14,16, 17	NC	**No Connection .** Brak połączenia.

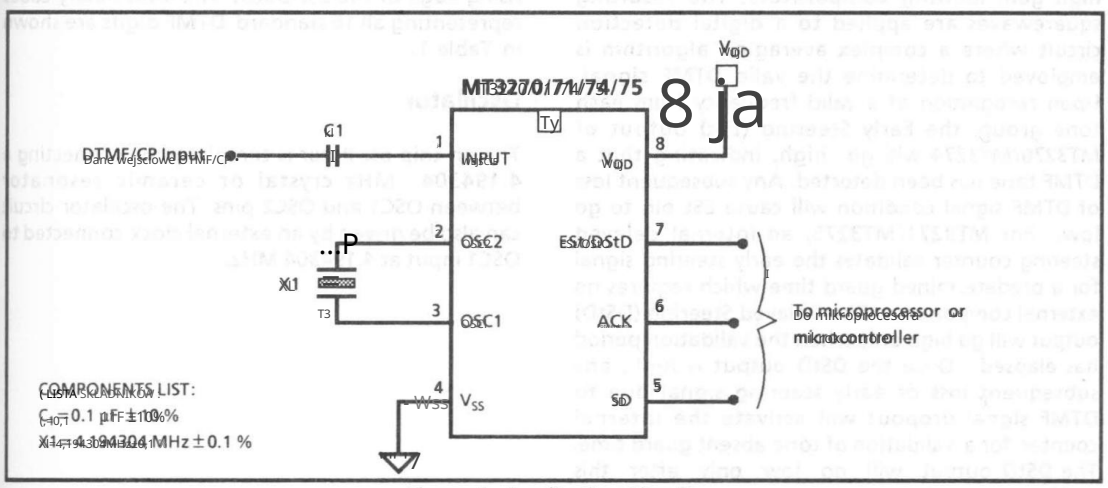

Figure 4 - Application Circuit
Rysunek 4 - Obwód aplikacyjny

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Functional Description

The MT3270/MT3271/MT3274/MT3275 is a high performance and low power consumption DTMF Receiver. The receiver provides wide dynamic range and a serial data output port. The MT3270/MT3271 also provides a supervisory tone detection function. The input signal is applied to a DTMF tone detection circuit and a supervisory tone detection circuit (MT3270/MT3271) via an Automatic Gain Control (AGC) circuit. The device incorporates a bandsplit filter section to separate the incoming DTMF signal into high and low group tones and a digital counting section to verify that the incoming signal corresponds to standard DTMF frequencies. Following verification, the DTMF signal is decoded into a 4-bit code and shifted out in a serial format.

Automatic Gain Control (AGC)

The input signal is buffered by an internal op amp, followed by an AGC circuit to provide a wide dynamic range. This signal is filtered by a lowpass filter to prevent aliasing distortion. This anti-aliasing filter also serves as the front end filter for the supervisory tone detection. The input signal is then routed to both the DTMF detection circuitry and the supervisory tone detection circuitry.

Filter and Decoder Section

Signals entering the DTMF detection circuitry are filtered by a notch filter at 350 and 440 Hz for dial tone rejection. This signal, still in its composite form, is split into its individual high and low frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then smoothed by an output filter and squared by high gain limiting comparators. The resulting squarewaves are applied to a digital detection circuit where a complex averaging algorithm is employed to determine the valid DTMF signal. Upon recognition of a valid frequency from each tone group, the Early Steering (ESt) output of MT3270/MT3274 will go high indicating that a DTMF tone has been detected. Any subsequent loss of DTMF signal condition will cause ESt pin to go low. For MT3271/MT3275, an internal delayed steering counter validates the early steering signal for a predetermined guard time which requires no external components. The Delayed Steering (DStD) output will go high only when the validation period has elapsed. Once the DStD output is high, any subsequent loss of early steering signal due to DTMF signal dropout will activate the internal counter for a validation of tone absent guard time. The DStD output will go low only after this validation period.

Supervisory Tone Detection (MT3270/MT3271)

The output signal from the AGC circuit is also applied to the supervisory tone detection circuit. When the signal level is above the threshold of the internal comparator, the supervisory tone detection circuit produces a tone present indication on the SD output. The detect circuit incorporates an integrator such that in the presence of supervisory tones, the SD output will remain a continuous high.

Since DTMF signals are in the detection bandwidth, the presence of a DTMF signal will also cause the SD output to go high. Therefore, the SD and ESt/DStD output pins should be monitored by a microprocessor in real time, so that various supervisory tones, presence of speech or DTMF signals can be identified. The supervisory tone detection circuit is enabled at all times except during the time between the rising edge of the first pulse and the falling edge of the fourth pulse on ACK pin (see Figure 2).

Serial Data (SD) Output

When a valid DTMF signal is present, ESt/DStD will go high. The application of four clock pulses on the ACK pin will provide a 4-bit serial binary code representing the decoded DTMF digit on the SD pin output. The rising edge of the first pulse applied on the ACK pin latches the data and the least significant bit of the decoded digit is also shifted out on the SD pin. The next three pulses on ACK pin will shift the remaining latched bits in a serial format (see Figure 3). If less than four pulses are applied to the ACK pin, new data cannot be latched even though ESt/DStD is valid. Clock pulses should be applied to shift out any remaining data bits and to resume normal operation. Any pulses in excess of four pulses will be ignored until the next rising edge of the ESt/DStD. The 4-bit binary codes representing all 16 standard DTMF digits are shown in Table 1.

Oscillator

The on-chip oscillator is completed by connecting a 4.194304 MHz crystal or ceramic resonator between OSC1 and OSC2 pins. The oscillator circuit can also be driven by an external clock connected to OSC1 input at 4.194304 MHz.

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F_{LOW}	F_{HIGH}	DIGIT	b_3	b_2	b_1	b_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

Table 1 Serial Decode Bit Table

Applications

The circuit shown in Figure 4 illustrates the use of the MT3270/MT3274/MT3275 in a typical receiver application. It requires only a crystal or ceramic resonator.

The MT3270/MT3274 is designed for the user who wishes to tailor the DTMF receiver for specific applications. When a DTMF signal is present, the ESt pin will go high. An external microprocessor monitors ESt in real time for a period of time set by the user. A guard time must be implemented such that DTMF signals of the appropriate duration are recognized. The MT3270/MT3275 uses an internal counter to provide a preset DTMF validation period. It requires no external components. The DStD output will indicate when a valid DTMF digit has been detected.

The 4194304 Hz frequency can be used as a secondary clock in systems where a real time clock is required. A 22-bit counter will count 4194304 cycles to provide a one second time base.

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NOTES:

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February 1985

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Features

- Up to 55 dB Dynamic Range.
- AGC for precise twist adjustment.
- No exernal components needed.
- Direct connection to telephone lines.
- Exceptional talk off.
- 14 dB acceptable signal to noise ratio.
- Acquisition time adjustable down to 10 ms.
- Major parameters externally adjustable.
- 5 V and 8 V to 12 V operation.

- Zakres dynamiki do 55 dB.
- AGC do precyzyjnej regulacji skrętu.
- Nie są wymagane żadne komponenty zewnętrzne.
- Bezpośrednie podłączenie do linii telefonicznych.
- Wyjątkowa gadatliwość.
- Stosunek sygnału do szumu wynosi 14 dB (akceptowalny).
- Czas akwizycji regulowany do 10 ms.
- Główne parametry można regulować zewnętrznie.
- Praca w zakresie 5 V i 8 V do 12 V.

Applications

- End to end signalling.
- Control systems.
- Mobile radio.
- Central office.
- PABX.
- Key systems.

- Sygnalizacja typu end-to-end
- Systemy sterowania.
- Radiotelefonia
- Centrala centralne.
- Centrala PABX.
- System kluczy.

Description

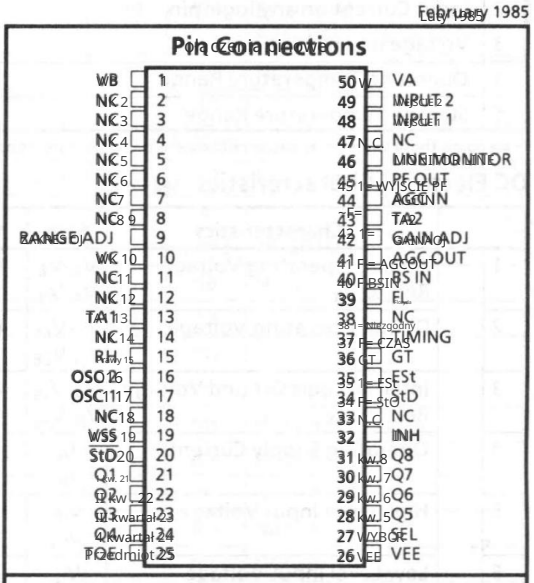
The Mitel MH88305 Hybrid TOUCH-TONE® Receiver is a high performance, high quality unit packaged in a dual-in-line hybrid measuring 2.5"x1.5"x0.25" and requires no external components for normal operation. The unit features exceptional dynamic range and precise twist performance, both adjustable to meet the exacting demands of end to end signalling applications as well as providing a unit of excellent central office quality. The MH88305 utilizes a digital detection algorithm which provides the unit with excellent talk-off immunity and signal to noise performance. Bandsplit filtering is achieved using the Mitel ISO²-CMOS MT8865 DTMF filter.

Opis

Odbiornik hybrydowy DUOTON-TONE® MH88305 jest to jednostka o wysokiej wydajności i jakości, pakowana w hybrydzie dual-in-line o wymiarach 2,5"x1,5"x0,25" nie wymaga żadnych zewnętrznych komponentów do normalnego działania. Jednostka charakteryzuje się wyjątkową dynamiką zasięgu i precyzyjną obsługą skrętu, oba regulowane, aby sprostać wymaganiom końcowym aplikacji sygnalizacji końcowej, a także zapewniania jednostka o doskonałej jakości biura centralnego. Ten odporność na stosunek sygnału do szumu. Pitrowanie z podziałem pasma odbywa się przy użyciu Mitel 1962-CMOS MT8865 DTMF filter.

Pin Connections

Connection Diagram



Ordering Information

MH88305 50 Pin −40°C to +85°C

Informacje o zamówieniu

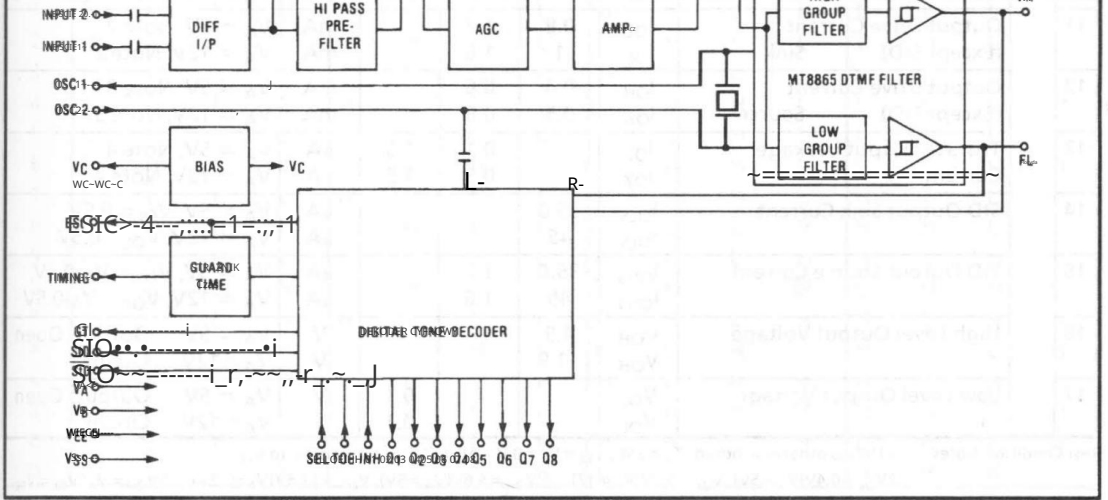


Figure 1. Functional Block Diagram

Rysunek 1. Schemat blokowy funkcji

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Absolute Maximum Ratings*

Wartości bezwzględne graniczne*

	Parameter	Symbol	Min	Max	Units
1	Napięcie zasilania Supply Voltage V_A vs V_{EE} V_A vs V_B V_{SS} vs V_{EE} Pracy 5 V Operation V_A vs V_{SS}	V_{DD}		15 15 5.5	V V V
2	Prąd wejściowy na dowolnym pinie logicznym Input Current on any logic pin	I_{IN}		10	mA
3	Napięcie na dowolnym pinie logicznym Voltage on any logic pin	V_{IN}	V_{EE} -0.3	V_A +0.3	V
4	Zakres temperatury pracy Operating Temperature Range	T_A	-40	+85	°C
5	Zakres temperatur przechowywania Storage Temperature Range	T_{STG}	-55	+100	°C

*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Funkcjonowanie urządzenia w tych warunkach nie jest domniemane.
*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics - See Note 1.

Charakterystyki elektryczne prądu stałego - patrz uwaga 1

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Analogowe napięcie robocze Analog Operating Voltage Ref. to V_B Ref. do V_B	V_A vs V_B V_A vs V_B	4.75 4.75		 13	V V	V_A = 5 V_A = 5V V_A = 12 V_A = 12V
2	Cyfrowe napięcie robocze Digital Operating Voltage V_A vs V_{EE} V_A vs V_{EE}	V_A vs V_{EE} V_A vs V_{EE}	4.75 4.75		 13	V V	V_A = 5 V_A = 5V V_A = 12 V_A = 12V
3	Wewnętrzne napięcie uziemienia logiki Internal Logic Ground Voltage Ref. vs V_{SS} Ref. do V_{SS}	V_A-V_{SS} V_A-V_{SS}	4.75 6.0	 6.5	5.25 7.5	V V	V_A = 5 V_A = 5V V_A = 12 V_A = 12V
4	Prąd roboczy Operating Supply Current	I_A I_A		10 15		mA mA	V_A = 5 V_A = 5V V_A = 12 V_A = 12V
5	Wysoki poziom napięcia wejściowego High Level Input Voltage	V_{IH} V_{IH}	3.5 8.5			V V	V_A = 5 V_A = 5V V_A = 12 V_A = 12V
6	Niski poziom napięcia wejściowego Low Level Input Voltage	V_{IL} V_{IL}			1.5 3.5	V V	V_A = 5 V_A = 5V V_A = 12 V_A = 12V
7	Pull Down Sink Current (INH, SEL)	I_{SI} I_{SI}	10 10	25 200	75 400	µA µA	V_A = 5 V_{IH} = 5V, V_{IH} = V_A V_A = 12 V_{IH} = 12V, V_{IH} = V_A
8	Pull Up Source Current (TOE)	I_{SO} I_{SO}	2 2	7 7	45 45	µA µA	V_A = 5 V_{IL} = 5V, V_{IL} = V_{EE} V_A = 12 V_{IL} = 12V, V_{IL} = V_{EE}
9	Wysoki wyciek wejściowy Input High Leakage Current	I_{IH} I_{IH}		0.1 0.1	1.5 1.5	µA µA	V_A = 5 V_{IH} = 5V, V_{IH} = V_A V_A = 12 V_{IH} = 12V, V_{IH} = V_A
10	Wejściowy niski prąd upływu Input Low Leakage Current	I_{IL} I_{IL}		0.1 0.1	1.5 1.5	µA µA	V_A = 5 V_{IL} = 5V, V_{IL} = V_{EE} V_A = 12 V_{IL} = 12V, V_{IL} = V_{EE}
11	Wyjściowy prąd napędowy (Z wyjątkiem StD) Output Drive Current (Except StD) Sink	I_{OL} I_{OL}	0.8 1	1.2 1.6		mA mA	V_A = 5 Uwaga 5V, Note 2 V_A = 12 Uwaga 12V, Note 2
12	Wyjściowy prąd napędowy (Z wyjątkiem StD) Output Drive Current (Except StD) Source	I_{OH} I_{OH}	0.4 0.5	0.6 0.8		mA mA	V_A = 5 Uwaga 5V, Note 3 V_A = 12 Uwaga 12V, Note 3
13	Wyciek wyjściowy w stanie wysokiej impedancji Tristate Output Leakage Current	I_{OZ} I_{OZ}		0.1 0.3	1.5 1.5	µA µA	V_A = 5 Uwaga 5V, Note 4 V_A = 12 Uwaga 12V, Note 4
14	Prąd wyjściowy StD StD Output Sink Current	I_{OLS} I_{OLS}	35.0 45			µA µA	V_A = 5 V_{OL} = 0.5V, V_{OL} = 0.5V V_A = 12 V_{OL} = 0.5V, V_{OL} = 0.5V
15	Prąd wyjściowy StD StD Outputs Source Current	I_{OHS} I_{OHS}	35.0 45	1.2 1.6		µA µA	V_A = 5 V_{OH} = 5V, V_{OH} = V_A-0.5V V_A = 12 V_{OH} = 12V, V_{OH} = V_A-0.5V
16	Wysokie napięcie na wyjściu High Level Output Voltage	V_{OH} V_{OH}	4.9 11.9			V V	V_A = 5 V_A = 5V Outputs Open V_A = 12 V_A = 12V Circuit
17	Niski poziom napięcia wyjściowego Low Level Output Voltage	V_{OL} V_{OL}			0.1 0.1	V V	V_A = 5 V_A = 5V Outputs Open V_A = 12 V_A = 12V Circuit

Uwagi dotyczące warunku testowego, chyba że zaznaczono inaczej: T_A = 25°C, V_{EE} = 0V. Wszystkie napięcia odniesione do V_{EE}.
Test Condition Notes: unless otherwise noted, T_A = 25°C, V_{EE} = 0V. All voltages referenced to V_{EE}.

① V_{OL} = 0.4V (5V), 0.5V (12V) ② V_{OH} = 2.4V (5V), 9.6V (12V) ③ V_{OH} = 4.5V (5V), 11.5V (12V) ④ V_{OH} = V_A, V_{OL} = V_{EE}

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AC Electrical Characteristics

Parametry elektryczne prądu zmiennego — Uwaga 5 — See Note 1.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Maximum Valid Input Signal (Each tone of composite signal)		+3 +3			dBm dBm	$V_A = 5V$ $V_A = 12V$
2	Minimum Valid Input Signal (Each tone of composite signal)		-26 -46		-20 -40	dBm dBm	Normal Extended
3	Accept Signal to Noise Ratio		14			dB	Note 2
4	Maximum Twist Acceptance		±6	+9		dB	
5	Frequency Detect Bandwidth	Δf_A	±1.8		±3.5	% Nom	
6	Differential Input Impedance		360	400		kΩ	f = 1 kHz
7	DC Common Mode Tolerance		±2000			V	
8	AC Common Mode Tolerance		70			V_{rms}	15-60 Hz
9	Dial Tone Tolerance		30			dB	Note 3
10	Tone Present Detection Time	t_{DP}	6		10	ms	
11	Tone Absent Detection Time	t_{DA}	0.5		6	ms	
12	Tone Present Guard Time	t_{GTP}		25		ms	Note 4
13	Tone Absent Guard Time	t_{GTA}		35		ms	Note 4
14	Minimum Tone Duration	t_{REC}			40	ms	Note 4
15	Maximum Invalid Tone Duration	t_{REC}			20	ms	Note 4
16	Minimum Interdigit Pause	t_{ID}			40	ms	Note 4
17	Maximum Interdigit Dropout	t_{DO}			20	ms	Note 4
18	Data Valid to StD Delay	t_{PSTD}	6		10	µs	

Notes:
1. Unless otherwise noted: $T_A = 25°C$; $V_A = 5V$ or 12V; normal mode; no external adjustment.
2. Band-limited white noise, 300 Hz - 3400 Hz, 50 ms on/50 ms off. Error Rate < 1 in 10,000.
3. Relative to minimum valid input signal level (A).
4. No external guard time components; $V_A = 12V$.
5. No external level adjustment. Typically up to a further 6 dB of sensitivity is available by insertion of R_{TI} (Fig. 10), see text.

	StD = H (Two-of-8 Code)								StD = L (Two 4-Bit Binary Codes)							
	Q_1	Q_2	Q_3	Q_4	Q_1	Q_2	Q_3	Q_4	Q_1	Q_2	Q_3	Q_4	Q_1	Q_2	Q_3	Q_4
1	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
2	H	L	L	L	L	H	L	L	L	H	L	L	L	H	L	L
3	H	L	L	L	L	L	H	L	H	H	L	L	L	L	H	L
4	L	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H
5	L	H	L	L	L	H	L	L	H	L	H	L	L	H	L	H
6	L	H	L	L	L	L	H	L	L	H	H	L	L	L	H	H
7	L	L	H	L	H	L	L	L	H	H	H	L	H	L	L	L
8	L	L	H	L	L	H	L	L	L	L	L	H	H	H	L	L
9	L	L	H	L	L	L	H	L	H	L	L	H	H	L	H	L
0	L	L	L	H	L	H	L	L	L	H	L	H	L	H	H	L
*	L	L	L	H	H	L	L	L	H	H	L	H	H	L	H	H
#	L	L	L	H	L	L	H	L	L	L	H	H	H	L	L	H
A	H	L	L	L	L	L	L	H	H	L	H	H	H	H	H	L
B	L	H	L	L	L	L	L	H	L	H	H	H	H	H	L	H
C	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H
D	L	L	L	H	L	L	L	H	L	L	L	L	H	H	H	H

Table 1 - Output Truth Table

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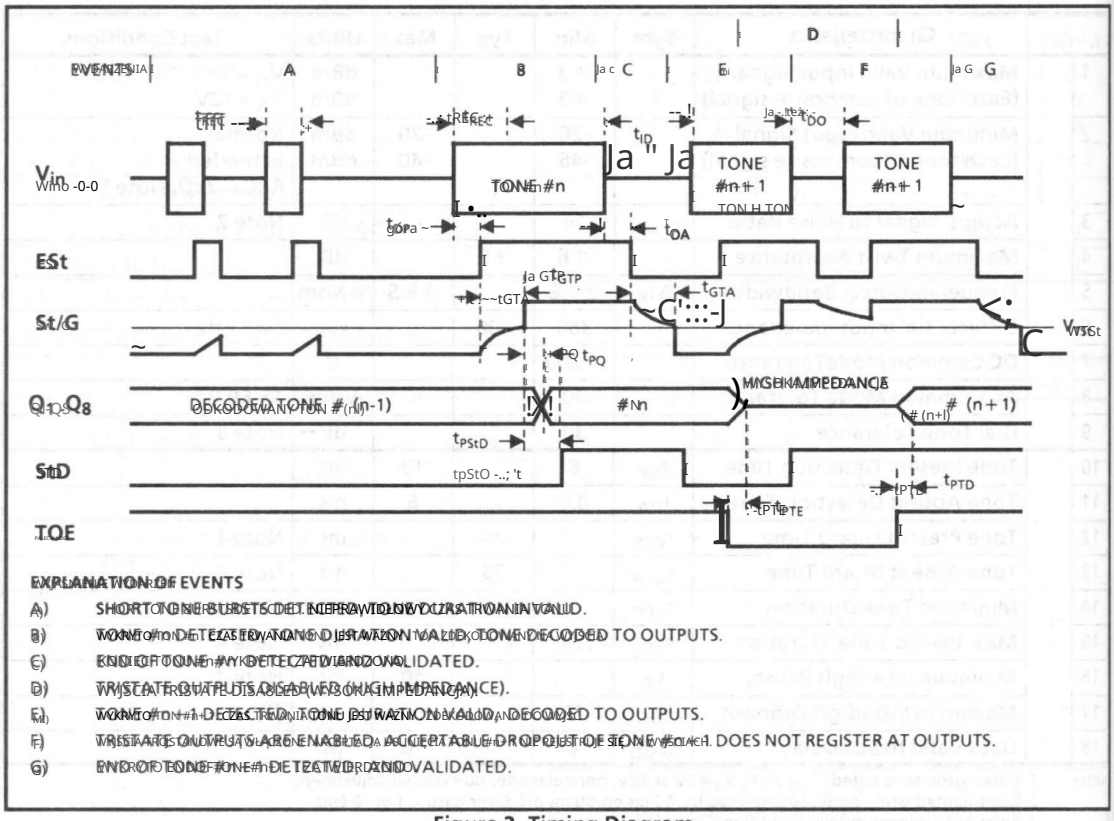

EXPLANATION OF EVENTS

A) SHORT TONE BURSTS DETECTED BUT REJECTED DUE TO TIMING VALUE.
B) VALID TONE #n DETECTED AND QUALIFIED. TONE #n DECODED TO OUTPUTS.
C) END OF TONE #n DETECTED AND VALIDATED.
D) TRISTATE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) VALID TONE #n+1 DETECTED AND QUALIFIED. TONE #n+1 DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ENABLED. ACCEPTABLE DROPOUT OF TONE #n+1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE #n+1 DETECTED AND VALIDATED.

Figure 2 Timing Diagram

Rysunek 2 Diagram czasowy

Pin Description

Opis wyprowadzeń

Pin #	Name	Description
1	V_{EE}	Negative Analog Power Supply.
2-8	NC	No Connection.
9	RANGE ADJ.	Resistor connected between Pin 9 and V_{EE} (Pin 10) increases input sensitivity.
10	V_{EE}	Internally derived reference voltage output.
11-12	NC	No Connection.
13	TA1	Twist Adjust 1. Resistor connected between Pin 13 and TA2 (Pin 42) increases twist acceptance. See Figs. 9 and 10.
14	NC	No Connection.
15	FiH	Test output of High Group Schmitt trigger.
16	OSC 2	Test output of internal oscillator amplifier. 3.579545 MHz.
17	OSC 1	Test input of internal oscillator amplifier.
18	NC	No Connection.
19	V_{SS}	Internal logic ground. Shorted to V_{EE} (Pin 26) for 5V Logic Operation.
20	$\overline{StD}$	Buffered inverted StD.

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Pin Description (cont'd)

Pin #	Name	Description
21	Q_1	Data Outputs 3-state buffered. Provides 4 bit binary word (SEL. LOW) or half of 2 of 8 binary word (SEL. HIGH), corresponding to the tone pair decoded, when enabled by TOE. See Table 1 for state table.
22	Q_2	
23	Q_3	
24	Q_4	
25	TOE	3-State Output Enable logic input. Active HIGH enables Q_1-Q_8 data output. When TOE = LOW, Q_1-Q_8 are high impedance.
26	V_{EE}	Negative Logic Power Supply. Logic ground for output signals.
27	SEL	Output Code Select logic input. HIGH on this input selects 2 of 8 code active HIGH on Q_1-Q_8. LOW selects two 4-bit codes on Q_1-Q_4 and Q_5-Q_8.
28	Q_5	Data outputs 3-state buffered. Provides 4 bit binary word (SEL. LOW) or half of 2 of 8 binary word (SEL. HIGH), corresponding to the tone pair decoded, when enabled by TOE. See Table 1 for state table.
29	Q_6	
30	Q_7	
31	Q_8	
32	INH	Inhibit logic input. Active HIGH disables detection of A, B, C, D, *, #.
33	NC	No Connection.
34	StD	Valid Tone Detect indication, logic output. Active HIGH.
35	ESt	Early Steering Digital Output. Active HIGH indicates digital detection of valid tone pair.
36	GT	Guard Time Output. Normally connected to (Pin 37), TIMING.
37	TIMING	Guard Time Adjust. A capacitor connected between Pin 37 and V_A (Pin 50) increases guard time. A resistor connected between Pin 37 and ESt (Pin 35) decreases guard time.
38	NC	No Connection.
39	FL	Test output of Low Group Schmitt trigger.
40	BS IN	Analog input to the bandsplitting filters. Normally connected to AGC OUT (Pin 41).
41	AGC OUT	Analog output of the AGC circuit. Normally connected to BS IN (Pin 40).
42	GAIN ADJ	Adjusts signal level into MT8865. Shorted to TA2 (Pin 43) for 5V analog operation.
43	TA2	Twist adjust 2. Resistor connected between Pin 43 and AGC output (Pin 41) decreases twist acceptance. See Figs. 9 and 10.
44	AGC IN	Analog input to the AGC circuit. Normally connected to PF OUT (Pin 45).
45	PF OUT	Analog output from Dial Tone Reject Highpass filter. Normally connected to AGC IN (Pin 44).
46	LINE MONITOR	Single-ended test output of the differential line input. Attenuated 6 dB referred to line input signal.
47	NC	No Connection.
48	INPUT 1	Differential line inputs AC coupled. Direct connection to telephone line.
49	INPUT 2	
50	V_A	Positive Power Supply.

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Opis funkcjonalny

Odbiornik tonów DTMF firmy Mitel Hybrid wyróżnia się niewielkimi rozmiarami (2,5"x 1,5"), wyjątkową wydajnością wykrywania sygnału i wysoką jakością, uzyskaną dzięki zastosowaniu najnowocześniejszej technologii grubowarstwowej i CMOS/LSI. Nie są potrzebne żadne zewnętrzne komponenty, urządzenie można podłączyć bezpośrednio do linii telefonicznych. Wyjścia cyfrowe są kompatybilne z CMOS i Low Power Schottky TTL (2 obciążenia). Jednostka jest szczególnie odpowiednia do zastosowań, w których wymagana jest wysoka czułość, wysoki skręt i wykrywanie w obecności szumu, takich jak sygnalizacja typu end-to-end, radio mobilne, centrala, PABX i inne zastosowania.

Aby zapewnić maksymalną elastyczność, wszystkie główne bloki funkcjonalne odbiornika są dostępne z zewnątrz, a użycie zewnętrznego rezystora umożliwia regulację czułości wejściowej, ograniczenia przebiegu skrętu w celu akceptacji/odrzucenia oraz skrócenie czasu ochronnego, podczas gdy użycie zewnętrznego kondensatora pozwala wydłużenie czasu ochronnego.

MH88305 jest zaprojektowany do akceptowania standardowych częstotliwości DTMF zalecanych przez CCITT, zwykle generowanych przez telefon z przyciskiem TOUCH-TONE. Zobacz rys. 4.

Sygnał wejściowy jest odbierany na INPUT 1 i INPUT 2, które zapewniają sprzężoną prądem przemiennym zrównoważoną różnicową impedancję wejściową wynoszącą około 400 kΩ. Sygnał jest przesyłany do górnoprzepustowego filtra wstępnego, zapewniającego 60 dB tłumienia sygnału wybierania w zakresie częstotliwości 0-480 Hz. Zastosowanie obwodu AGC zapewnia jednostce zakres dynamiki do 55 dB, a wzmacniacz wyjściowy AGC umożliwia precyzyjną regulację skrętu.

Sygnały o wysokiej i niskiej częstotliwości są oddzielane przez filtr/limiter DTMF MT8865, którego wyjścia są falami prostokątnymi o tej samej częstotliwości co przychodzące tony wysokie i niskie i pojawiają się odpowiednio na FH i FL.

Dekoder tonów cyfrowych na chipie akceptuje sygnały FH i FL i wykonuje złożony, opatentowany algorytm uśredniania opracowany empirycznie w ramach praktycznej telekomunikacji. Po prawidłowym wykryciu zarówno tonu wysokiego, jak i niskiego wczesny wysterowany sygnał (ESt) przechodzi w stan WYSOKI. (Patrz rys. 2.) Aktywuje prosty analogowy obwód czasu ochronnego, który działa na zasadzie akwizycji i zwalniania tonu, zapobiegając rozpoznawaniu wielu cyfr w przypadku obecności szumu impulsowego lub przerwy w tonie krótszej niż dopuszczalny czas zaniku tonu. W przypadku zaniku tonu lub zmiany częstotliwości przed upływem czasu ochronnego (t_{GTP}) sygnał ESt przechodzi w stan niski, resetując analogowy obwód czasu ochronnego, a algorytm wykrywania cyfrowego zostaje powtórzony.

Pozytywne przejście StD wskazuje, że zatrzaski wyjściowe Q-Q zostały zaktualizowane. Trzy formaty wyjściowe można wybrać za pomocą SEL Pin 27. Te formaty to 2 z 8 aktywnych wysokich i dwa 4-bitowe kody. Tabela prawdy jest wymieniona w Tabeli 1. Dane w zatrzaskach wyjściowych pozostaną stabilne do momentu prawidłowego rozpoznania kolejnej pary tonów. Opóźniony sygnał stroboskopowy (StD) jest dostępny na Pinie 34 i ten sygnał pozostaje WYSOKI przez czas trwania wykrytej pary tonów i przechodzi w niski po upływie czasu ochrony zwolnienia (t_{GTA}). Dodatkowo, trójstanowe włączenie wyjścia, TOE, (pin 25) jest zapewnione w celu umożliwienia magistralowania wyjść danych.

Ustawienie pinu INH w stanie WYSOKIM umożliwia użytkownikowi zablokowanie dekodowania par tonów odpowiadających oznaczeniom klawiatury A, B, C, D, *, # ze względów bezpieczeństwa lub w celu dalszego zmniejszenia podatności na wyłączanie się połączeń.

Aplikacje

Typowy schemat połączeń (rys. 3) ilustruje łatwość, z jaką układ MH88305 można zastosować w systemie, nie wymagając żadnych dodatkowych komponentów zewnętrznych do realizacji funkcji odbioru i dekodowania tonów, a także zapewniając bezpośrednie połączenie z układem CMOS Logic 5V.

Wyjścia Q_1-Q_4 i StD są bezpośrednio interfejsowalne do Low Power Schottky TTL, jeśli VA i VBE są podłączone odpowiednio do dodatnich i ujemnych szyn TTL. Jednak konieczne jest buforowanie StD, jak pokazano na rys. 5.

Cechą MH88305 jest elastyczność dostosowywania parametrów rozpoznawania tonów poprzez użycie pojedynczych zewnętrznych komponentów. Następujące parametry są regulowane:

- czułość wejściowa
- czas ochronny
- ograniczenie akceptacji/odrzucenia skrętu.

Metody zwiększania lub zmniejszania każdego z tych parametrów pokazano odpowiednio na rys. 7, 8, 9 i 10. Należy zauważyć, że minimalne ważne poziomy sygnału wejściowego określone w Charakterystyce elektrycznej prądu przemiennego i rys. 7 mają zastosowanie, gdy sygnał wejściowy nie ma skrętu.

Dostosowanie poziomu akceptacji skrętu i minimalnego prawidłowego sygnału wejściowego można wykonać w następujący sposób. Używając rys. 9 lub 10, określ wartość rezystora regulacji skrętu (R_T) dającą pożądany poziom akceptacji skrętu. Odejmij 9 dB od tego poziomu akceptacji skrętu (w dB) i dodaj ten wynik do żądanego minimalnego prawidłowego sygnału wejściowego. Przy tym dostosowanym poziomie sygnału użyj rys. 7, aby określić

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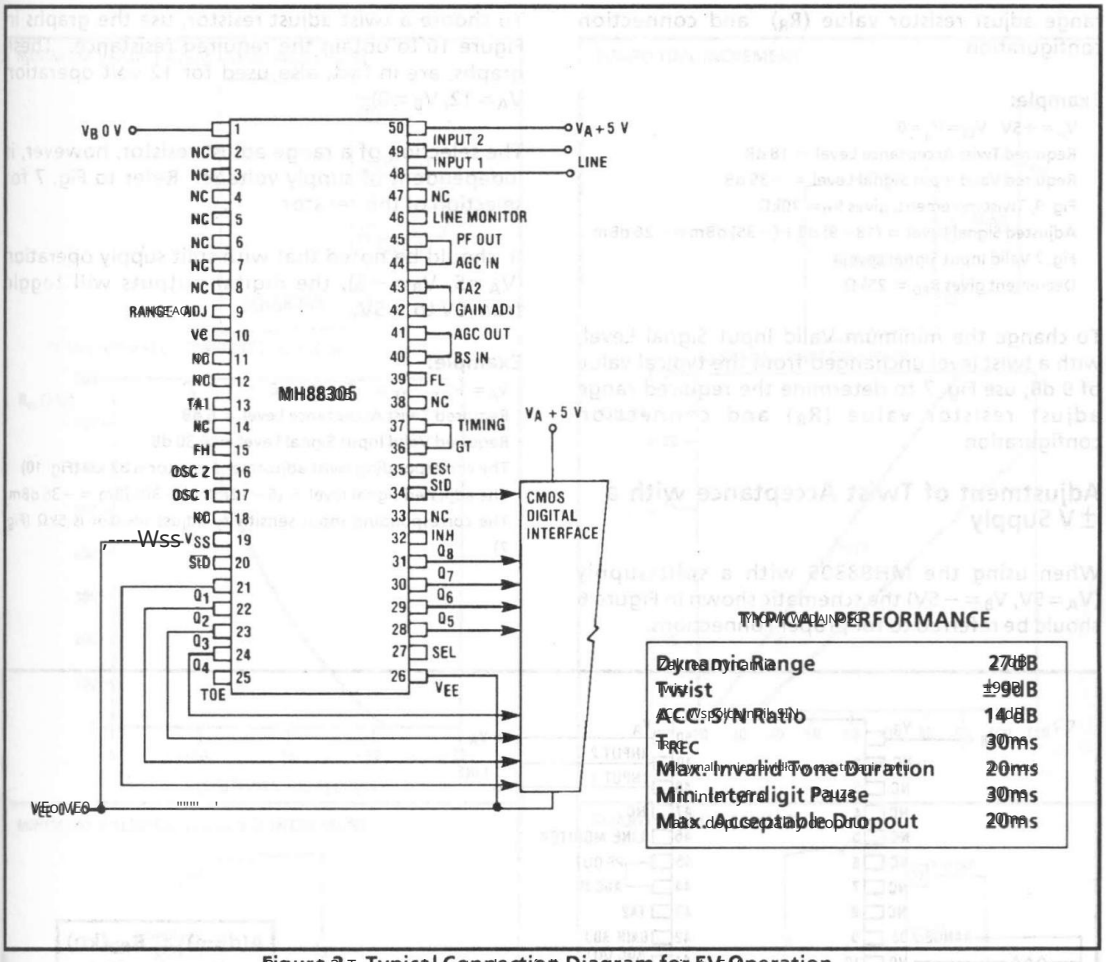

TYPICAL PERFORMANCE

Dynamic Range	27dB
Twist	±9dB
ACC.S/N Ratio	14dB
TREC	30ms
Max. Invalid Tone Duration	20ms
Min. Interdigit Pause	30ms
Max. Acceptable Dropout	20ms

Figure 3. Typical Connection Diagram for 5V Operation

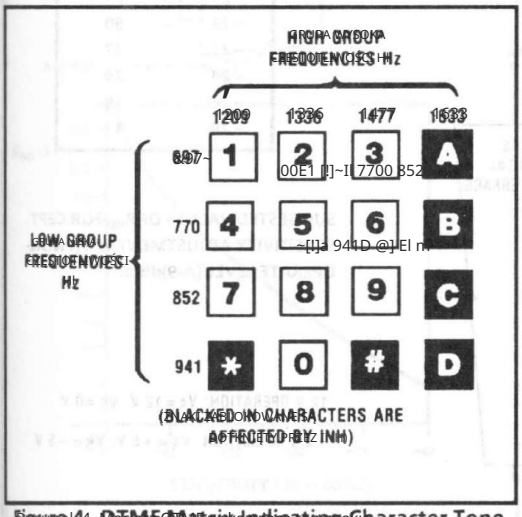

Figure 4. DTMF Matrix Indicating Character Tone Pair Correspondence

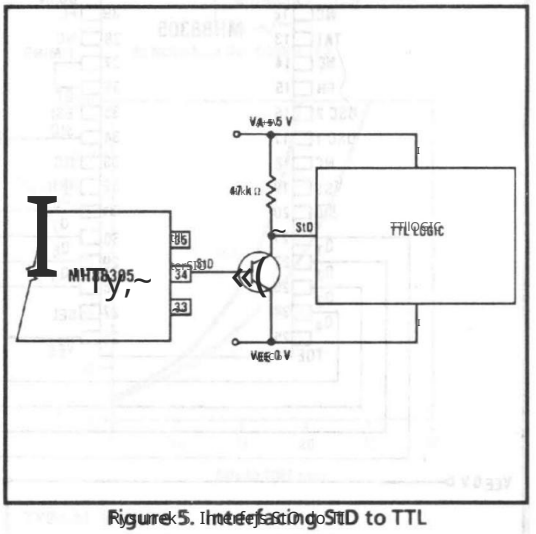

Figure 5. Interfacing STD to TTL

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range adjust resistor value (R_R) and connection configuration.

zakresu regulacji wartości rezystora(RR) i konfiguracji połączenia.

Example:

Przykład:

$V_A = +5V, V_{EE} = V_B = 0$

V_A +5V V_{EE} = V_B = 0

Required Twist Acceptance Level = 18 dB

Required Twist Acceptance Level dB 18 dB

Required Valid Input Signal Level = −35 dBm

Required Valid Input Signal Level dBm −35 dBm

From Fig. 9, Twist Increment, gives R_T = 20kΩ

Fig 9, Twist Przyrost , daje R_T = 20kΩ

Adjusted Signal Level = (18 − 9) dB + (−35) dBm = −26 dBm

Adjusted Signal Level = (18−9)dB + (−35)dBm = −26 dBm

Fig 7 Valid Input Signal Level

Fig 7 Poprawny poziom sygnału wejściowego

Decrement gives R_{RD} = 25kΩ

Dekrementacja daje R_{RD} 25kΩ

To change the minimum Valid Input Signal Level, with a twist level unchanged from the typical value of 9 dB, use Fig. 7 to determine the required range adjust resistor value (R_R) and connection configuration.

Aby zmienić minimalny prawidłowy poziom sygnału wejściowego, przy zachowaniu poziomu skrętu niezmienionego od typowej wartości 9 dB, należy użyć rys. 7 w celu określenia wymaganej wartości rezystora regulacji zakresu (RR) i konfiguracji połączenia.

To choose a twist adjust resistor, use the graphs in Figure 10 to obtain the required resistance. These graphs are in fact also used for 12 volt operation ($V_A = 12, V_B = 0$).

Aby wybrać rezystor do regulacji skrętu, należy użyć wykresów z rysunku 10, aby uzyskać wymagany opór. Wykresy te są w rzeczywistości również używane do pracy przy napięciu 12 V ($V_A = 12, V_B = 0$).

The selection of a range adjust resistor, however, is independent of supply voltage. Refer to Fig. 7 for selection of this resistor.

Wybór rezystora do regulacji zakresu jest jednak niezależny od napięcia zasilania. Zobacz rys. 7, aby zapoznać się z wykresem regulacji rezystora.

It should be noted that with split supply operation ($V_A = 5, V_B = -5$), the digital outputs will toggle from 0V to +5V.

Należy pamiętać, że przy pracy z rozdzielonym zasilaniem ($V_A = 5, V_B = -5$) wyjścia cyfrowe będą przełączać się z 0V na +5V.

Example:

Przykład:

V_A +5V 5V V_B −5 −5 V_{EE} = 0

Required Twist Acceptance Level dB = 6 dB

Required Valid Input Signal Level = −30 dBm

Required Valid Input Signal Level dBm −30 dBm

From Fig. 10, Twist Increment, gives R_T = 82kΩ (Fig. 10)

Z wykresu regulacji przyrostu skrętu, daje R_T = 82kΩ (rys. 10)

The adjusted signal level = (6 − 12) dB + (−30) dBm = −36 dBm

The adjusted signal level = (6−12)dB + (−30)dBm = −36 dBm

From Fig. 7, Decrement gives R_{RD} = 5kΩ (Fig. 7).

Z wykresu regulacji czułości, dekrementacja daje R_{RD} = 5kΩ (rys. 7).

Adjustment of Twist Acceptance with a 5V Supply

Regulacja akceptacji skrętu przy zasilaniu 5V

When using the MH8830S with a split supply (V_A = 5V, V_B = −5V) the schematic shown in Figure 6 should be referred to for proper connections.

W przypadku stosowania modułu MH8830S z rozdzielaczem (VA 5V, VB = −5V) w celu uzyskania prawidłowych połączeń należy zapoznać się ze schematem przedstawionym na rysunku 6.

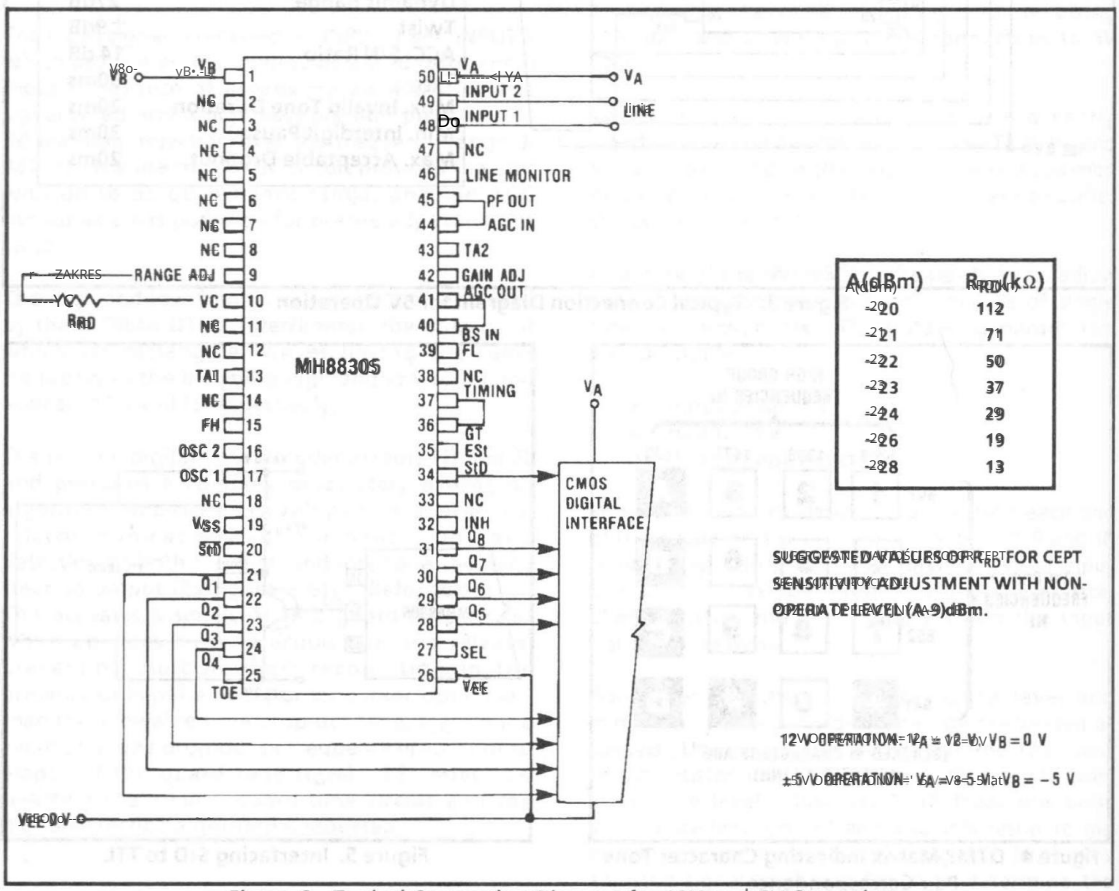

Figure 6 - Typical Connection Diagram for 12V or ±5V Operation

Rysunek 6 Typowy schemat połączeń dla pracy przy napięciu 12V lub ± 5V

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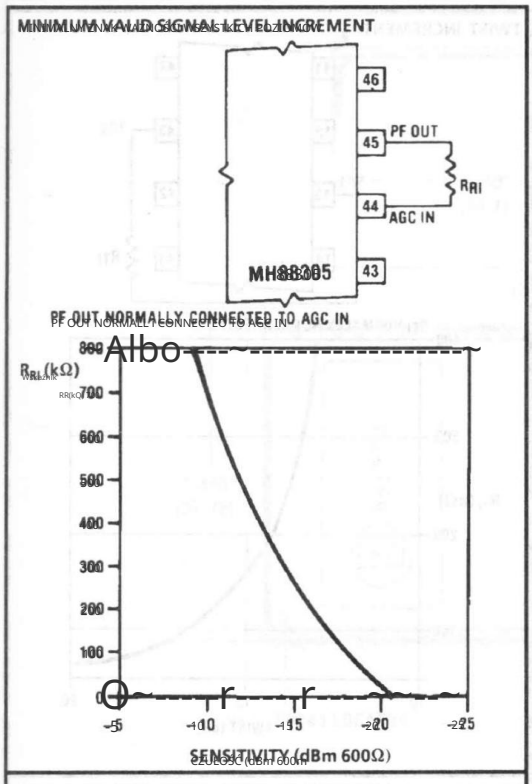

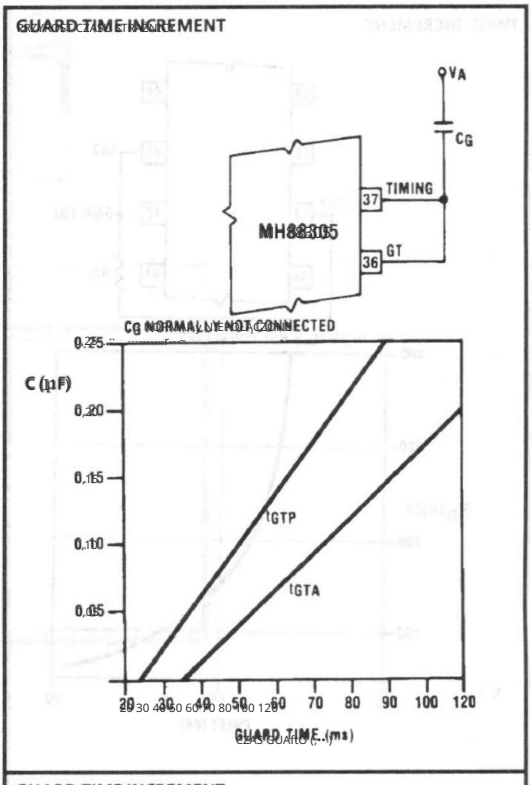

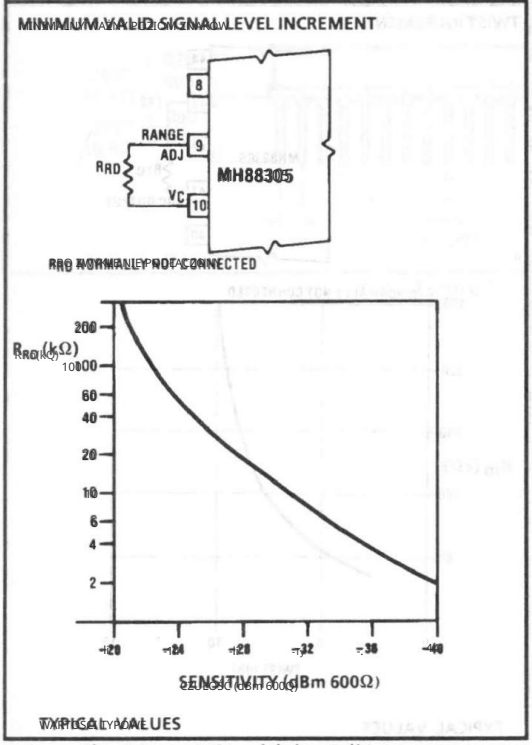

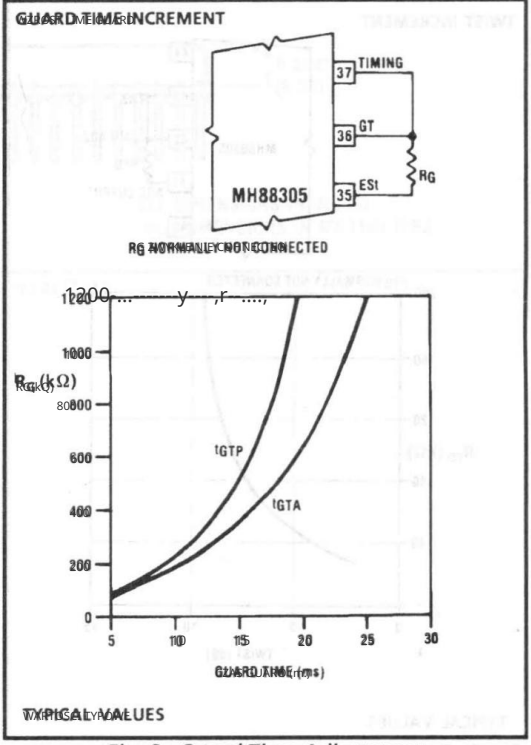

Fig. 7 - Input Sensitivity Adjustment

Fig. 8 - Guard Time Adjustment

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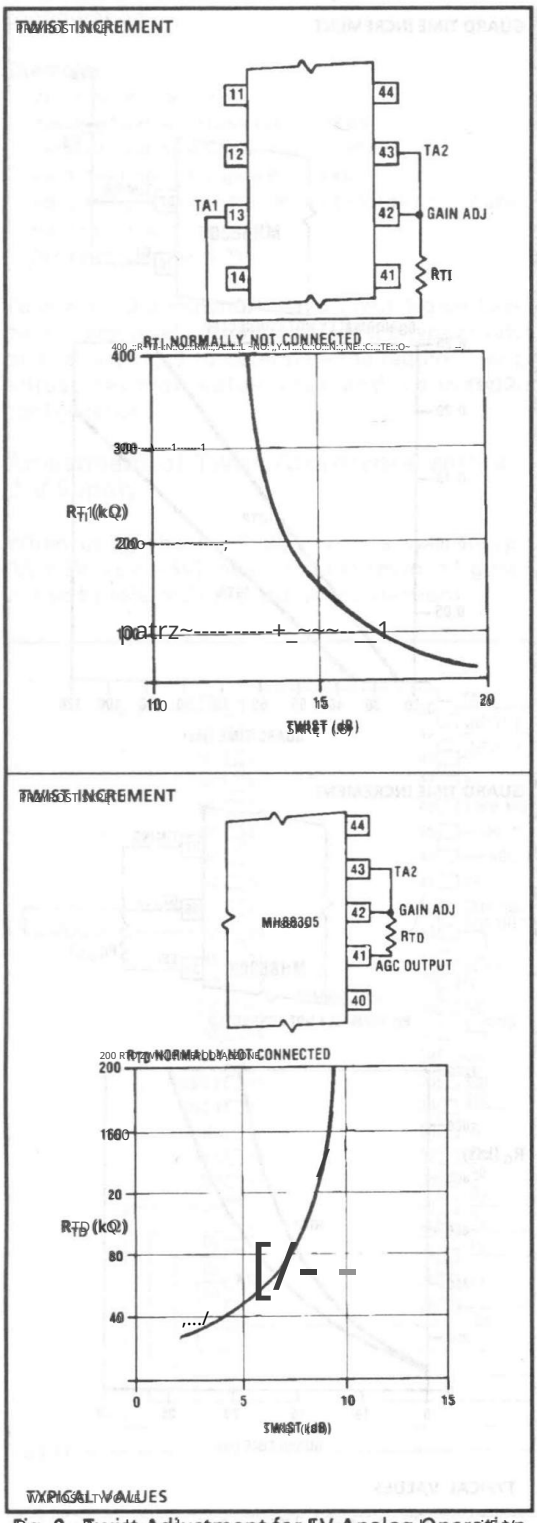

Fig. 9 - Twist Adjustment for 5V Analog Operation

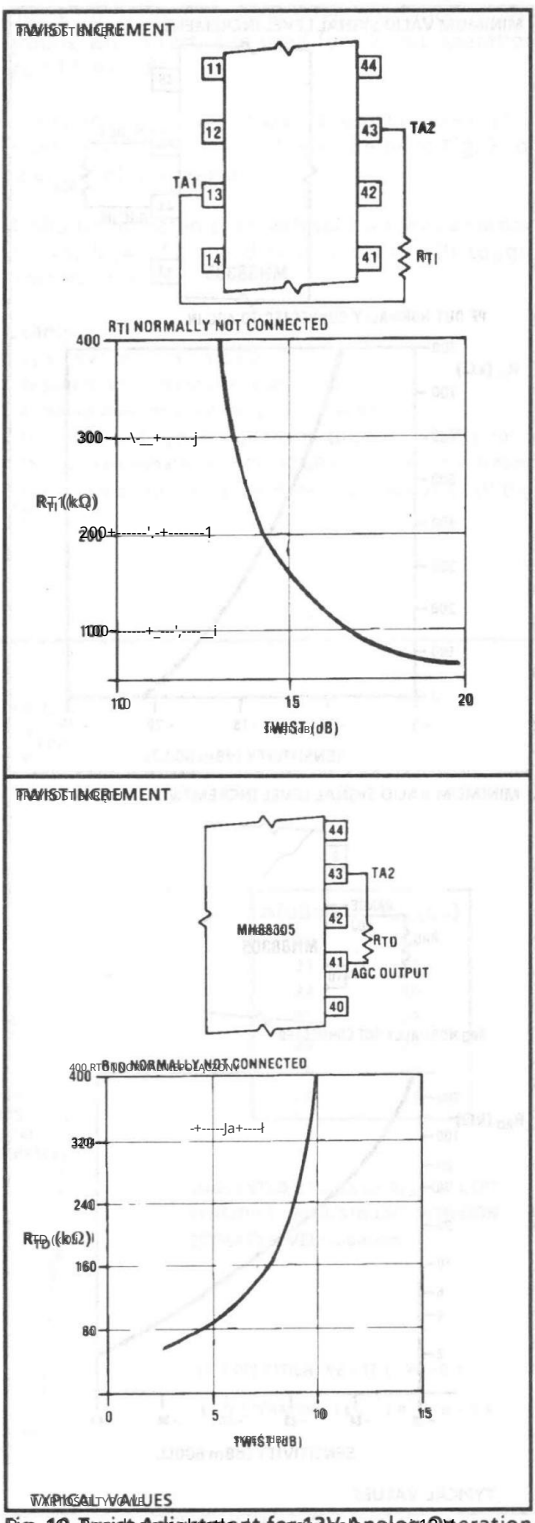

Fig. 10 - Twist Adjustment for 12V Analog Operation

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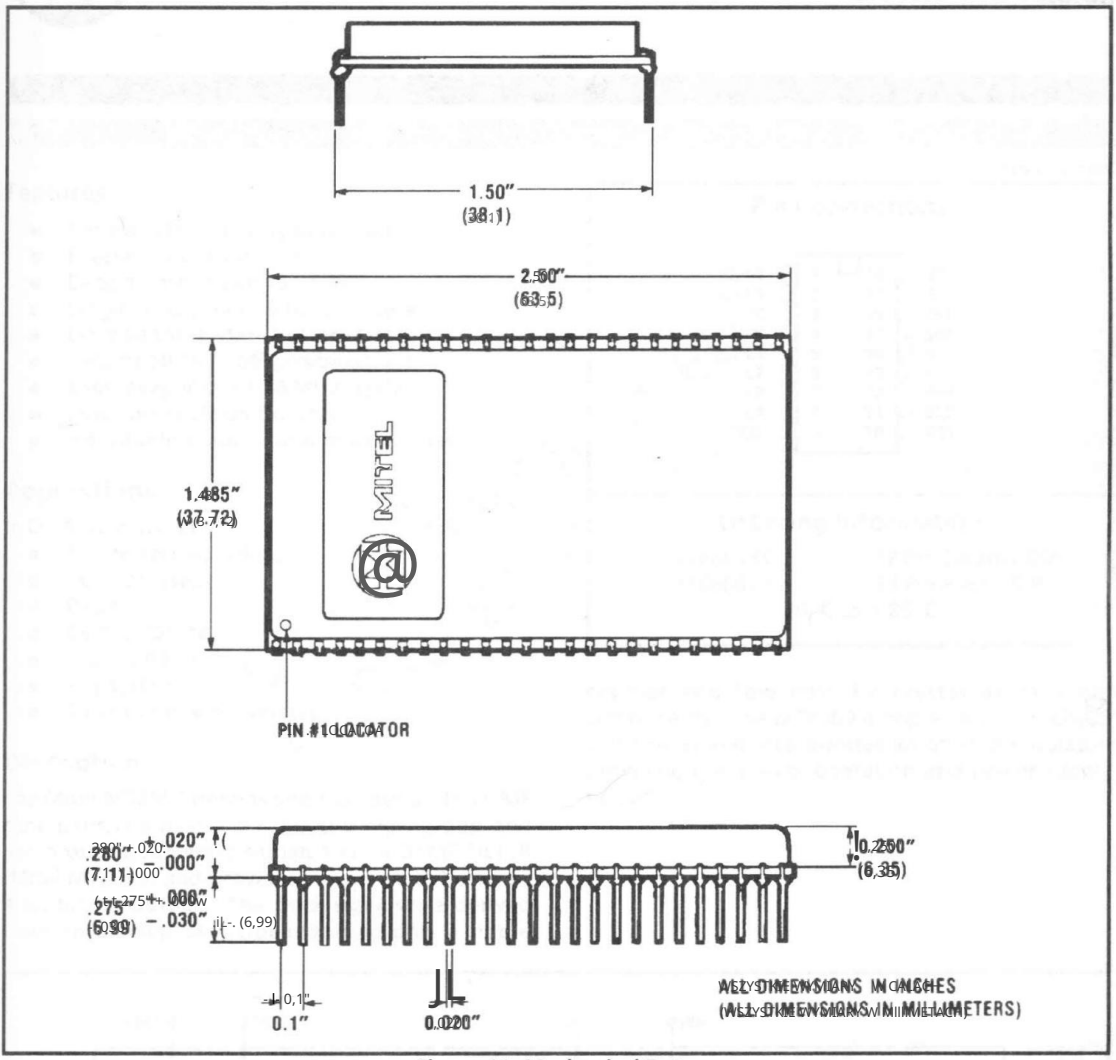

Figure 11 - Mechanical Data

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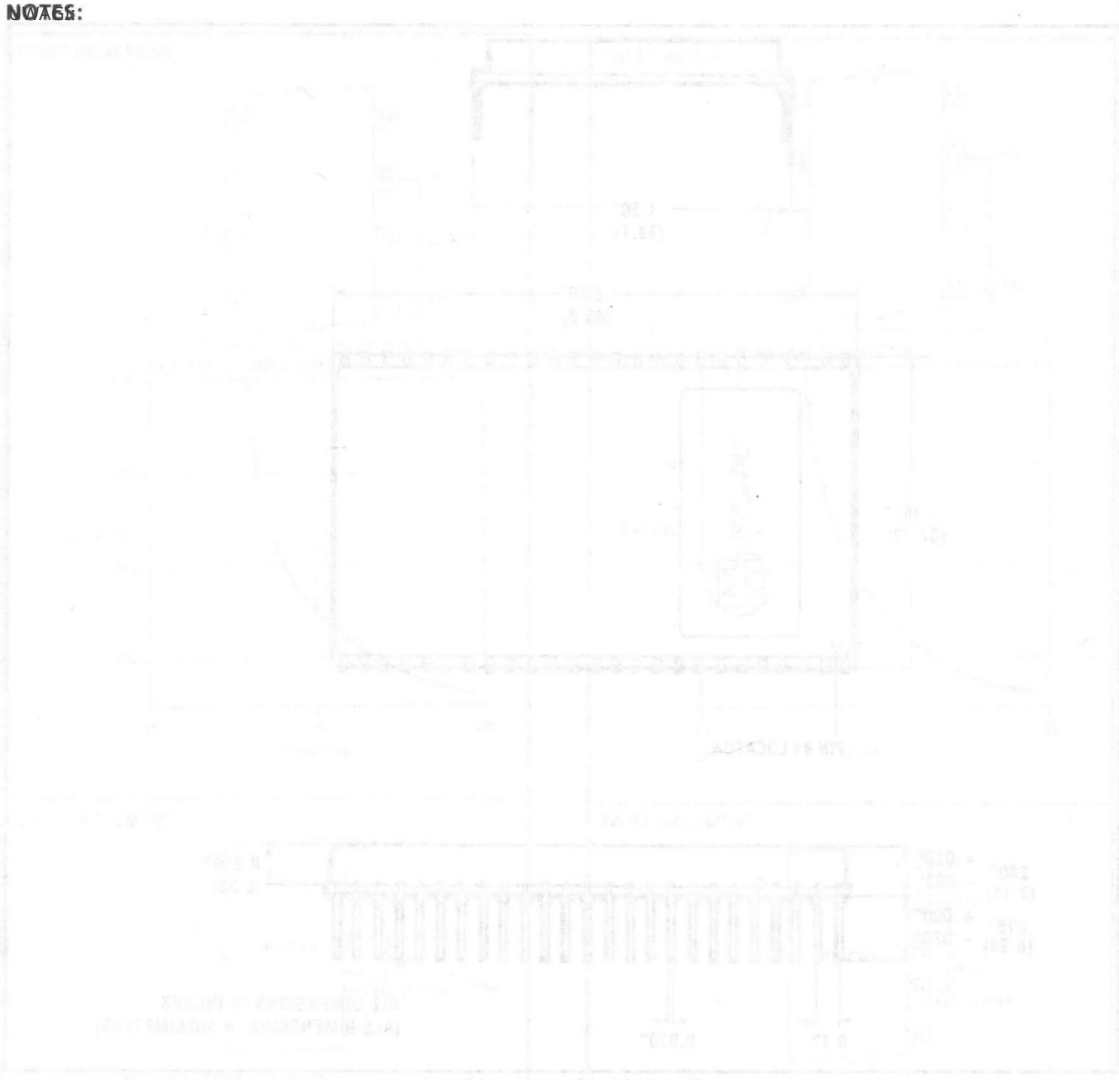
NOTES:



Machine Translated by Google

February 1985

Features

- Central Office quality detection
- Excellent voice talk-off
- Detects all 16 DTMF combinations
- Uses inexpensive 3.58 MHz crystal
- Low power CMOS circuitry
- Adjustable acquisition & release times

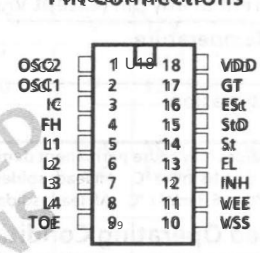
Applications

- DTMF Receivers For
  - End to end signalling
  - Control systems
  - PABX
  - Central Office
  - Mobile Radio
  - Key systems
  - Tone to pulse converters

Description

The Mitel MT8860 detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF FILTER (Mitel MT8865) and provides a three-state buffered 4 Bit binary output. The clock signals are derived from an on chip oscillator requiring only a single resistor and low cost TV crystal as external components. The MT8860 is implemented in CMOS technology and incorporates an on chip regulator, providing low power operation and power supply flexibility.

Pin Connections



Ordering Information

MT8860XC	18 Pin Ceramic DIP
MT8860XE	18 Pin Plastic DIP

-40 °C to +85 °C

NOT RECOMMENDED FOR NEW DESIGNS

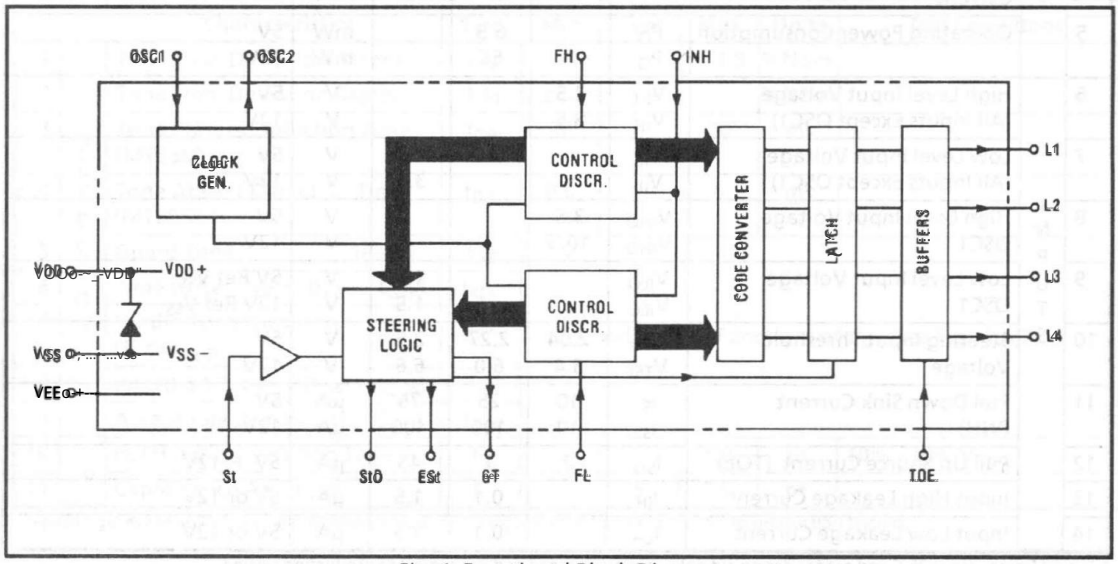


Fig. 1 Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne dopuszczalne wartości graniczne*

	Parameter	Symbol	Min	Max	Units
1	Voo - VEE			15	V
2	Voo - Vss (Zasilanie o niskiej impedancji)			5.5	V
3	Voltage on any pin except OS1, OSC2		VEE -0.3	VDD + 0.3	V
4	Napięcie na dowolnym pinie z wyjątkiem OS1, OSC2		Vss -0.3	VDD + 0.3	V
5	Max. Current at any pin (except VDD & VEE)	II		10	mA
6	Storage Temperature				
	Temperatura przechowywania	Package C Pakiet C	TSTG	-65	+150 °C
		Package E Pakiet E	TSTG	-65	+125 °C
7	Power Dissipation				
	Rozpraszanie mocy	Package C Pakiet C	PD	1000	mW
		Package E Pakiet E	PD	450	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Normalne działanie w tych warunkach nie jest gwarantowane.

① Derate above 75°C at 16 mW/°C. Leads soldered to board.
Obniżenie powyżej 75°C o 16 mW/°C. Przewody przylutowane do płytki.

② Derate above 25°C at 9.3 mW/°C. Leads soldered to board.
Obniżenie powyżej 25°C o 9,3 mW/°C. Przewody przylutowane do płytki.

Recommended Operating Conditions - All voltages referenced to V_{EE} unless otherwise stated

Zalecane warunki pracy - Wszystkie napięcia odniesienia do VEE, chyba że podano inaczej

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Power Supply Voltage (VDD-VEE)	VDD	4.75	5	5.25	V	Connections Fig. 5a
	Napięcie zasilania DC (VDD-VEE)	VDD	8		13	V	Connections Fig. 5b
2	Operating Temperature	TO	-45		+85	°C	
	Temperatura pracy						

‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
Typowe figury są w temperaturze 25°C i są tylko pomocą projektową, nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics - All voltages referenced to V_{EE}, Tamb = 25°C, f_c = 3.579545 MHz unless otherwise stated.

Charakterystyka elektryczna prądu stałego - Wszystkie napięcia odniesione do VEE, Tamb = 25°C, fc = 3,579545 MHz, chyba że podano inaczej

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Operating Supply Voltage (VDD-VEE)	VDD	4.75	5	5.25	V	Connections Fig. 5a
		Napięcie zasilania roboczego (VDD-VEE)	VDD	8		13	V	Connections Fig. 5b
2		Internal Logic Ground Voltage (VDD-VSS)	VDDSS	4.75		5.25	V	Connections Fig. 5a
		Logic wewnętrzny Napięcie dzielnika VDDSS (VDD-VSS)	VDDSS	6.0	6.5	7.5	V	IDD = 7mA
3		Operating Supply Current	IDD		1.3	4	mA	5V
		Prąd zasilania operacyjnego	IDD		2.5	5	mA	12V VDD - VSS = 5.5V
4		Internal Logic Ground Pin Current	ISS		5.5	6.7	mA	12V RSSEE = 900Ω
		Wewnętrzna logika Prąd uziemienia						
5		Operating Power Consumption	PD		6.5		mW	5V
		Moc pobierana podczas pracy	PD		66		mW	12V
6	INPUTS	High Level Input Voltage (All Inputs Except OSC1)	VIH	3.5			V	5V
		Wysoki poziom wejściowy Napięcie (wszystkie wejścia oprócz OSC1)	VIH	8.5			V	12V
7		Low Level Input Voltage (All Inputs Except OSC1)	VIL			1.5	V	5V
		Niski poziom wejściowy Napięcie (wszystkie wejścia oprócz OSC1)	VIL			3.5	V	12V
8		High Level Input Voltage OSC1	VIHO	3.5			V	5V
		Wysoki poziom wejściowy Napięcie OSC1	VIHO	10.5			V	12V
9		Low Level Input Voltage OSC1	VILO			1.5	V	5V Ref VSS
		Niski poziom wejściowy Napięcie OSC1	VILO			1.5	V	12V Ref VSS
10		Steering Input Threshold Voltage	VTSt	2.04	2.27	2.5	V	5V
		Sygnał sterujący Napięcie progowe	VTSt	5.4	6.0	6.6	V	12V
11		Pull Down Sink Current (INH)	ISI	10	25	75	µA	5V
		Prąd ściągający w dół (INH)	ISI	10	190	400	µA	12V
12		Pull Up Source Current (TOE)	ISO	2	7	45	µA	5V + 12V
		Prąd źródła podciągającego (TOE)						
13		Input High Leakage Current	IIH		0.1	1.5	µA	5V lub 12V
		Wejście wysoki prąd upływu						
14		Input Low Leakage Current	ILL		0.1	1.5	µA	5V lub 12V
		Wejście niskiego prądu upływu						

‡ Typical parameters are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
Wartości parametrów typowe w temperaturze 25°C służą jedynie do projektowania, nie są gwarantowane i nie podlegają testom produkcyjnym.

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DC Electrical Characteristics (cont'd) All voltages referenced to V_{EE}, T_A = 25°C, f = 3.579545 MHz, unless otherwise stated.

(cd) Wszystkie napięcia odnoszą się do V_{EE}, T_A = 25°C, f = 3,579545 MHz, chyba że podano inaczej.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
15	O U T P U T S	High Level Output Voltage (All Outputs Except OSC2)	V_{OH}	4.9			V	5V
			V_{OH}	11.9			V	12V
16		Low Level Output Voltage (All Outputs Except OSC2)	V_{OL}			0.1	V	5V
			V_{OL}			0.1	V	12V
17		High Level Output Voltage OSC2	V_{OHO}	4.9			V	5V
				11.9			V	12V
18		Low Level Output Voltage OSC2	V_{OL}			0.1	V	5V Ref V_{SS}
			V_{OL}			0.1	V	12V Ref V_{SS}
19		Output Drive Current P Channel Source (All Outputs Except OSC2)	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.6V
			I_{OH}	0.5	0.8		mA	12V V_{OH} = 11.5V
20		Output Drive Current N Channel Sink (All Outputs Except OSC2)	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.4V
			I_{OL}	1.0	1.6		mA	12V V_{OL} = 0.5V
21		Output Drive Current - OSC2 P Channel Source	I_{OH}	90	120		µA	5V V_{OH} = 4.6V
			I_{OH}	90	120		µA	12V V_{OH} = 11.5V
22		Output Drive Current - OSC2 N Channel Sink	I_{OL}	100	160		µA	5V V_{OL} = 0.4V
			I_{OL}	100	160		µA	12V V_{OL} = 0.5V
23		Tristate Output Current (High Impedance State) $L1{\cdot}L4 = H$ $L1{\cdot}L4 = L$ $L1{\cdot}L4 = H$ $L1{\cdot}L4 = L$	I_{OZ}		0.035	1.5	µA	5V Apply V_{OL} = 0V
			I_{OZ}		0.1	1.5	µA	5V Apply V_{OH} = 5V
			I_{OZ}		0.1	1.5	µA	12V Apply V_{OL} = 0V
			I_{OZ}		0.3	1.5	µA	12V Apply V_{OH} = 12V

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Typy kalkulacji wynoszą 25°. Podane wartości służą jedynie do celów pomocy projektowej: nie są gwarantowane i nie podlegają testom produkcyjnym.

Test Conditions: 5V: V_{DD} = 5V, V_{EE} = 0V, V_{SS} = 0V, Voltages as Fig. 5a, 12V: V_{DD} = 12V, V_{EE} = -12V, V_{SS} = 0V, Connection as Fig. 5b

Warunki testowe: 5V: V_{DD} = 5V, V_{EE} = 0V, V_{SS} = 0V, napięcia jak na rys. 5a, 12V: V_{DD} = 12V, V_{EE} = -12V, V_{SS} = 0V, Połączenie jak na rys. 5b

For Input current parameters only $V_{IH} = V_{DD}$, $V_{OO} = V_{DD} - V_{EE}$, $V_{SS} = V_{SS}$

Tylko dla parametrów prądu wejściowego $V_{IH} = V_{DD}$, $V_{OO} = V_{DD} - V_{EE}$, $V_{SS} = V_{SS}$

AC Electrical Characteristics V_{DD} = 5V, T_A = 25°C, f = 3.579545 MHz, unless otherwise stated.

Charakterystyka elektryczna prądu przemiennego V_{DD} = 5V, T_A = 25°C, f = 3,579545 MHz, chyba że podano inaczej.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	D E T E C T O R	Tone Freq. Deviation Accept	Δf_{TA}			±2.5	% Nom.	
		Odchylenie częstotliwości tonu akceptowanie				±2,5 nominalnej		
2		Tone Freq. Deviation Reject	Δf_{TR}	±3.5			% Nom.	
		Odrzucenie odchylenia częstotliwości tonu						
3		Tone Present Detection Time (MT8860X)	t_{DP}	6		10	ms	
		Czas wykrywania obecności tonu (MT8860X)						
4		Tone Absent Detection Time (MT8860X)	t_{DA}	0.6		6	ms	
		Czas wykrycia braku sygnału T (MT8860X)						
5		Guard Time (Period A)	t_{GT}	Adjustable Functions of t_{GT} - See Figs. 2,6,7.				
		Czas straży (Okres A)		Regulowane funkcje t_{GT} - patrz rys. 2,6,7.				
6		Time to Receive = (t_{DP} + t_{GTP})	t_{REC}					
		Czas odbioru = (góra + t_{GTP})						
7		Invalid Tone Duration (If not t_{REC})	t_{REC}					
	R	Nieprawidłowy czas trwania tonu (Jeśli nie t_{REC})						
8		Interdigit Pause = (t_{DA} + t_{GTA})	t_{ID}					
		Pauza międzycyfrowa = (t_{DA} + t_{GTA})						
9		Acceptable Dropout (If not t_{ID})	t_{DO}					
		Dopuszczalne porzucenie (Jeśli nie t_{ID})						
10	I/P	FL FH Input Transition Time	t_{IT}			1.0	µs	10% - 90% V_{DD}
		Czas przejścia wejściowego FL-FH						10% - 90% V_{DD}
11		Capacitance Any Input	C		5	7.5	pF	
		Pojemność dowolne wejście						

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Typowe wartości liczbowe wynoszą 25°. Podane wartości służą wyłącznie do celów projektowych: nie są gwarantowane i nie podlegają testom produkcyjnym.

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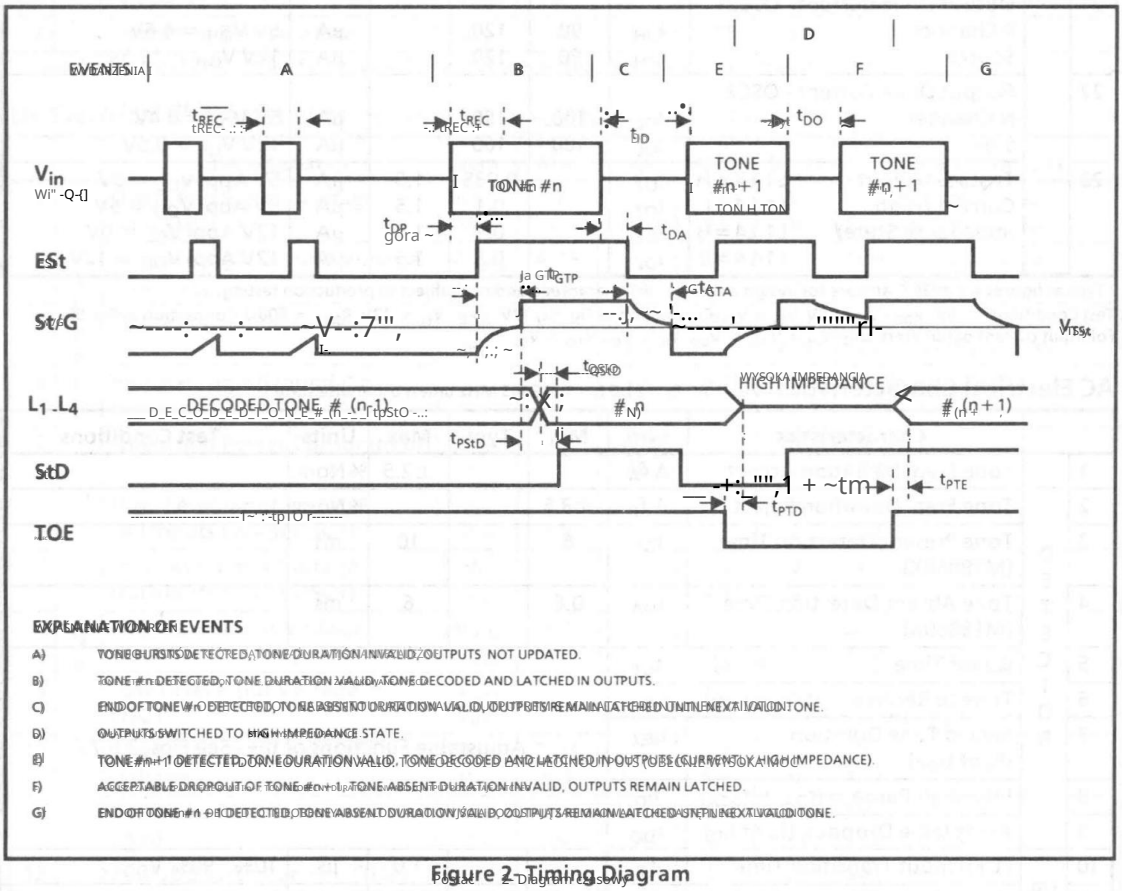
AC Electrical Characteristics cont'd

Ciąg dalszy charakterystyk elektrycznej prądu przemiennego - V_{DD} = 5V, T_A = 25°C, f_c = 3.579545 MHz, chyba że podano inaczej. otherwise stated.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
12	OUTPUTS	Propagation Delay St to L_1-L_4	t_{PL}		8	11	µs	V_{DD}=5V or 12V
13		Propagation Delay St to StD	t_{PStD}		12	14	µs	V_{DD}=5V or 12V
14		Sync. Delay L_1-L_4 to StD	t_{LStD}		3.43		µs	V_{DD}=5V or 12V
15		Propagation Delay TOE to L_1-L_4 Enable	t_{PTE} t_{PTE}		300 200		ns ns	V_{DD} 5V V_{DD} 12V
16		Propagation Delay TOE to L_1-L_4 Disable	t_{PTD} t_{PTD}		300 200		ns ns	V_{DD} 5V V_{DD} 12V
17	CLOCK	Crystal/Clock Frequency	f_c	3.5759	3.5795	3.581	MHz	OSC1 OSC2
18		Clock Input (OSC 1) Rise Time	t_{LHCl}			110	ns	10%-90%
		Fall Time	t_{HLCl}			110	ns	V_{DD}-V_{SS}
		Duty Cycle	DC_{Cl}	40	50	60	%	Externally Applied Clock
19		Clock Output (OSC 2) Capacitive Load	C_{LO}			30	pF	

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

†Typowe parametry zakłóceń w 25°C służą wyłącznie celom projektowym i nie są gwarantowane ani podlegają testom produkcyjnym.



EXPLANATION OF EVENTS

A) TONE BURST DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS.

C) END OF TONE #n DETECTED, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENT HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

Figure 2 - Timing Diagram

Rysunek 2 - Diagram czasowy

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Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DTMF	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
	*	H	H	L	H	H
	#	H	H	H	L	L
D	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

Fig. 3a) Output Coding

Detected Character	INH	ESt
None	0	L
X	L	H
DTMF	H	H
D	H	L

Fig. 3b) Inhibit Function

ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

Fig. 3c) Steering

*Delayed wrt St.

For the purpose of these Tables consider:

Logic LOW (L)

Logic HIGH (H)

H = LOGIC HIGH L = LOGIC LOW

0 = DON'T CARE LOGIC HIGH OR LOW

Z = HIGH IMPEDANCE X = DON'T CARE CHARACTER

Fig. 3 Coding Tables

Pin Description

Pin #	Name	Description
1	OSC2	Clock Output.
2	OSC1	Clock Input. A 3.579545MHz crystal with parallel 5M resistor connected between this pin and OSC2 completes the internal oscillator circuit.
3	IC	Internal Connection. For testing only. Must be left open circuit.
4	FH	High Frequency Group Input. Accepts single rectangular wave high group tone from DTMF filter.
5,6, 7,8	L1,L2, L3,L4	Data Output, Three-state Buffered. Provides 4 bit binary word corresponding to the tone pair decoded, when enabled by TOE. See Fig. 3 for state table.
9	TOE	Three-state Output Enable Input. Logic high on this input enables outputs L1-L4. Internal pull-up.
10	V_{SS}	Internal Logic Ground. For $V_{DD} - V_{SS} = 5V$, V_{SS} connected to V_{EE}. For $V_{DD} - V_{EE} > 8V$, V_{SS} connected via resistor to V_{EE}, see Fig. 5.
11	V_{EE}	Negative Power Supply. External logic ground.
12	INH	Inhibit Input. Logic high inhibits detection of tones representing characters A, B, C, D, #, *. Internal pull-down.
13	FL	Low Frequency Group Input. Accepts single rectangular wave low group tone from DTMF filter.
14	St	Steering Input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and update the contents of the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. See Fig. 3c and Functional Description.
15	StD	Delayed Steering Output. Presents a logic high when a valid tone pair has been received. Returns to logic low when St detects an absence of tones.
16	ESt	Early Steering Output. Presents a logic high immediately after the digital algorithm detects a recognizable tone pair. Any momentary loss of the incoming tone or excessive distortion will cause ESt to return to a logic low.
17	GT	Guard Time Output. Three-state output. Normally connected to St, is used in the steering algorithm and controls functions of St and ESt (See Fig. 3c).
18	V_{DD}	Positive Power Supply.

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Functional Description

The Mitel MT8860 is a CMOS Digital DTMF Detector and Decoder. Used in conjunction with a suitable DTMF filter (Mitel MT8865) it can detect and decode all 16 standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MT8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group of the composite dual tone signal and limit the resulting pair of sine wave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The High Group and Low Group rectangular waves are applied to the MT8860's FH and FL inputs respectively. Mitel's MT8865 DTMF Filter provides these functions.

Within the MT8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators Fig. 1) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both High Group and Low Group signals have been simultaneously detected a flag ESt (Logic High) is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig. 2) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk-off performance of the system. The check also imposes a minimum period of "tone absent" before a valid received tone is recognized as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig. 7a) is charged via resistor R from ESt when a DTMF tone pair is detected. After a period t_{GTP}, V_c exceeds the St input threshold voltage V_{TSt} setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. This mode of operation is shown by the steering state table (Fig 3c) and timing diagram (Fig. 2).

Internally the presence of the ESt flag allows the Control/Discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L1-L4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_c (Fig. 7a) falling below V_{TSt}.

Increasing the "time to receive" t_{REC} tends to further improve "talk off" performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing the interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal-to-noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig. 7.

When L1-L4 are connected to a data bus TOE may be controlled by external circuitry, or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MT8860 may be supplied from either a 5 volt or 8 to 13 volt supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig. 5.

When using the MT8860 with the MT8865 DTMF Filter it is only necessary to use the MT8865 crystal oscillator (see Fig. 6). When using the higher supply voltage range the 8865 OSC2 output should be capacitively coupled to the 8860 OSC1 input as shown in Fig. 6.

Where it is desirable to receive only the DTMF digits taking INH to a logic high inhibits detection of the # * ABCD DTMF characters. This also further improves "talk off" performance due to the reduced number of detectable tones.

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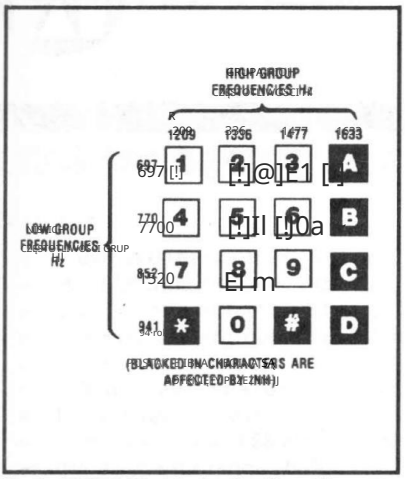

Fig. 4 - DTMF Matrix Indicating Character Tone Pair Correspondence

Rys.4 - Macierz DTMF wskazująca zgodność par znaków tonowych

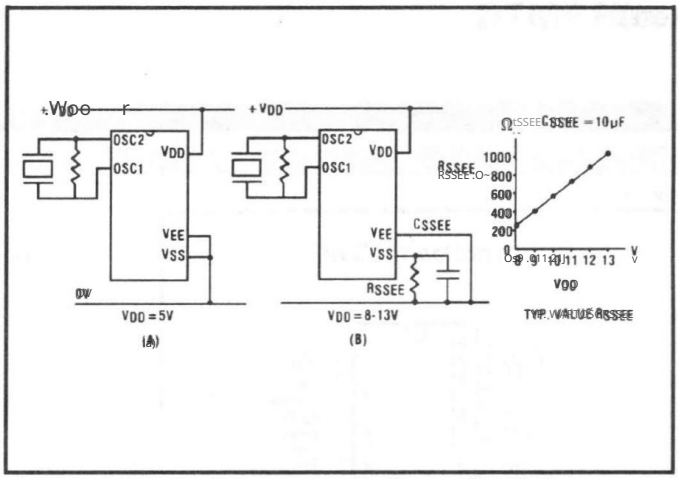

Fig. 5 - Power Supply Connection Options

Rys. 5 - Opcje podłączenia zasilania

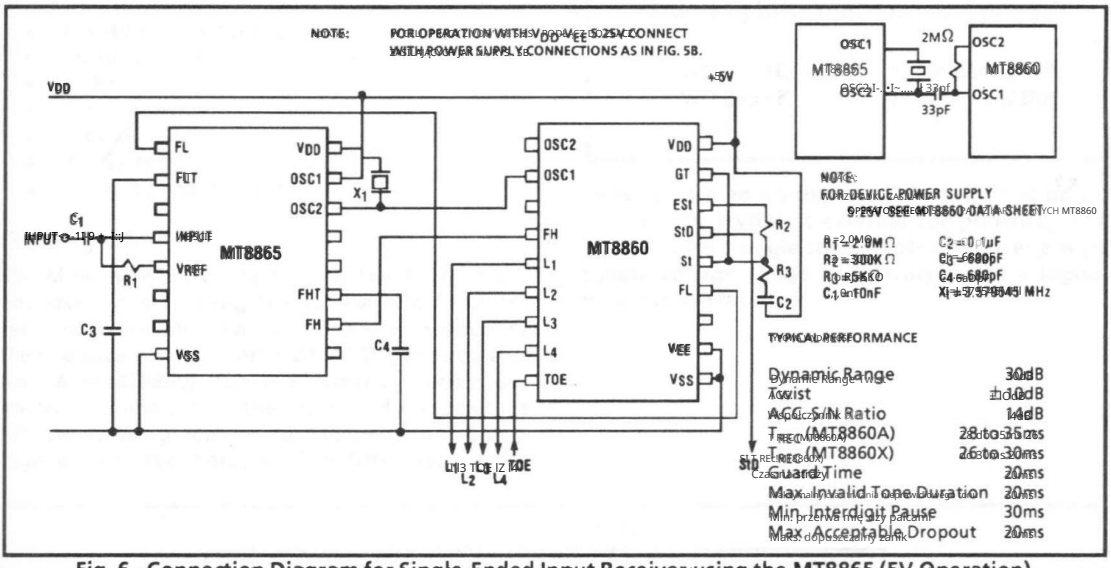

Fig. 6 - Connection Diagram for Single-Ended Input Receiver using the MT8865 (5V Operation)

Rys. 6 - Schemat połączeń odbiornika wejściowego Single-Ended z wykorzystaniem MT8865 (zasilanie 5 V)

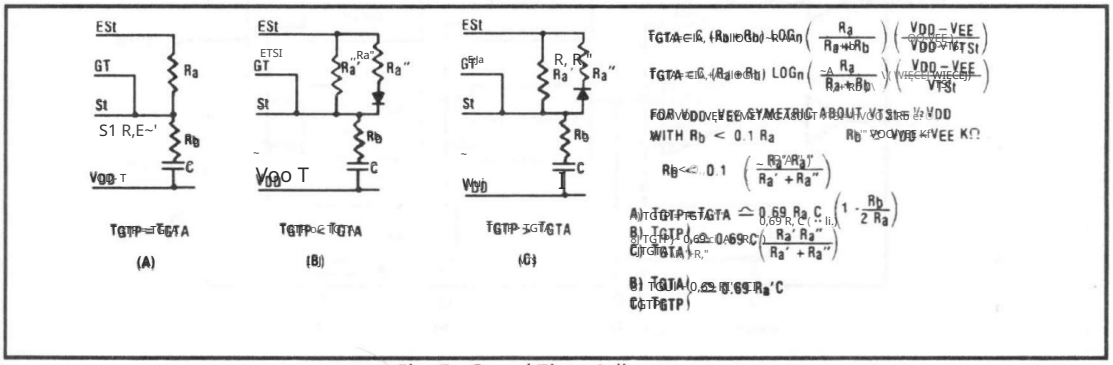

Fig. 7 - Guard Time Adjustment

Rys. 7 - Regulacja czasu ochrony

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NOTES:

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Features

- Provides DTMF high and low group filtering
- Hard limiting on filter outputs
- 6 pole bandpass high and low group filters
- 40 dB (typ) inter group attenuation
- Dial tone suppression
- 5 to 12V single supply operation
- Logical powerdown
- Uses inexpensive 3.58 MHz crystal
- Wide dynamic range 30dB

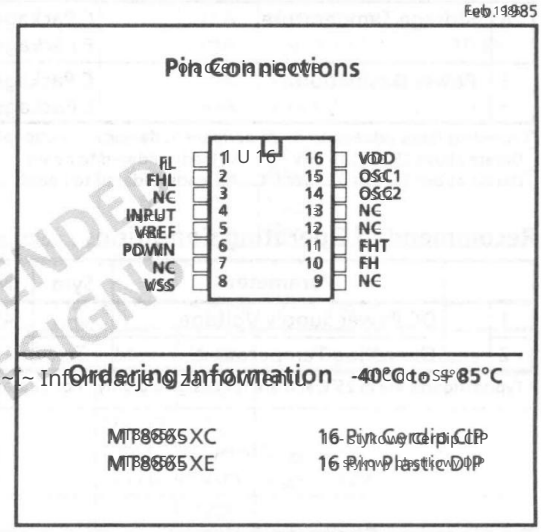
Applications

- DTMF Receivers For
  - End to end signalling
  - Control systems
  - PABX
  - Central Office
  - Mobile Radio
  - Key systems
  - Tone to pulse converters

Description

The Mitel MT8865 contains both high and low group filters and comparator functions required to implement a Dual Tone Multi Frequency (DTMF) receiver. To complete a Mitel DTMF Digital Detector (Mitel MT8860) switched capacitor techniques are used for the filters and oscillator frequency derived from an inexpensive 3.58 MHz crystal. The MT8865 is fabricated using Mitel's double poly ISO²-CMOS high density technology. Power consumption is low and the filter clocks are derived from an on chip oscillator requiring only a low cost TV crystal. The MT8865 operates from a single supply of 5 to 12 volts. The MT8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

Pin Connections



Ordering Information

MT8865XC	16 Pin Ceramic DIP
MT8865XE	16 Pin Plastic DIP

-40°C to +85°C

NOT RECOMMENDED FOR NEW DESIGN

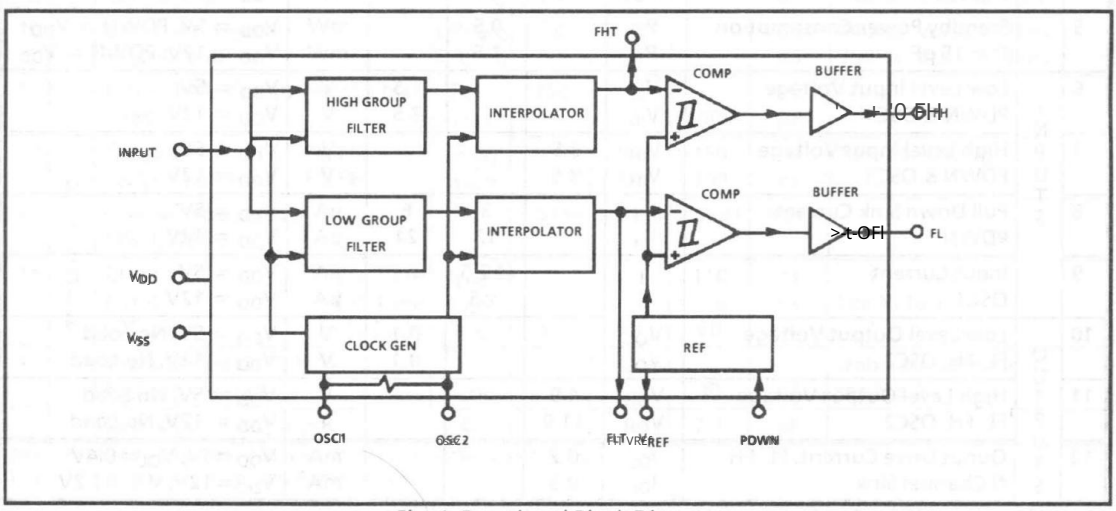


Fig. 1 Functional Block Diagram

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Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	VDD - VSS			15	V
2	Voltage on any pin except OS1, OSC2		VEE - 0.3	VDD + 0.3	V
3	Max. Current at any pin	II		10	mA
4	Storage Temperature — J Package	TSTG	-65	+150	°C
	— P Package	TSTG	-65	+125	°C
5	Power Dissipation — J Package①	PD		850	mW
	— P Package②	PD		400	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

① Derate above 75 °C at 16 mW/°C. All leads soldered to board.

② Derate above 25 °C at 8.3 mW/°C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (VSS) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Power Supply Voltage	VDD	4.75		13	V	
2	Operating Temperature	TO	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (VSS) unless otherwise stated, TA = 25°C, fc = 3.579545 MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Operating Supply Voltage	VDD	4.75			V	VDD = 5V
			VDD			13	V	VDD = 12V
2		Operating Supply Current	IDD		1.2	3	mA	VDD = 5V, PDWN = VSS
			IDD		5	10	mA	VDD = 12V, PDWN = VSS
3		Standby Supply Current	IDDS		70	100	µA	VDD = 5V, PDWN = VDD
			IDDS		300	500	µA	VDD = 12V, PDWN = VDD
4		Operating Power Consumption Fig. 5(c)	PO		6		mW	VDD = 5V, PDWN = VSS
			PO		60		mW	VDD = 12V, PDWN = VSS
5		Standby Power Consumption C = 15 pF	PS		0.5		mW	VDD = 5V, PDWN = VDD
			PS		1.5		mW	VDD = 12V, PDWN = VDD
6	INPUTS	Low Level Input Voltage PDWN & OSC1	VIL			1.5	V	VDD = 5V
			VIL			3.5	V	VDD = 12V
7		High Level Input Voltage PDWN & OSC1	VIH	3.5			V	VDD = 5V
			VIH	8.5			V	VDD = 12V
8		Pull Down Sink Current PDWN	IIH		3	6	µA	VDD = 5V
			IIH		12	24	µA	VDD = 12V
9		Input Current OSC1	II		±2.5		µA	VDD = 5V
			II		±6		µA	VDD = 12V
10	OUTPUTS	Low Level Output Voltage FL, FH, OSC2	VOL			0.1	V	VDD = 5V, No Load
			VOL			0.1	V	VDD = 12V, No Load
11		High Level Output Voltage FL, FH, OSC2	VOH	4.9			V	VDD = 5V, No Load
			VOH	11.9			V	VDD = 12V, No Load
12		Ouput Drive Current, FL, FH N-Channel Sink	IOL	0.2			mA	VDD = 5V, VOL = 0.4V
			IOL	0.5			mA	VDD = 12V, VOL = 1.2V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

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DC Electrical Characteristics (Cont'd)

Charakterystyka elektryczna prądu stałego (cd.) - Napięcia podano w odniesieniu do uziemienia (Vss), TA = 25°C, f = 3,579545 MHz, chyba że określono inaczej.

Voltages are with respect to ground (V_{ss}), $T_A = 25°C$, $f_c = 3.579545$ MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
13	OUTPUTS	Output Drive Current OSC2, N Channel Sink Prąd wyjściowy napędu OSC2, kanał spustowy ONZ	I_{OL} I_{OL}	0,1 0,25			mA mA	V_{DD} = 5V, V_{OL} = .4V V_{DD} = 12V, V_{OL} = 1.2V
14		Output Drive Current, FL, FH P Channel Source Prąd wyjściowy napędu FL, FH źródło kanału typ	I_{OH} I_{OH}	0,2 0,5			mA mA	V_{DD} = 5V, V_{OH} = 4.6V V_{DD} = 12V, V_{OH} = 10.8V
15		Output Drive Current, OSC2, P Channel Source Prąd wyjściowy napędu do OSC2, kanał źródła	I_{OH} I_{OH}	0,1 0,25			mA mA	V_{DD} = 5V, V_{OH} = 4.6V V_{DD} = 12V, V_{OH} = 10.8V
16		Output Voltage, V_{Ref} Napięcie wyjściowe, V_{Ref}	V_{Ref} V_{Ref}	2,3 5,4		2,6 6,2	V V	V_{DD} = 5V, bez obciążenia V_{DD} = 12V, bez obciążenia
17		Output Resistance, V_{Ref} Rezystancja wyjściowa, V_{Ref}	R_{OUT} R_{OUT}			16 8	kΩ kΩ	V_{DD} = 5V V_{DD} = 12V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Podane wartości współczynnika sprawności wynoszą 25°C, mają one jedynie charakter pomocniczy przy projektowaniu, nie są gwarantowane i nie podlegają testom produkcji.

AC Electrical Characteristics

Charakterystyka urządzenia AC Electrical - Napięcia odnoszą się do masy (Vss), TA = 25°C, f = 3,579545, V_{DD} = 4,75 - 13V.

Voltages are with respect to ground (V_{ss}), $T_A = 25°C$, $f_c = 3.579545$, $V_{DD} = 4.75$ - 13V.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	FILTER	Dynamic Range Zakres Dynamiki		30		36	dB	
2		Valid Input Signal Levels (Each tone of composite signal) Prawidłowe poziomy sygnału wejściowego (Każdy ton sygnału złożonego)		27 670		$V_{DD}/2\sqrt{2}$ 883 mVrms 2120 mVrms	V_{pp} mVrms V_{DD} = 5V mVrms V_{DD} = 12V	
3		Input Impedance Impedancja wejściowa	Z_{IN}	10			MΩ	
4		Passband Ripple Tętnienie pasma przepustowego	A_{PR}		±0.3	±1.0	dB	Zobacz uwagę See Note 1
5		Low Group Lower Limit 1dB Bandwidth Upper Limit Niska Grupa dolny limit 1dB Pasmo przenoszenia górny limit	f_{LL} f_{LU}	670 958	697 941	684 924	Hz Hz	
6		High Group Lower Limit 1dB Bandwidth Upper Limit Wysoka grupa dolny limit 1dB pasmo przenoszenia górny limit	f_{HL} f_{HU}	1162 1660	1209 1740	1188	Hz Hz	
7		Intergroup Rejection Low Group with High Tone Międzygrupowe tłumienie zakłóceń Grupa niska z wysokim tonem	IR_{LH1209} IR_{LH1477}	34 36	45 40		dB dB	1209Hz w.r.t. 770Hz 1477Hz w.r.t. 770Hz
8		Intergroup Rejection High Group with Low Tone Międzygrupowe tłumienie zakłóceń Grupa wysoka z niskim tonem	IR_{HL941} IR_{HL770}	38 36	50 40		dB dB	941Hz w.r.t. 1336Hz 770Hz w.r.t. 1336Hz
9		Dial Tone Rejection Low Group Odrzucanie sygnału wybierania Grupa niska	DR_{L440} DR_{L350}	40 28	60 30		dB dB	440Hz w.r.t. 770Hz 440Hz w.r.t. 770Hz
10		Dial Tone Rejection High Group Odrzucanie sygnału wybierania Grupa wysoka	DR_{H440} DR_{H350}	52 50	60 55		dB dB	440Hz w.r.t. 1336Hz 350Hz w.r.t. 1336Hz
11		FHT FLT Maximum Permissible Load Pojemność maksymalna dopuszczalna	R_{FLFT} C_{FLFT}	250		1000	kΩ pF	
12	CLOCK	Output Rise Time FL, FH Czas narastania sygnału wyjściowego FL, FH Output Fall Time FL, FH Czas opadania sygnału wyjściowego FL, FH	t_{THO} t_{THO}		90 60	150 100	ns ns	10% do 90% V_{DD}
13		Crystal/Clock Freq. Częstotliwość kryształu/kryształu OSC1, OSC2	f_c	3,5759	3,5795	3,5831	MHz	Zakres wartości 3,5759, 3,5795, 3,5831 MHz
14		Clock Input (OSC1) Godzina Wejście (OSC1) Rise Time Czas narastania Fall Time Czas opadania Duty Cycle Współczynnik wypełnienia	t_{LHCI} t_{HLCI} DC	40	50	110 110 60	ns ns %	Zobacz uwagę See Note 2
15		Clock Output OSC 2 Capacitive Load Wyjście zegara OSC 2 Obciążenie pojemnościowe	C_{LOC}			30	pF	Niezrównoważone obciążenie zobacz rys. 5 see Fig. 5
16		Capacitance Any Input Pojemność Dowolne wejście	C_{IN}		5	7.5	pF	

Note 1: Passband ripple measured with respect to a passband gain of 0 dB ± 1dB.
Uwaga 1: Pasmo przepustowe mierzone w odniesieniu do pasma przepustowego 0 dB ± 1 dB.
Note 2: 10% to 90% V_{DD} Externally Applied Clock.
Uwaga 2: 10% do 90% V_{DD} zewnętrznie zastosowany zegar.

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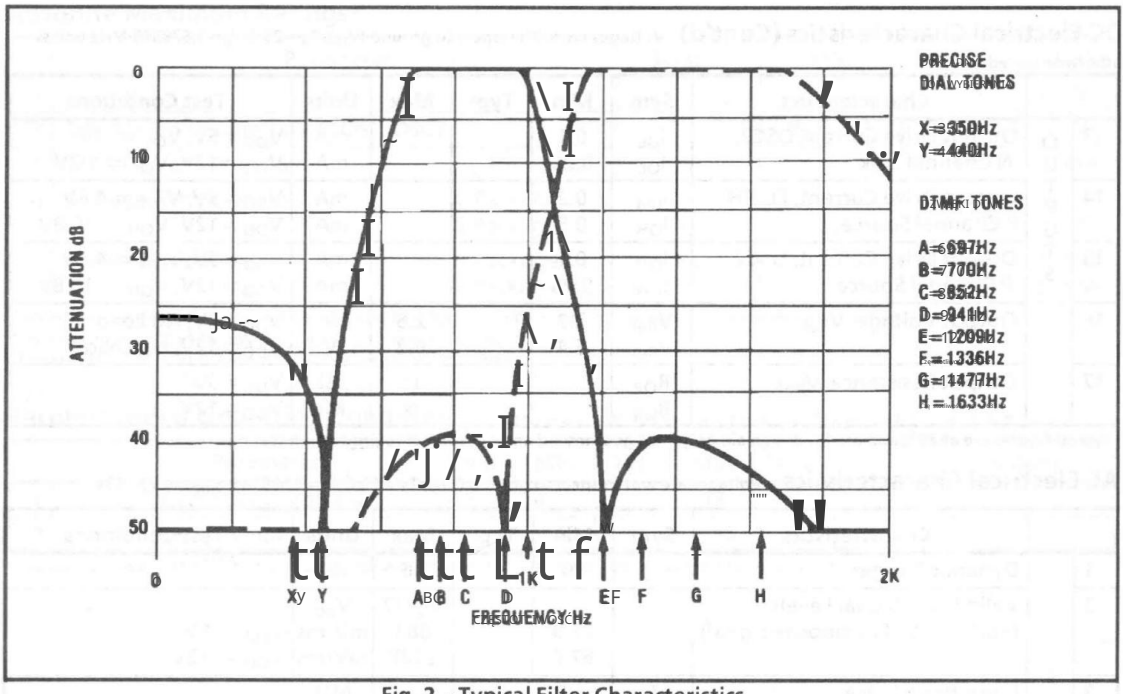

Fig. 2 - Typical Filter Characteristics

Rys. 2 Typowe krzywe filtra

Pin Description

Pin Description

Pin #	Name	Description
1	FL	Low Group Limiter Output.
2	FLT	Test Output. Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.
3	NC	Not Connected.
4	INPUT	Tone Signal Input (single ended).
5	V_{ref}	Internal Reference. Can be used to bias input via 2MΩ resistor.
6	PDWN	Power Down Active High. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.
7	NC	Not Connected.
8	V_{SS}	Negative (0V) Power Supply.
9	NC	Not Connected.
10	FH	High Group Limiter Output.
11	FHT	Test Output. Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.
12	NC	Not Connected.
13	NC	Not Connected.
14	OSC2	Clock Output.
15	OSC1	Clock Input. 3.579545 MHz crystal connected between this pin and OS2 completes the internal oscillator circuit.
16	VDD	Positive Power Supply.

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Functional Description

The MT8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of the DTMF Digital Decoder (MT8860). See Fig. 3.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig. 2) also incorporates a notch at 440Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting. The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MT8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig. 3) or via a differential buffer to a telephone line (Fig. 4). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input

Układ MT8865 zadziela komponenty grupy wysokiej i niskiej sygnału dwutonowego i ogranicza powstałą parę fal sinusoidalnych, aby wytworzyć fale prostokątne o takich samych częstotliwościach jak pojedyncze tony wejściowe. Te ograniczone tony grupy niskiej i wysokiej pojawiają się odpowiednio na wyjściach FL i FH. Aby zaimplementować kompletny odbiornik DTMF, wyjścia FL i FH są podłączone do wejść FL i FH cyfrowego dekodera DTMF (MT8860). Zobacz rys. 3.

Rozdzielenie tonów grupy niskiej i wysokiej uzyskuje się poprzez równoczesne doprowadzenie sygnału dwutonowego do wejść dwóch filtrów pasmowo-przepustowych z przełączanymi kondensatorami szóstego rzędu, szerokość pasm

z których odpowiadają pasmom obejmującym tony grupy niskiej i wysokiej. Charakterystyka częstotliwościowa każdego filtra (patrz rys. 2) jest również wcięta przy 440 Hz, aby zapewnić odrzucenie sygnału wybierania. Po każdym wyjściu filtra następuje sekcja przełączanego kondensatora pojedynczego rzędu, która działa jako interpolator wygładzając sygnały przed ograniczeniem. Funkcje ograniczające są wykonywane przez komparatory o wysokim wzmocnieniu, które są wyposażone w histerezę, aby zapobiec wykrywaniu niepożądanych sygnałów niskiego poziomu i szumów. Wyjścia komparatora są buforowane, aby sterować pinami wyjściowymi FL i FH oraz wejściami urządzenia wykrywającego. MT8865 ma wejście jednostronne, umożliwiające podłączenie do dekodera PCM, odbiornika radiowego (rys. 3) lub przez bufor różnicowy do linii telefonicznej (rys. 4). Wejście sygnału (pin 4) powinno mieć ustawione napięcie przy $V_{DD}/2$. Przy

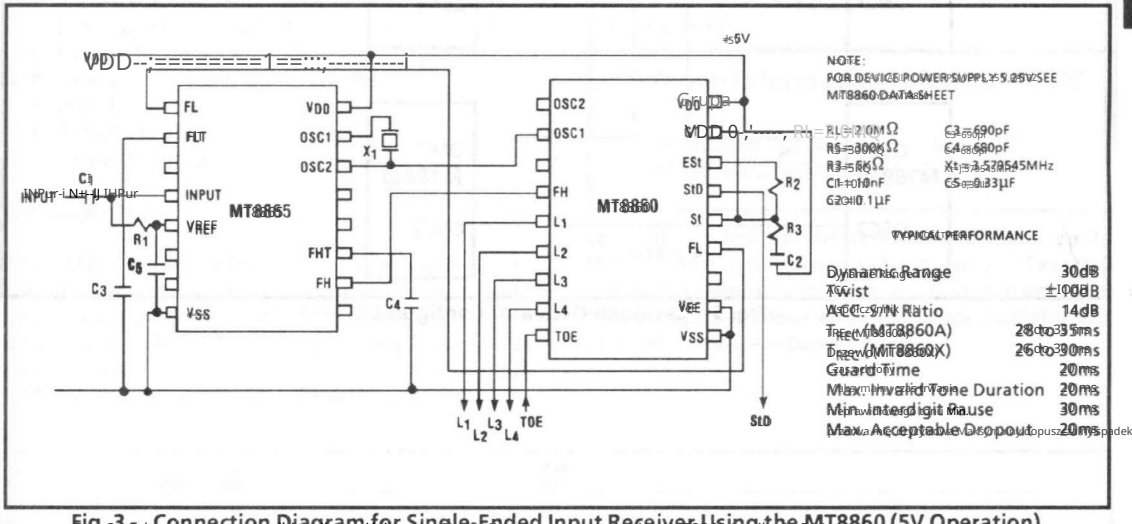

Fig. 3 - Connection Diagram for Single Ended Input Receiver Using the MT8860 (5V Operation)

Rys. 3 - Schemat połączeń odbiornika wejściowego single ended z wykorzystaniem MT8860 (zasilanie 5 V)

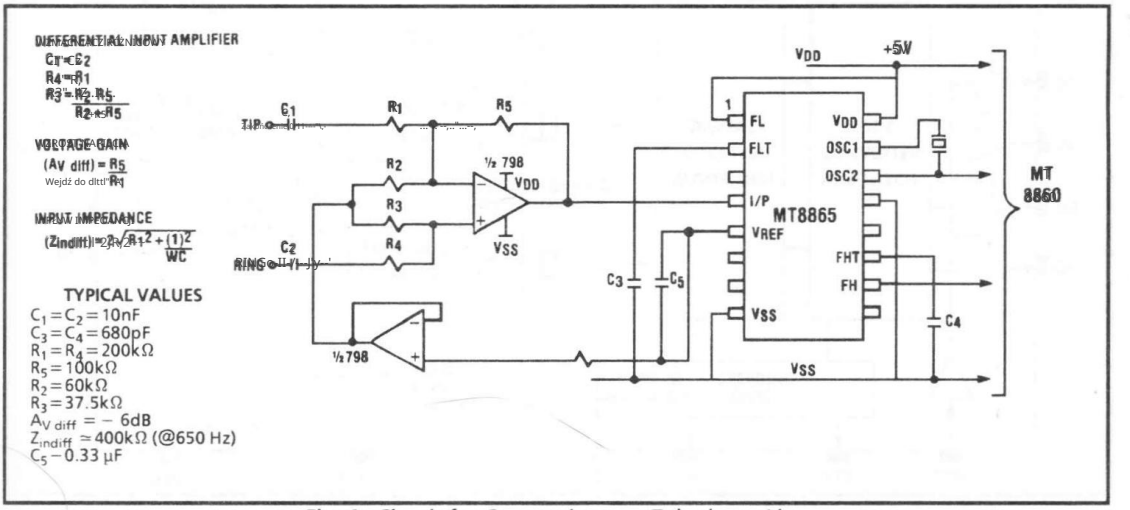

Fig. 4 - Circuit for Connection to a Telephone Line

Rys. 4 - Schemat podłączenia do linii telefonicznej

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capacitively coupled, this is achieved by connecting the signal input to V_{Ref} (Pin 5) via a 2MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680pF capacitors.

The MT8865 and its companion, the MT8860 DTMF decoder, can share a crystal by cascading the oscillator inputs (OSC2). To the adjacent device oscillator input (OSC1). The recommended circuit is shown in Figure 5.

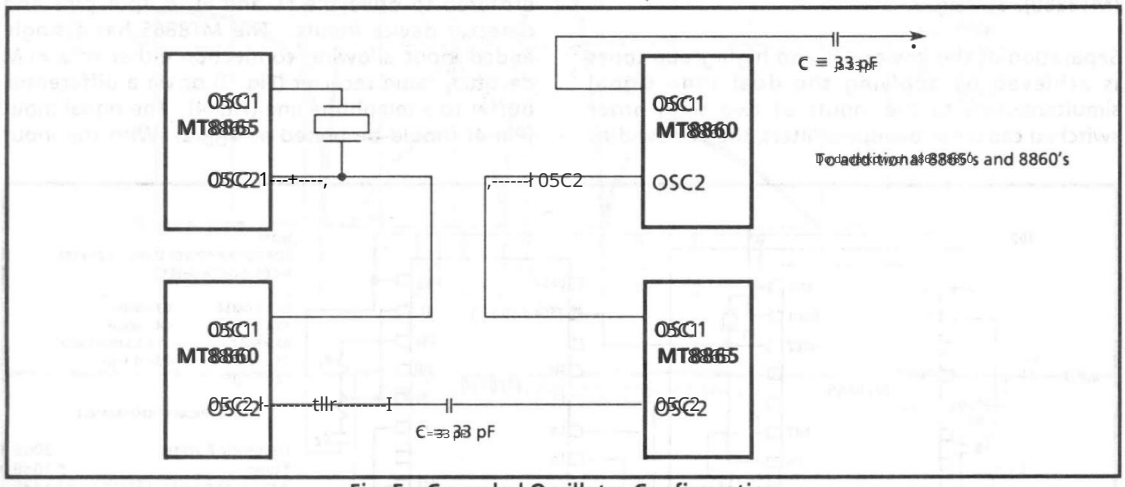

Fig. 5 - Cascaded Oscillator Configuration

Rys. 5 - Konfiguracja kaskadowego oscylatora

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9116 002 051-NA ISSUE 2 December 1987

Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

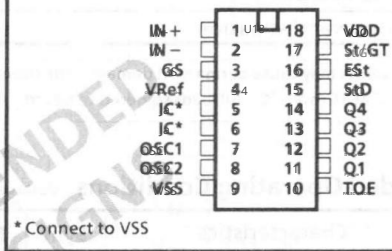
Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870B-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers

Description

The MT8870B/MT8870B-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters, the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three state bus interface.

Pin Connections



* Connect to VSS

Ordering Information

MT8870BE/MT8870BE-1 Plastic DIP
MT8870BC/MT8870BC-1 Cerdip

-40°C to +85°C

NOT RECOMMENDED FOR NEW DESIGN

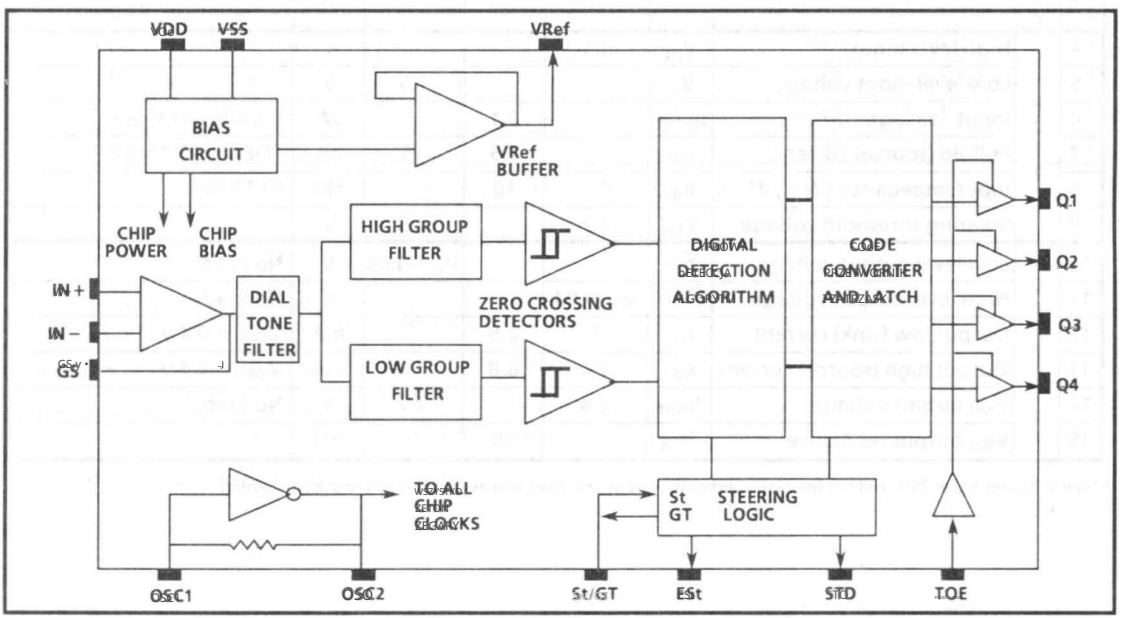


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}			6	V
2	Voltage on any pin		V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)			10	mA
4	Operating temperature	T_{OA}	-40	+85	°C
5	Storage temperature		-65	+150	°C
6	Package power dissipation			1000	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75°C at 16mW/°C. All leads soldered to board.

Recommended Operating Conditions

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive Supply Voltages	V_{DD}		5		V	V_{SS} = 0V
2	Oscillator Clock Frequency	fc	3.579545	3.579545		MHz	
3	Oscillator Frequency Tolerance	Δfc			±0.1	%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_D		15	45	mW	f = 3.58 MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5		Low level input voltage	V_{IL}			1.5	V	
6		Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{DD} or V_{SS}
7		Pull-up (source) current	I_{SO}	2.5	7.5	15	μA	TOE (pin 10) = 0V
8		Input impedance (IN+, IN−)	R_{IN}		10		MΩ	@1 kHz
9		Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
11		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4 V
13		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.7	V	No load
15		V_{Ref} output resistance	R_{OR}		10		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

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Operating Characteristics† Voltages are with respect to ground (V_{SS}) unless otherwise stated

Charakterystyka pracy – napięcia są podane w stosunku do uziemienia (V_{SS}) chyba że podano inaczej

Wzmacniacz z ustawieniem wzmocnienia

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current Prąd upływu wejściowego	I_{IN}		100		nA	$V_{SS} - V_{IN} \le V_{DD}$
2	Input resistance Rezystancja wejściowa	R_{IN}		10		MΩ	
3	Input offset voltage Napięcie przesunięcia wejściowego	V_{OS}		25		mV	
4	Power supply rejection Odrzucenie zasilania	PSRR		60		dB	1 kHz
5	Common mode rejection Odrzucenie sygnału wyłącznie wspólnym	CMRR		60		dB	$-3.0V \le V_{IN} \le 3.0V$
6	DC open loop voltage gain Wzmocnienie napięciowe pętli otwartej DC	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth Otwarta pętla wzmocnienia jednostkowego	f_C		1,5		MHz	
8	Output voltage swing Wahania napięcia wyjściowego	V_O		4.5		V_{pp}	$R_L \ge 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS) Maksymalne obciążenie pojemnościowe (GS)	C_L		100		pF	
10	Maximum resistive load (GS) Maksymalne obciążenie rezystancyjne (GS)	R_L		50		KΩ	
11	Common mode range Zakres trybu wspólnego	V_{CM}		3.0		V_{pp}	No Load Bez obciążenia

†V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C

‡Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

‡Typowe liczby są przy 25°C i tylko do celów projektowych: nie gwarantowane i nie podlegają testowaniu produkcyjnemu.

MT8870B AC Electrical Characteristics† Voltages are with respect to ground (V_{SS}) unless otherwise stated

MT8870B AC – elektryczne charakterystyki – napięcia są podane w stosunku do uziemienia (V_{SS}) chyba że podano inaczej

		Characteristics	Sym	Min	Typ	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal) Prawidłowe poziomy sygnału wejściowego Sygnał wejściowy (każdy ton kompozytowy)		-29			dBm	1,2,3,5,6,9
				27.5			mVRMS	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mVRMS	1,2,3,5,6,9
2		Positive twist accept Pozytywny zwrot akceptacji			10		dB	2,3,6,9
3		Negative twist accept Akceptacja skrętu negatywnego			10		dB	2,3,6,9
4		Freq. deviation accept Odchylenie częstotliwości akceptowane		±1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject Odrzucenie odchylenia częstotliwości		±3.5%			Nom.	2,3,5,9
6		Third tone tolerance Tolerancja trzeciego tonu			-16		dB	2,3,4,5,9
7		Noise tolerance Tolerancja hałasu			-12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance Tolerancja tonu wybierania			+22		dB	2,3,4,5,8,9,11

†V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, 3.579545MHz crystal frequency, 3.579545MHz oscillator frequency, using test circuit shown in Figure 2.

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 2.5% ± 2Hz.
7. Bandwidth limited (3kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz). ± 2 %.
9. Per worst case of best than 1 in 100,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid acceptable level.
12. For guard time calculation purposes.

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MT8870B-1 AC Electrical Characteristics

MT8870B/MT8870B-1 Charakterystyki elektryczne prądu przemiennego - Napięcia podane względem ziemi (V_{SS}), chyba że podano inaczej

		Characteristics	Sym	Min	Typ	Max	Units	Notes
		Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9
				21.8			mVRMS	1,2,3,5,6,9
1	SIGNAL CONDITIONS					+1	dBm	1,2,3,5,6,9
						869	mVRMS	1,2,3,5,6,9
2		Input Signal Level Reject		-37			dBm	1,2,3,5,6,9
				10.9			mVRMS	1,2,3,5,6,9
3		Positive twist accept				6	dB	2,3,6,9
4		Negative twist accept				6	dB	2,3,6,9
5		Freq. deviation accept		±1.5% ± 2Hz				2,3,5,9
6		Freq. deviation reject		±3.5%				2,3,5,9
7		Third tone tolerance		-18		5	dB	2,3,4,5,9,13
8		Noise tolerance			-12		dB	2,3,4,5,7,9,10
9		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

† V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C, and f_c = 3.579545 MHz, using test circuit shown in Figure 2.

NOTES

1. dBm = decybele powyżej/poniżej mocy odniesienia 1 mW przy 600 omach
2. Sekwencja cyfr składa się z wszystkich tonów DTMF
3. Czas trwania dźwięku = 40 ms, przerwa dźwiękowa = 40 ms
4. Sygnał sygnału składa się z normalnych częstotliwości DTMF
5. Oba tony w sygnale kompozytowym mają równą amplitudę.
6. Para tonowa jest odchylona o ± 1,5% ± 2Hz.
7. Szum Gaussa ograniczony pasmowo (3 kHz) (Gaussian noise).
8. Dokładne częstotliwości tonów wybierania wynoszą (350 Hz i 440 Hz) ± 2%.
9. Dla szybkości błędów lepszej niż 1 do 10 000.
10. Odniesione do najniższej częstotliwości składowej sygnału DTMF.
11. Odnosi się do minimalnego ważnego poziomu akceptacji.
12. Do celów obliczania czasu ochronnego.
13. W odniesieniu do rys. 10 poziom tonu wejściowego DTMF przy -25 dBm (-28 dBm na pinie GS) zakres częstotliwości zakłóceń 480-3400 Hz.

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AC Electrical Characteristics

Charakterystyki elektryczne dynamiczne – Napięcia względem masy cyfrowej (V_{SS}) chyba że podano inaczej

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	TONE/TONE	Tone present detect time	t_{DP}	5	11	14	ms	Note 12
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 12
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	t_{REC}	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PSD}		12		µs	TOE = V_{DD}
9		Output data set-up (Q to StD)	t_{QSD}		3.4		µs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	R_L = 10kΩ, C_L = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	R_L = 10kΩ, C_L = 50 pF
12	CLOCK	Crystal clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
13		Clock input rise time	t_{LH}			110	ns	Ext. clock
14		Clock input fall time	t_{HL}			110	ns	Ext. clock
15		Clock input duty cycle	DC	40	50	60	%	Ext. clock
16		Capacitive load (OSC2)	C_{LO}			30	pF	

† V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25°C, 3.579545 MHz crystal used, using test circuit shown in Figure 2.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

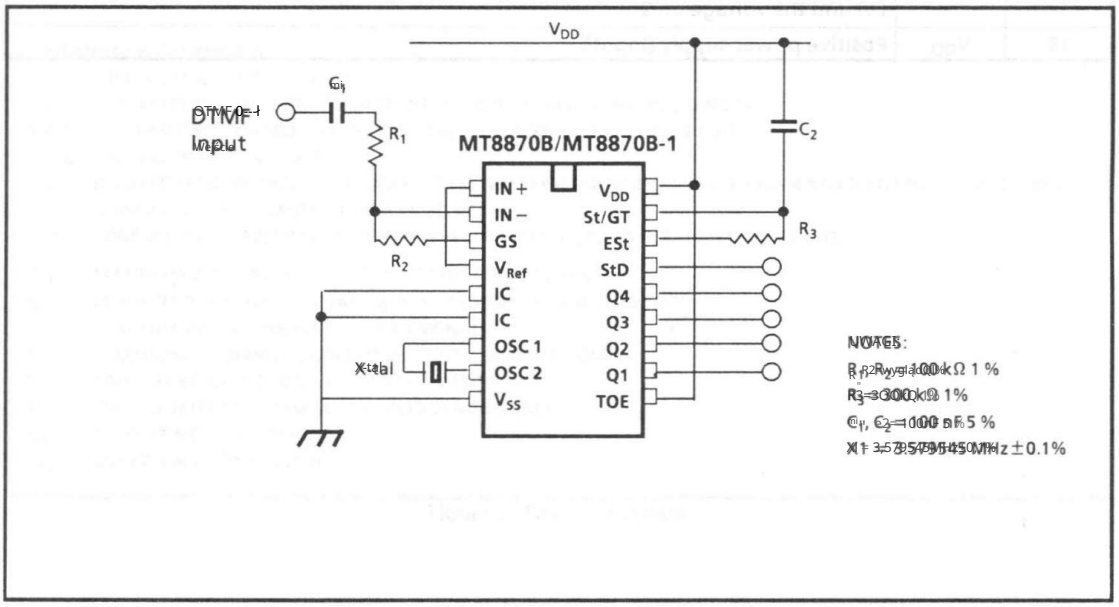

Figure 2 - Single Ended Input Configuration

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Pin Description

Pin #	Name	Description
1	IN+	Non-Inverting Op-Amp (Input).
2	IN−	Inverting Op-Amp (Input).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{Ref}	Reference Voltage (Output). Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 2).
5	IC	Internal Connection. Must be tied to V_{SS}.
6	IC	Internal Connection. Must be tied to V_{SS}.
7	OSC1	Clock (Input).
8	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative Power Supply (Input).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered, and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}
16	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply (Input).

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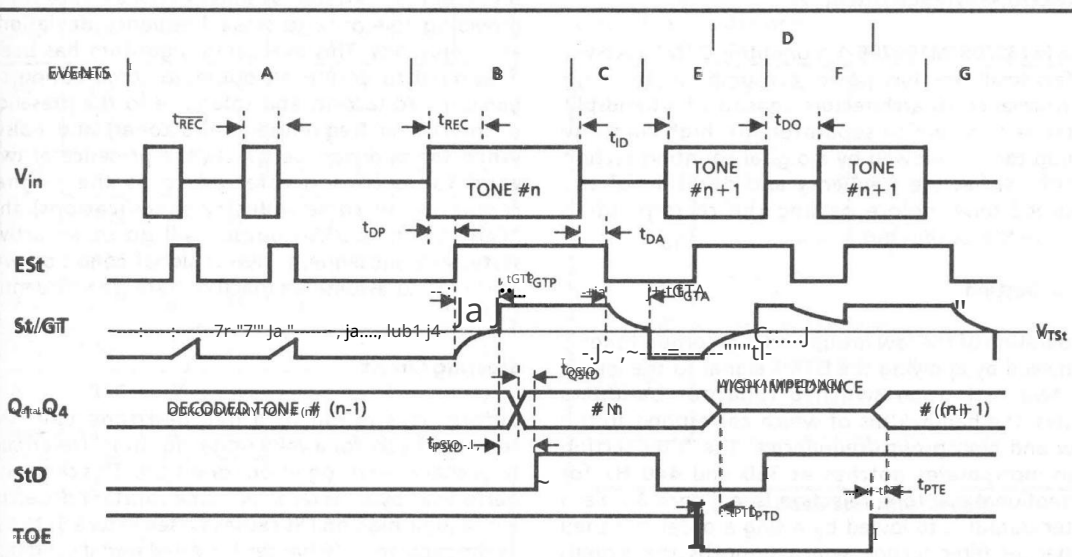

EXPLANATION OF EVENTS

A) TONE BURST DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS.

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

Q_1-Q_4 4 BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME, THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE INPUT. A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

t_{REC} MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.

t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.

t_{ID} MINIMUM TIME BETWEEN VALID DTMF SIGNALS.

t_{DO} MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.

t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

t_{GTP} GUARD TIME, TONE PRESENT.

t_{GTA} GUARD TIME, TONE ABSENT.

Figure 3 Timing Diagram

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Functional Description

The MT8870B/MT8870B-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4). Each filter output is followed by a single-order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice, while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period (t_{REC}), V_C reaches the threshold (V_T) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit

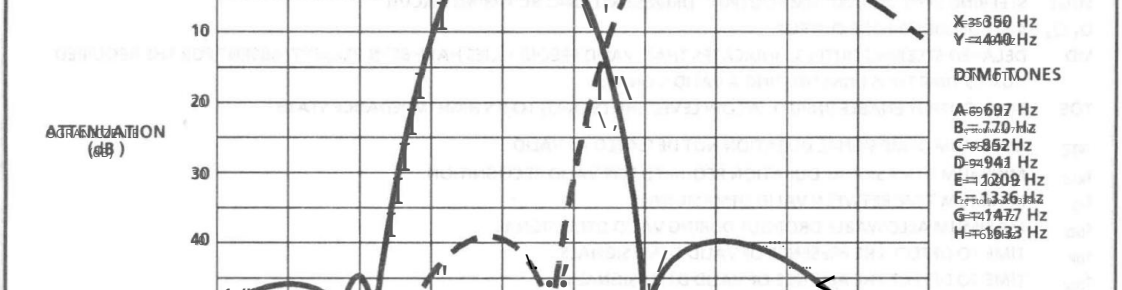

Figure 4 - Filter Response

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F_{LOW}	F_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = WYSOKA IMPEDANCJA

Tabela 1. Tabela dekodowania funkcjonalnego

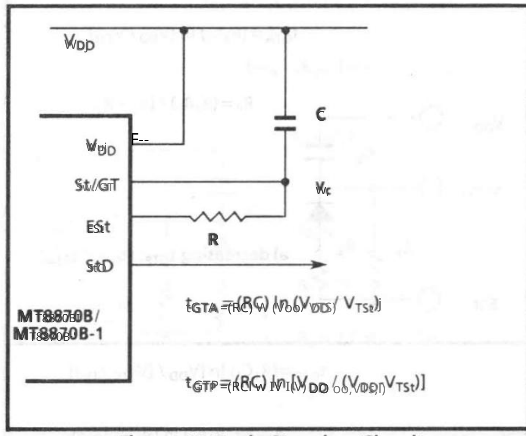
pauza między sygnałami. W ten sposób, jak również odrzucenie sygnałów zbyt krótkich, aby uznać je za ważne, odbiornik będzie tolerować przerwy w sygnale (zanik sygnału) zbyt krótkie, by zostać uznane za ważną pauzę. Ta funkcja, razem z możliwością wyboru czasu sterowania stałe zewnętrznie, pozwala projektantowi dostosować wydajność, spełniającą wymagania określonego systemu.

Regulacja czasu ochronnego

W wielu sytuacjach nie wymaga się niezależnego wyboru czasu trwania tonu i przerwy między tonami, prosty obwód sterowania pokazany na rysunku 5 jest odpowiedni. Wartości komponentów są wybierane według wzoru:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

Wartość t_{DP} jest parametrem urządzenia (patrz rysunek 3) a t_{REC} to minimalny czas trwania sygnału, który ma zostać rozpoznany przez odbiornik. Wartość C wynosząca 0,1 µF jest zalecana dla większości zastosowań, pozostawiając R do wybrania przez projektanta.



Rysunek 5 - Podstawowy obwód sterujący

Różne stałe czasowe sterowania mogą być użyte do niezależnego wyboru czasu trwania tonu (t_{GTP}) i przerwy (t_{GTA}). Może to być konieczne do spełnienia specyfikacji systemu, które określają zarówno akceptację, jak i odrzucenie ograniczeń dotyczących czasu trwania tonu i przerwy między cyframi. Regulacja czasu ochronnego pozwala również projektantowi dostosować parametry systemu, takie jak odporność na zakłócenia i mowę. Zwiększenie t_{REC} poprawia odporność na zakłócenia, ponieważ zmniejsza prawdopodobieństwo, że tony symulowane przez mowę będą utrzymywać sygnał wystarczająco długo, aby zostać zarejestrowane. Alternatywnie, stosunkowo krótki t_{REC} z długim t_{DO} byłby odpowiedni dla bardzo hałaśliwych środowisk, w których wymagany jest szybki czas akwizycji i wymagana jest odporność na zaniki tonu. Informacje dotyczące dostosowania czasu ochronnego są wyświetlane w Rysunek 6.

Konfiguracja wejścia różnicowego

Układ wejściowy MT8870B/MT8870B-1 zapewnia wzmacniacz operacyjny o wejściu różnicowym, jak również źródło polaryzacji (V_{Ref}), które służy do polaryzacji wejścia na środkowej szynie. Przewidziano możliwość podłączenia rezystora sprzężenia zwrotnego do wyjścia wzmacniacza operacyjnego (GS) w celu regulacji wzmocnienia. W konfiguracji single-ended piny wejściowe są połączone tak, jak pokazano na rysunku 2, ze wzmacniaczem operacyjnym podłączonym dla wzmocnienia jednostkowego i V_{Ref} polaryzującym wejście przy $\frac{1}{2}V_{DD}$. Rysunek 7 pokazuje konfigurację różnicową, która umożliwia regulację wzmocnienia za pomocą rezystora sprzężenia zwrotnego R_5.

3

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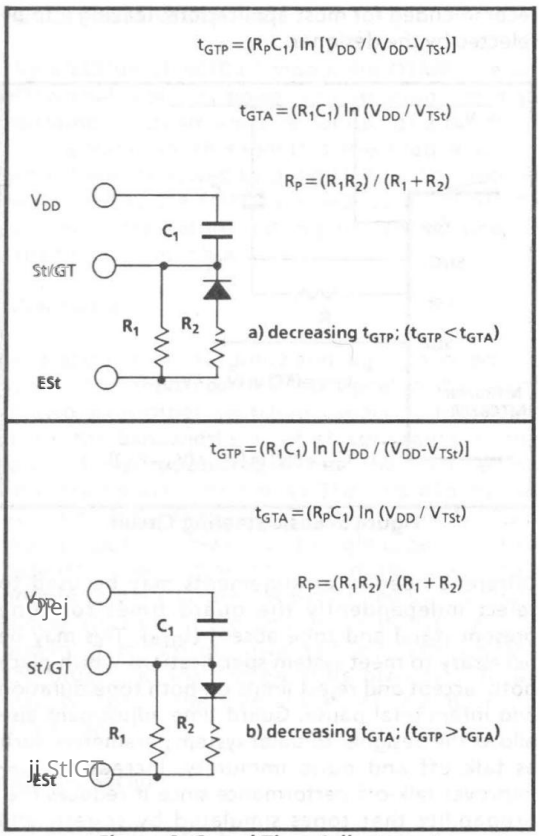
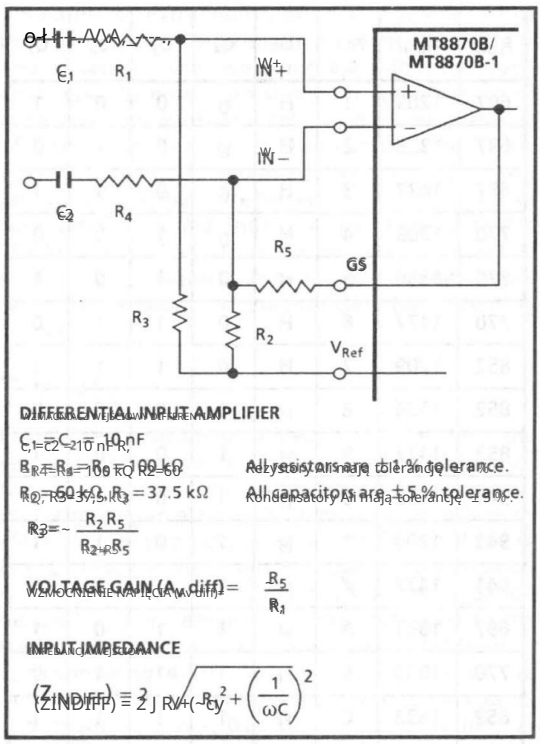


Figure 6. Guard Time Adjustment

Rysunek 6 – Regulacja czasu ochrony



All resistors are 1% tolerance.
All capacitors are ±5% tolerance.

Figure 7. Differential Input Configuration

Rysunek 7 – Różnicowe wejście konfiguracja

Crystal Oscillator

Oscylator kryształowy

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal, and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870B/MT8870B-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 8 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

Wewnętrzny obwód zegarowy jest kompletny z zewnętrzny 3,579545 MHz kryształ i jest normalnie podłączony tak jak pokazano na rysunku 2 (konfiguracja wejścia single ended). Jednakże możliwe jest skonfigurowanie kilku urządzeń MT8870B/MT8870B-1 wykorzystując tylko jeden oscylator kryształ. Wyjście oscylatora pierwszego urządzenia w łańcuchu jest sprzężone przez kondensator 30 pF z wejściem oscylatora (OSC1) następnego urządzenia. Następne urządzenia są podłączone w podobny sposób. Zobacz rysunek 8 aby uzyskać szczegółowe informacje. Problemy niesymetrycznego obciążenia nie są problemem w pokazanym układzie, tj. precyzyjne kondensatory bilansowe nie są wymagane.

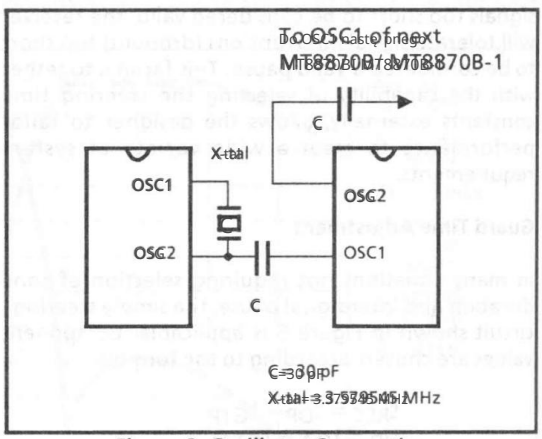


Figure 8. Oscillator Connection

Rysunek 8 – Podłączenie oscylatora

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APPLICATION

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 10 illustrates the use of MT8870B-1 device in a typical receiver system. BT defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870B-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance it is recommended to use the non-symmetric guard time circuit in Fig. 9.

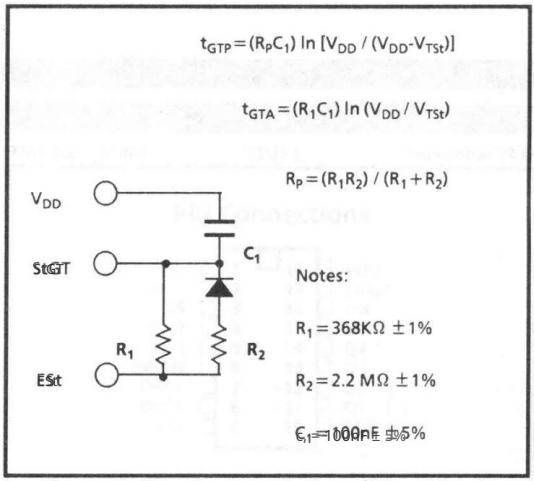

Figure 9 - Non-Symmetric Guard Time Circuit

Rysunek 9 – Niesymetryczny obwód czasu ochronnego

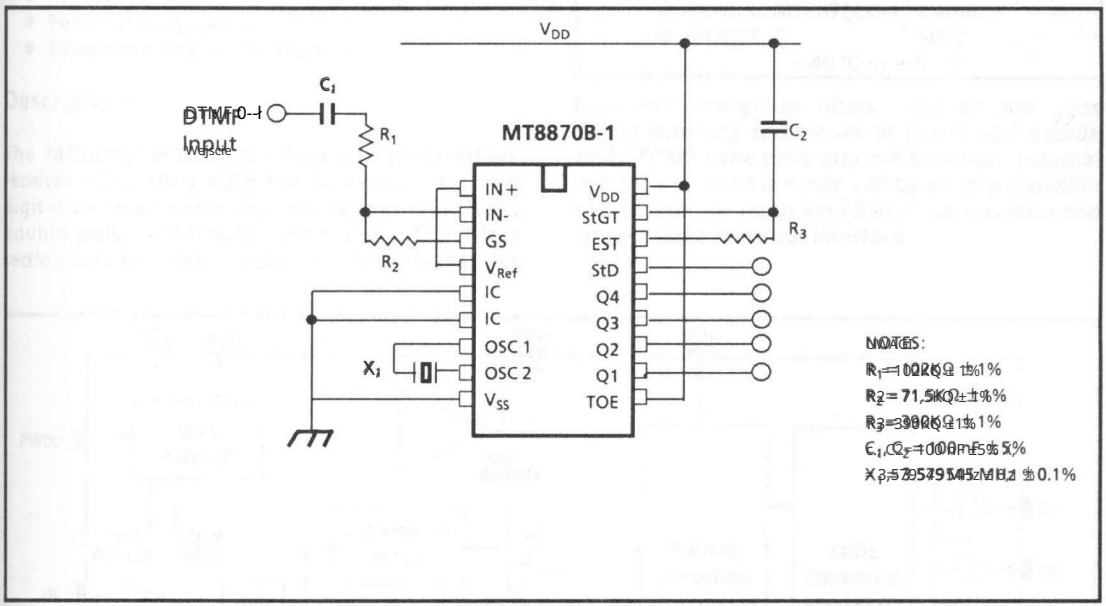

Figure 10 – Single Ended Input Configuration for BT or CEPT Spec

Rysunek 10 – konfiguracja wejściaswingle ended dla BT lub CEPT spec

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MITEL

ISO²-CMOS MT8870C/MT8870C-1
Integrated DTMF Receiver

9164-002-094-NA ISSUE 1 November 1990

Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality
- Power-down Mode
- Inhibit Mode

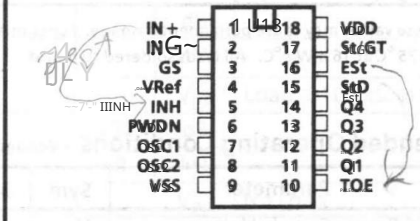
Applications

- Receiver System for British Telecom (BT) or CEPT Spec. (MT8870C-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers
- Telephone Answering Machine

Description

The MT8870C/MT8870C-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

Pin Connections



Ordering Information

MT8870CE/ME	Plastic DIP
MT8870CC/MC	Ceramic DIP
MT8870CE-1/ME-1	Plastic DIP
MT8870CC-1/MC-1	Cerdip
MT8870CS	SOIC

−40 °C to +85 °C

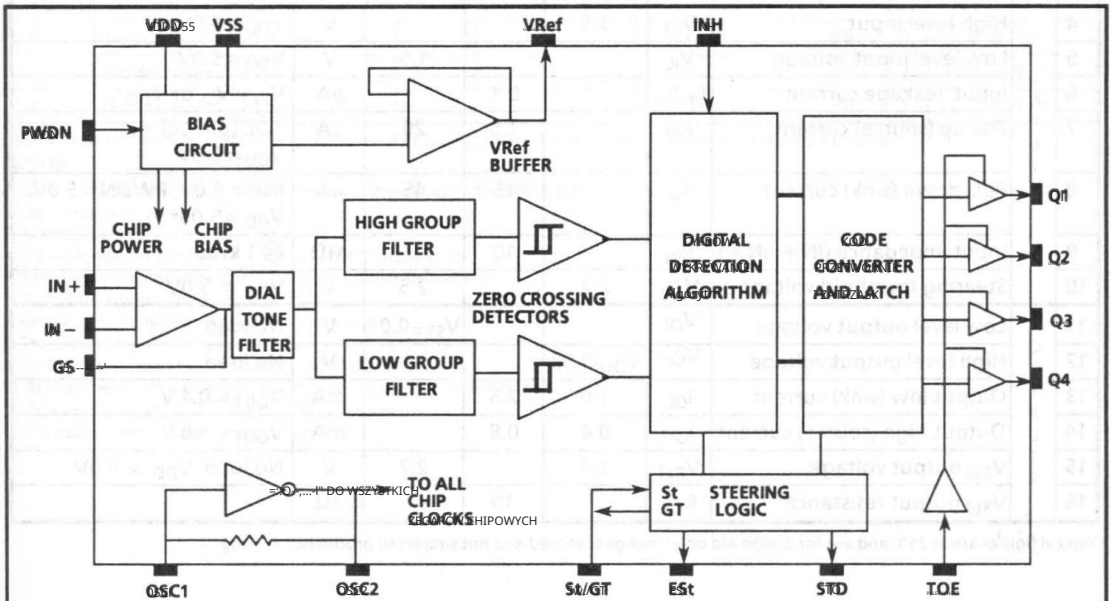


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}		6	V
2	Voltage on any pin	V_I	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		1000	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75°C at 16 mW/°C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ†	Max	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_{OP}	-40		+85	°C	
3	Crystal/Clock Frequency	f_c		3.579545		MHz	
4	Crystal/Clock Freq. Tolerance	Δf_c			±0.1	%	

† Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - $V_{DD}=5.0V\pm5\%$, $V_{SS}=0V$, $-40°C\le T_A\le+85°C$, unless otherwise stated.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}			100	µA	PWDN = V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_D		15	50	mW	$f_c = 3.579545$ MHz
4	INPUTS	High level input voltage	V_{IH}	3.5			V	$V_{DD}=5.0V$
5		Low level input voltage	V_{IL}			1.5	V	$V_{DD}=5.0V$
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	$V_{IN}=V_{SS}$ or V_{DD}
7		Pull-up (source) current	I_{SO}	7.5	20	45	µA	TOE (pin 10) = 0, $V_{OUT}=0V$, $V_{DD}=5.0V$
8		Pull-down (sink) current	I_{SI}	15	45		µA	$V_{INH}=5.0V$, PWDN = 5.0V, $V_{OUT}=5.0V$, $V_{DD}=5.0V$
9		Input impedance (IN+, IN−)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2		2.5	V	$V_{DD}=5.0V$
11	OUTPUTS	Low level output voltage	V_{OL}			$V_{SS}+0.05$	V	No load
12		High level output voltage	V_{OH}	$V_{DD}-0.03$			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	$V_{OUT}=0.4$ V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	$V_{OUT}=4.6$ V
15		V_{Ref} output voltage	V_{Ref}	2.4	2.7		V	No load, $V_{DD}=5.0V$
16		V_{Ref} output resistance	R_{OR}		10		kΩ	

† Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

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Operating Characteristics

Charakterystyka pracy - V_{DD} = 5.0V ±5%, V_{SS} = 0V, -40°C do +85°C, o ile nie podano inaczej. V_{DD} = 5.0V ±5%, V_{SS} = 0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

Gain Setting Amplifier

Wzmacniacz z ustawieniem wzmocnienia

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
					Maksymalna liczba bajtów danych		Warunki testowe
1	Input leakage current Prąd upływu wejściowego	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance Rezystancja wejściowa	R_{IN}	10			MΩ	
3	Input offset voltage Napięcie przesunięcia wejściowego	V_{OS}			25	mV	
4	Power supply rejection Odrzucenie zasilania	PSRR	50			dB	1 kHz
5	Common mode rejection Odrzucanie sygnału w trybie wspólnym	CMRR	40			dB	-3.0 V ≤ V_{IN} ≤ 3.0 V
6	DC open loop voltage gain Wzmocnienie napięcia dla pętli otwartej DC	A_{VOL}	32			dB	
7	Unity gain bandwidth Jednostkowe wzmocnienie pasma	f_C	0.30			MHz	
8	Output voltage swing Wahania napięcia dla wyjściowego	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} Obciążenie Vpp 2. 100 kN do VSS
9	Maximum capacitive load (GS) Maksymalne obciążenie pojemnościowe (GS)	C_L			100	pF	
10	Maximum resistive load (GS) Maksymalne obciążenie rezystancyjne (GS)	R_L			50	kΩ	
11	Common mode range Zakres trybu wspólnego	V_{CM}	2.5			V_{pp}	No Load Bez obciążenia

MT8870C AC Electrical Characteristics†

Charakterystyka elektryczna prądu przemiennego MT8870C - V_{DD} = 5.0 V ± 5%, V_{SS} = 0V, -40°C ≤ T_O ≤ +85°C, using Test Circuit shown in Figure 2.
Do +85°C, używając obwodu testowego pokazanego na rysunku 2.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
								Uwagi*
1		Valid input signal levels (each tone of composite signal) Prawidłowe poziomy sygnału wejściowego (każdy ton lub sygnał kompozytowy)		-29			dBm	1,2,3,5,6,9
				-27.5			mVRMS	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mVRMS	1,2,3,5,6,9
2		Negative twist accept Akceptacja negatywnego zwrotu				6	dB	2, 3, 6, 9
3		Positive twist accept Pozytywny zwrot akcji, zakres				6	dB	2, 3, 6, 9
4		Frequency deviation accept Odchylenie częstotliwości - przyjęcie		±1.5% ± 2 Hz				2, 3, 5, 9
5		Frequency deviation reject Odrzucenie odchylenia częstotliwości		±3.5%				2, 3, 5, 9
6		Third tone tolerance Tolerancja trzeciego tonu				+16	dB	2, 3, 4, 5, 9, 10
7		Noise tolerance Tolerancja hałasu				+12	dB	2, 3, 4, 5, 7, 9, 10
8		Dial tone tolerance Tolerancja tonu wybierania				+22	dB	2, 3, 4, 5, 8, 9, 11

‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Typowe wartości podano w temperaturze 25°C i służą wyłącznie celom projektowym: nie są gwarantowane i nie podlegają testom produkcyjnym.

*NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5 % ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. For guard time calculation purposes.

*UWAGI

1. dBm = decybele powyżej lub poniżej mocy odniesienia 1 mW przy obciążeniu 600 omów.
2. Sekwencja cyfr składa się ze wszystkich tonów DTMF.
3. Czas trwania dźwięku = 40 ms, przerwa w dźwięku = 40 ms.
4. Stan sygnału składa się z nominalnych częstotliwości DTMF.
5. Oba tony w sygnale złożonym mają taką samą amplitudę.
6. Para tonów odchylona jest o ± 1,5 % ± 2 Hz.
7. Szum Gaussa ograniczony szerokością pasma (3 kHz).
8. Dokładne częstotliwości tonu wybierania wynoszą (350 Hz i 440 Hz) ± 2%.
9. Współczynnik błędów lepszy niż 1 na 10 000.
10. Odnosi się do najniższej częstotliwości składowej w sygnale DTMF.
11. Odnosi się do minimalnego ważnego poziomu akceptacji.
12. W celu obliczenia czasu ochrony.

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MT8870C-1 AC Electrical Characteristics[†] — $V_{DD}=5.0V \pm 5\%$, $V_{SS}=0V$, $-40°C \leq T_O \leq +85°C$, using Test Circuit shown in Figure 2.

		Characteristics	Sym	Min	Typ[‡]	Max	Units	Notes*
1		Valid input signal levels (each tone of composite signal)		-31		+1	dBm	$V_{DD}=5.0V$ 1,2,3,5,6,9
				21.8		869	mV_{RMS}	
2		Input Signal Level Reject		-37			dBm	$V_{DD}=5.0V$ 1,2,3,5,6,9
				10.9			mV_{RMS}	
3		Negative twist accept				6	dB	2,3,6,9
4		Positive twist accept				6	dB	2,3,6,9
5		Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
6		Frequency deviation reject		±3.5%				2,3,5,9
7		Third tone tolerance		-18.5			dB	2,3,4,5,9,13
8		Noise tolerance			-12		dB	2,3,4,5,7,9,10
9		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. For guard time calculation purposes.
13. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.

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AC Electrical Characteristics - $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $-40°C \le T_O \le +85°C$, using Test Circuit shown in Figure 2.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	Note 12
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 12
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	t_{REC}	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{ID}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12	16	µs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 kΩ, 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 kΩ, 50 pF
12	CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
13		Clock input rise time	t_{rCL}			110	ns	Ext. clock
14		Clock input fall time	t_{fCL}			110	ns	Ext. clock
15		Clock input duty cycle	DC	40	50	60	%	Ext. clock
16		Capacitive load (OSC2)	C_O			30	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

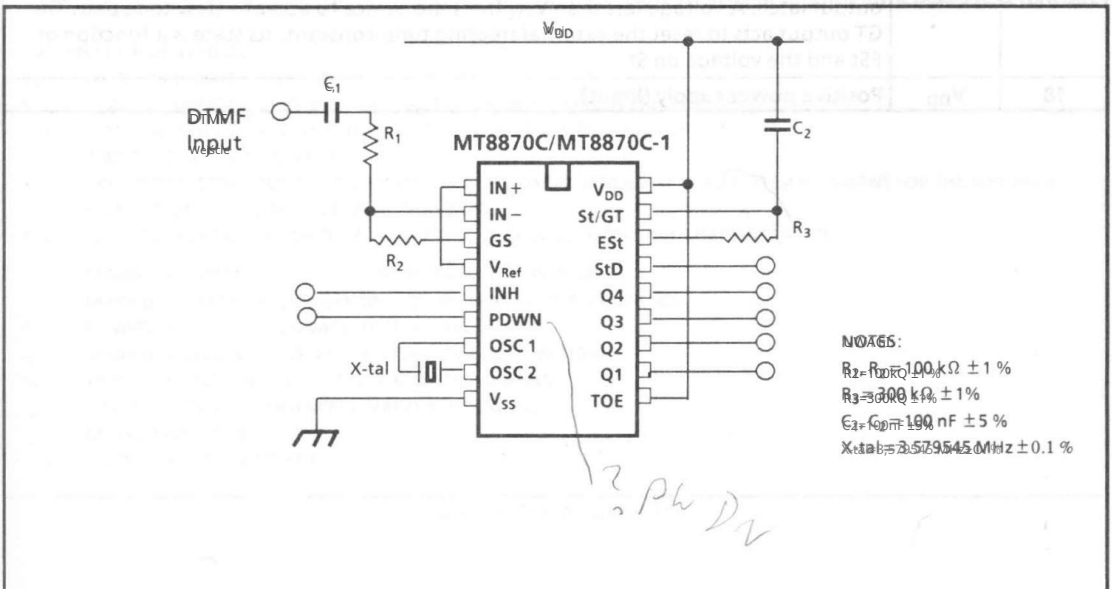

Figure 2 - Single Ended Input Configuration

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Pin Description

Opis pinów

Pin # / Pinka #	Name / Nazwa	Description / Opis
1	IN+	Non-Inverting Op-Amp (Input). Wzmacniacz operacyjny nieodwracający (wejście).
2	IN−	Inverting Op-Amp (Input). Wzmacniacz operacyjny odwracający (wejście).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor. GS Gain Select. Podaje dostęp do wyjścia przedniego wzmacniacza różnicowego dla connection rezystora sprzężenia zwrotnego.
4	VRef	Reference Voltage (Output). Nominally VDD/2 is used to bias inputs at mid-rail (see Fig. 2). Napięcie odniesienia VRef (wyjście), nominalnie VDD/2 jest używane do polaryzacji wejść na środkowej szynie (patrz Rys.2).
5	INH	Inhibit (Input). Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down. Inhibit (input). Logic-high hamuje detection tonów reprezentujących znaki dostępu A, B, C and D. To wejście pinowe jest wewnętrznie trzymane ściągnięte do.
6	PWDN	Power Down (Input). Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down. PWDN Power Down (input). Aktywny wysoki. Wyłącza urządzenie i blokuje oscylator. Ten pin wejściowy jest wewnętrznie trzymany podciągnięty do dołu.
7	OSC1	Clock (Input). Zegar OSC1 (wejście).
8	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit. Zegar OSC2 (wyjście). Kryształ 3,579545 MHz podłączony między pinami OSC1 i OSC2 uzupełnia wewnętrzny układ oscylatora obwodu.
9	VSS	Negative Power Supply (Input). Ujemne napięcie zasilania (wejście).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally. Trzy stany wyjścia włączone (wejście). Logiczne high włączają wyjścia Q1-Q4. Ten pin jest podciągnięte do wewnątrz.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone pair received (see Table 1). When TOE is logic low, the data outputs are high impedance. Q1-Q4 Three State Data (Output). Po włączeniu przez TOE, podają kod odpowiadający ostatnio zarejestrowanej parze tonów odebrania (patrz Tabela 1). Gdy TOE jest logicznie niskie, dane wyjściowe mają wysoką impedancję.
15	StD	Delayed Steering (Output). Presents a logic high when a received tone pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below VTSt. Opóźnione sterowanie (wyjście). Przedstawia stan logiczny wysoki, gdy odebrana para tonów została zarejestrowana i wyjście zatrzaskowe zaktualizowane; wraca do stanu niskiego, gdy napięcie na St/GT spada poniżej VTSt.
16	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low. Wczesne sterowanie (wyjście). Przedstawia logicznie wysoki, jeden, który wykrył algorytm cyfrowy ważna para tonów (stan sygnału). Każda chwilowa utrata stanu sygnału spowoduje ESt powrót do logicznie niskiego poziomu.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St. Czas wejścia sterującego (wyjście) Dwukierunkowy. Napięcie większe niż VTSt wykryte na St powoduje, że urządzenie zarejestruje wykrytą parę tonów i zaktualizować wyjście latch. Napięcie mniejsze niż VTSt zwalnia urządzenie do akceptowania nowej pary tonów. Wyjście GT działa resetuje zewnętrzną stałą czasową sterowania, jego stan jest funkcją ESt i napięcia na St.
18	VDD	Positive power supply (Input). Zasilanie dodatnie (wejście)

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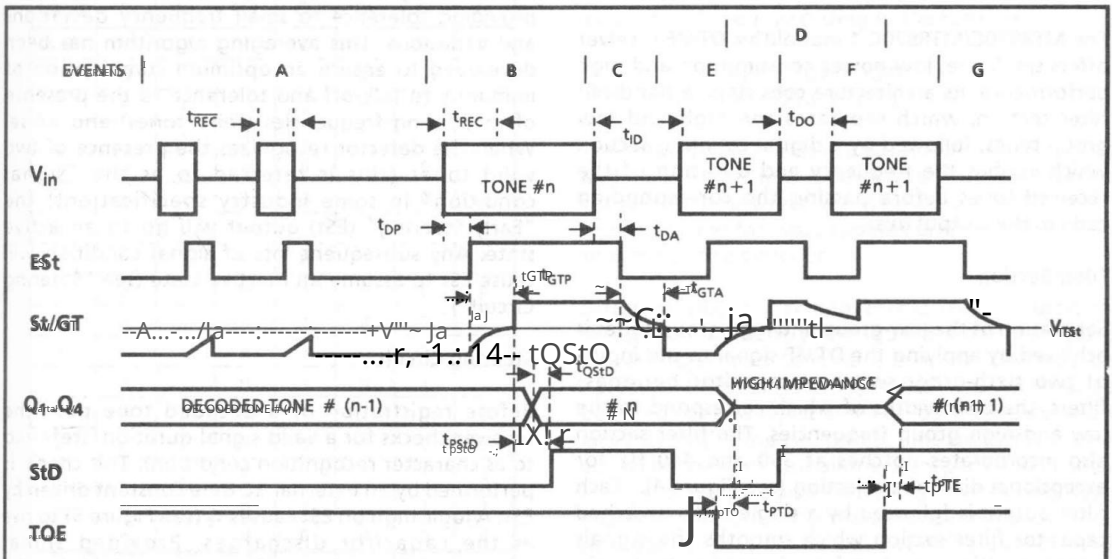

EXPLANATION OF EVENTS

A) TONE BURST DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS.

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OR TONE #n+1 TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT / GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

Q_1-Q_4 4 BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME, THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

t_{REC} MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.

t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.

t_{ID} MINIMUM TIME BETWEEN VALID DTMF SIGNALS.

t_{DO} MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.

t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

t_{GTP} GUARD TIME, TONE PRESENT.

t_{GTA} GUARD TIME, TONE ABSENT.

Figure 3 - Timing Diagram

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Functional Description

Opis funkcjonalny

The MT8870C/MT8870C-1 combines a complete DTMF receiver offers small size, low power consumption and high performance. its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Monolityczny odbiornik DTMF MT8870C/MT8870C-1 łączy w jednym elemencie kompletny, niskie zużycie energii i wysoką wydajność jego architektura składa się z sekcji filtra podziału pasma, która oddziela tony grupy wysokich i niskich, a następnie cyfrowej sekcji liczącej, która weryfikuje częstotliwość i czas trwania odebranych tonów przed przekazaniem odpowiedniego kodu do magistrali wyjściowej.

Filter Section

Sekcja filtra

Separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Oddzielenie tonów grupy niskiej wysokiej uzyskuje się przez zastosowanie sygnału DTMF do wejść dwóch filtrów pasmowo-przepustowych z przełączanymi kondensatorami szóstego rzędu, których charakterystyki częstotliwościowe odpowiadają grupie niskiej i wysokiej. Sekcja filtra zawiera również wycięcia przy 350 i 440 Hz w celu wyjątkowego odrzucenia tonu wybierania (patrz rysunek 4). Po każdym wyjściu filtra następuje sekcja filtra z przełączanym kondensatorem pojedynczego rzędu, która wygładza sygnały przed ograniczeniem. Ograniczanie jest wykonywane przez komparatory o wysokim wzmocnieniu, które mają wyposażone w histerezę, aby zapobiec wykrywaniu niepożądanych sygnałów niskiego poziomu. Wyjścia komparatorów zapewniają pełne wahania logiki szynowej przy częstotliwościach przychodzących sygnałów DTMF.

Decoder Section

Sekcja dekodera

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications), the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Po sekcji filtrów następuje sekcja dekodera wykorzystująca cyfrowe techniki zliczania w celu określenia częstotliwości przychodzących tonów i sprawdzenia, czy odpowiadają one standardowym częstotliwościom DTMF. Złożony algorytm uśredniania chroni przed tonami symulacja za pomocą sygnałów zewnętrznych, takich jak głos, przy jednoczesnym zapewnieniu tolerancji na niewielkie odchylenia i zmiany częstotliwości. Ten algorytm uśredniania został opracowany w celu zapewnienia optymalnej kombinacji odporności na rozmowę i tolerancji na obecność częstotliwości zakłócających (trzeciego tonu) i szumu. Gdy detektor rozpozna obecność dwóch prawidłowych tonów (w niektórych specyfikacjach przemysłowych określa się to jako „stan sygnału"), wyjście „Early Steering" (ESt) przejdzie w stan aktywny. Każda późniejsza utrata stanu sygnału spowoduje, że ESt przejdzie w stan nieaktywny (patrz „Steering Circuit").

Steering Circuit

Obwód sterujący

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 5) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (VTSt) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point, the GT output is activated and drives V_C to GND. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate

Przed zarejestrowaniem zdekodowanej pary tonów dobornik sprawdza prawidłowy czas trwania sygnału (nazywany warunkiem rozpoznawania znaków). Sprawdzenie jest wykonywane przez zewnętrzną stałą czasową RC sterowaną przez ESt. Wysoki stan logiczny ESt powoduje wzrost V_C (patrz rysunek 5) w miarę rozładowywania się kondensatora. Pod warunkiem, że stan sygnału jest utrzymywany (ESt pozostaje wysoki) przez okres walidacji (t_{GTP}), V_C osiąga próg (VTSt) logiki sterującej, aby zarejestrować parę tonów, zatrzaskując odpowiadający jej 4-bitowy kod (patrz tabela 1) w zatrzasku wyjściowym. W tym momencie wyjście GT jest aktywowane i napędza V_C do GND. GT nadal napędza wysoki poziom tak długo, jak ESt pozostaje wysoki. Na koniec, po krótkim opóźnieniu, aby zatrzask wyjściowy mógł się ustalić, opóźniona flaga wyjściowa sterująca (StD) staje się wysoka, sygnalizując, że odebrano parę tonów. Zawartość zatrzasku wyjściowego jest udostępniana na 4-bitowej magistrali wyjściowej poprzez podniesienie wejścia sterującego trzech stanów (TOE) do wysokiego stanu logicznego. Obwód sterujący działa w odwrotnej kolejności, aby potwierdzić

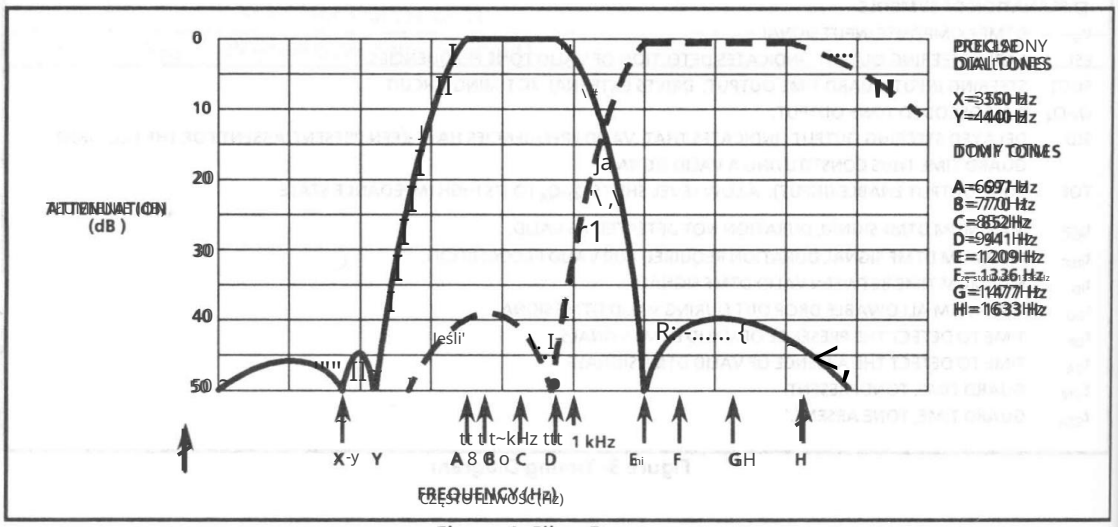

Figure 4. Filter Response

Rysunek 4. Odpowiedź filtra

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Digit	TOE	INH	EST	Q_4	Q_3	Q_2	Q_1
DOWOLNY	L	X	-	Z	Z	Z	Z
1	H	L	H	0	0	0	1
2	H	L	H	0	0	1	0
3	H	L	H	0	0	1	1
4	H	L	H	0	1	0	0
5	H	L	H	0	1	0	1
6	H	L	H	0	1	1	0
7	H	L	H	0	1	1	1
8	H	L	H	1	0	0	0
9	H	L	H	1	0	0	1
0	H	L	H	1	0	1	0
*	H	L	H	1	0	1	1
#	H	L	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
1	H	H	H	0	0	0	1
2	H	H	H	0	0	1	0
3	H	H	H	0	0	1	1
4	H	H	H	0	1	0	0
5	H	H	H	0	1	0	1
6	H	H	H	0	1	1	0
7	H	H	H	0	1	1	1
8	H	H	H	1	0	0	0
9	H	H	H	1	0	0	1
0	H	H	H	1	0	1	0
*	H	H	H	1	0	1	1
#	H	H	H	1	1	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

L = NISKA LOGIKA. H = WYSOKA LOGIKA. Z = WYSOKA IMPEDANCJA

Tabela 1 Funkcjonalna tabela dekodowania

przerwa międzycyfrowa między sygnałami. Tak więc, jak również jako odrzucanie sygnałów zbyt krótkich, aby można je było uznać za ważne, odbiornik będzie tolerował przerwy sygnału (przerwa) jest zbyt krótka, aby można ją było uznać za ważną przerwę. Ta funkcja, wraz z możliwością wyboru stałe czasowe sterowania zewnętrznie, pozwala zaprojektowane w celu dostosowania spotkać się z szeroką publicznością wydajności do różnorodnych wymagań systemowych.

Regulacja osłony wapna

W wielu sytuacjach nie wymagających wyboru tonu czas trwania i pauza międzycyfrowa wymagają prostego sterowania obwód pokazany na rysunku 5 jest stosowalny. Komponent wartości wybierane są według wzoru:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

Wartość t_{DP} jest parametrem urządzenia (patrz rysunek 3) a t_{REC} jest minimalnym czasem trwania sygnału być rozpoznawanym przez odbiornik. Wartość C wynosząca 0,1 µF to zalecane dla większości zastosowań, pozostawiając R wybrane przez projektanta.

Różny układy kierownicze mogą być używane do wybierz niezależnie obecny czasy straży dla tonu (t_{GTP}) i ton nieobecny (t_{GTA}). Może to być konieczne do spełnienia specyfikacji systemu, które umieszczają zarówno akceptują, jak i odrzucają ograniczenia dotyczące czasu trwania tonu i pauza międzypalcowa. Regulacja czasu straży również umożliwia projektantowi dostosowanie parametrów systemu, takich jak jak wyciszanie rozmów i odporność na zakłócenia. Zwiększanie t_{REC} poprawia wydajność wyciszania rozmów, ponieważ redukuje prawdopodobieństwo, że dźwięki symulowane przez mowę będą utrzymywać stan sygnału wystarczająco długo, aby zarejestrowany. Alternatywnie, stosunkowo krótki t_{REC} z długi t_{DO} byłby odpowiedni w przypadku bardzo głośnych dźwięków środowiska, w których wymagany jest szybki czas akwizycji i wymagana jest odporność na zaniki tonu. Informacje dotyczące projekt regulacji czasu ochronnego są pokazane w Rysunek 6.

Tryb wyłączania i blokowania

Logiczne wysokie napięcie przyłożone do pinu 6 (PWDN) spowoduje zasilanie wyłączyć urządzenie zminimalizować moc zużycia w trybie gotowości. Zatrzymuje oscylator i funkcje filtrów.

Tryb hamowania włącza się poprzez podanie wysokiego logicznego sygnału wejściowego do pinu 5 (INH). Hamuje wykrywanie tonów reprezentujące znaki A, B, C i D. Wyjście kod pozostanie taki sam jak poprzednio wykryty kod (patrz Tabela 1).

Różnicowe wejście Konfiguracja

Układ wejściowy MT8870C/MT8870C-1 zapewnia wzmacniacz operacyjny o wejściu różnicowym „ponieważ my" jako źródło stronniczości (VRef), które jest wykorzystywane do stronniczości wejścia na mid-rail. Przewidziano także podłączenie rezystora sprzężenia zwrotnego do wyjścia wzmacniacza operacyjnego (GS) dla regulacja wzmocnienia. W konfiguracji single-ended, piny wejściowe są podłączone tak jak pokazano na rysunku 2 ze wzmacniaczem operacyjnym podłączonym dla wzmocnienia jednostkowego i VRef polaryzując wejście na 1/2 VDD. Rysunek 7 pokazuje konfiguracja różnicowa, która pozwala na regulacja wzmocnienia za pomocą rezystora sprzężenia zwrotnego Rf.

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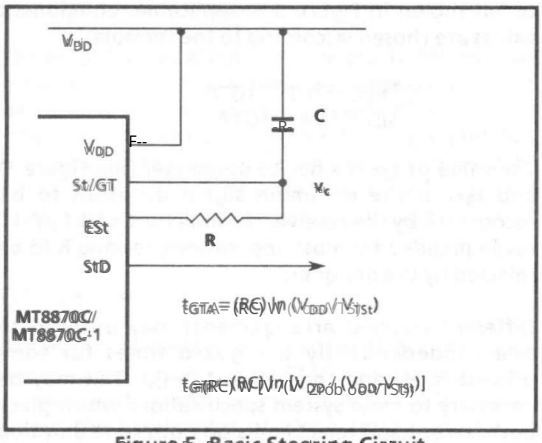

Figure 5 - Basic Steering Circuit

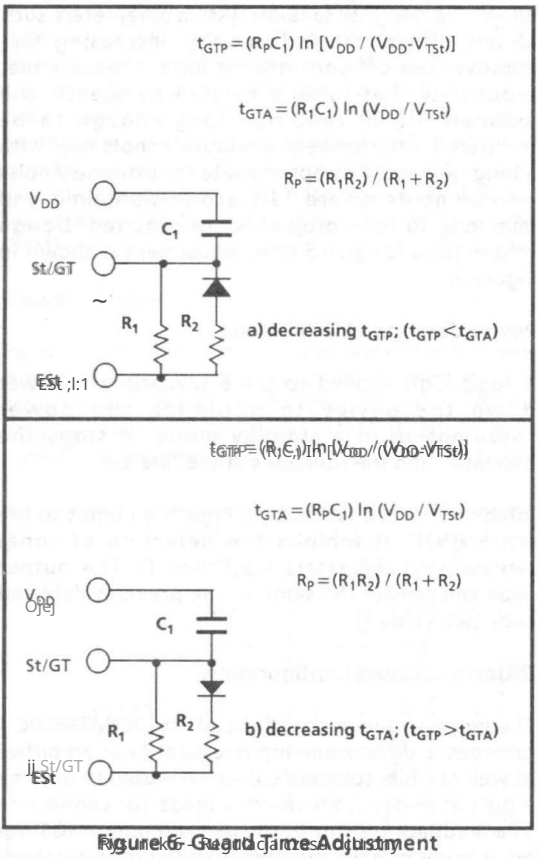

Figure 6 - Guard Time Adjustment

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal. For accurate frequency generation, it is recommended that crystals with tolerance of ±0.1% be used. Typical component values for use with crystals of various tolerances are shown in Figure 8. To ensure reliable starting, it is recommended that the user's PCB layout minimize the capacitive loading on the OSC1 and OSC2 pins.

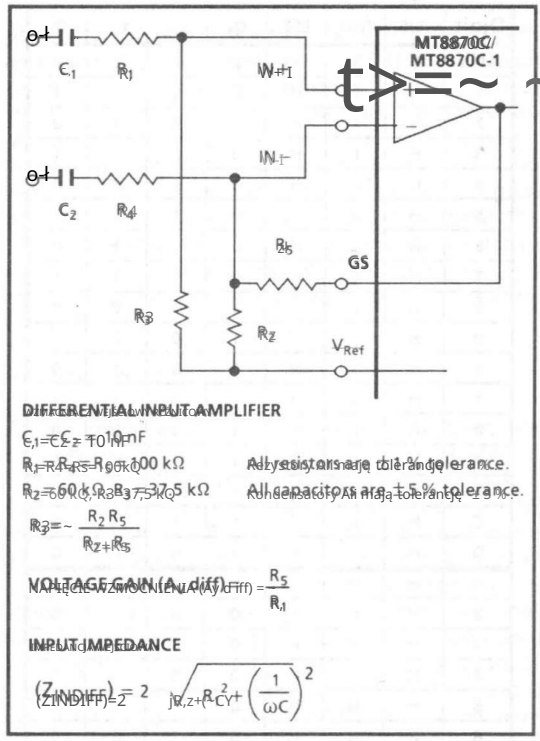

Figure 7 - Differential Input Configuration

Power-down/Inhibit Mode

A logic high on this input pin will power down the device and inhibit the oscillator. Power consumption during power-down is reduced to a minimum by this mode. All internal functions are inhibited, including the guard time and code recognition logic. The contents of the output latch will be lost if power-down is entered during the reception of a valid tone pair.

Inhibit Mode

A logic high on this input pin will inhibit the detection of tones. Any tone bursts during inhibit will not be decoded. The output code will remain unchanged from the previous valid tone pair detected.

Tone Burst Detect Mode

A logic high on this input pin will force the receiver into tone burst detect mode. In this mode, the receiver will decode tones with a minimum duration of 40 ms, regardless of the programmed guard time. This mode can be used to shorten the minimum signal duration requirement for fast signalling systems.

Applications

The MT8870C/MT8870C-1 may be used in a wide variety of call progress tone detection systems. Figure 9 shows a typical single ended input configuration. For those applications requiring differential inputs, Figure 10 shows the recommended circuit. For further information on differential input configuration, see Figure 7.

In some applications, it may be necessary to decode tones from a source which is corrupted by noise. In such cases, the noise immunity of the receiver may be enhanced by connecting a bandpass filter between the tone source and the receiver input. Figure 11 shows a 6th order switched capacitor bandpass filter using the MT8880C. Refer to the MT8880C data sheet for more details.

Power supply transients may cause problems with any digital system. Care should be taken in the layout of printed circuit boards to minimize the effects of fast transients. Power supply lines should be routed away from sensitive analog circuits such as the oscillator and the tone inputs. Adequate power supply bypassing is also necessary. Figure 12 shows the recommended power supply arrangement with bypass capacitors.

Oscillator Connection

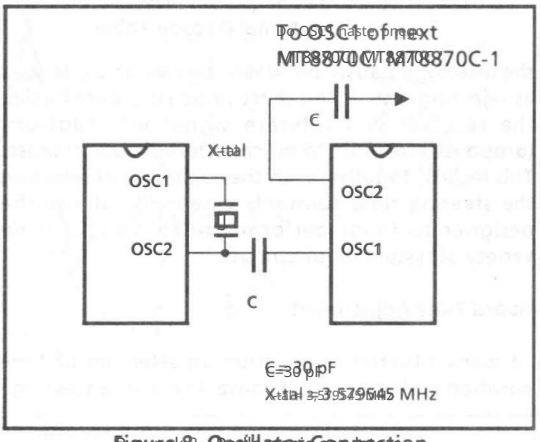

Figure 8 - Oscillator Connection

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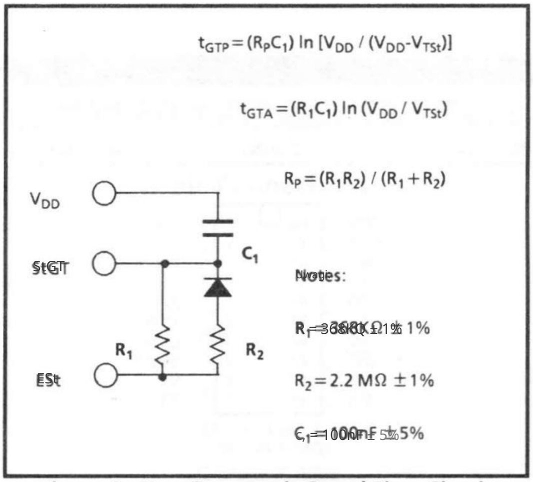
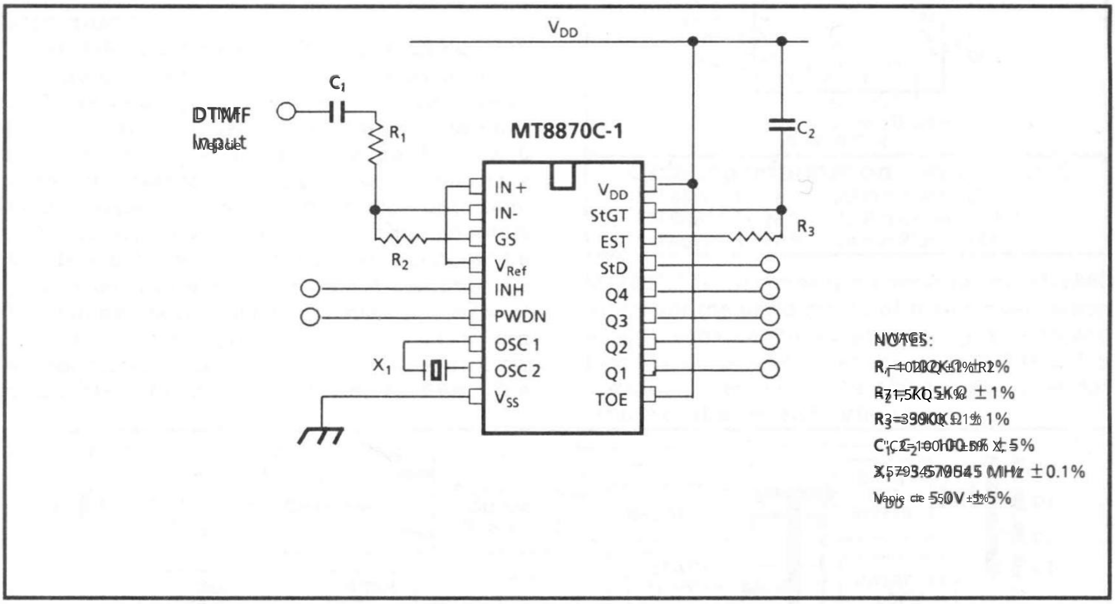
Aplikacja

SYSTEM ODBIORNIKA DLA BRYTYJSKIEJ TELECOM SPEC POR 1151

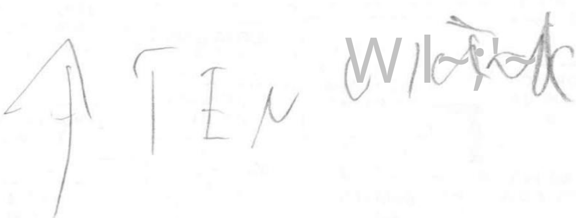
Układ pokazany na rys. 10 ilustruje zastosowanie układu MT8870C-1 w typowym systemie odbiornika. Specyfikacja BT definiuje sygnały wejściowe mniejsze niż -34 dBm jako poziom nieoperacyjny. Warunek ten można osiągnąć, wybierając odpowiednie wartości R1 i R2, aby zapewnić tłumienie 3 dB, tak aby sygnał wejściowy -34 dBm odpowiadał -37 dBm na pinie ustawienia wzmocnienia GS układu MT8870C-1. Jak pokazano na schemacie, wartości składowych R3 i C2 to wymagania czasu ochronnego, gdy całkowita tolerancja składowych wynosi 6%. Aby uzyskać lepszą wydajność, zaleca się użycie niesymetrycznego układu czasu ochronnego na rys. 9.



Rysunek 9 - Niesymetryczny obwód czasu ochronnego



Rysunek 10 — Konfiguracja wejścia single-ended dla BT or CEPT Spec



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MITEL

ISO2-CMOS MT8880/MT8880-1/MT8880-2

Integrated DTMF Transceiver

9161-002-032-NA ISSUE 5 April 1989

Features

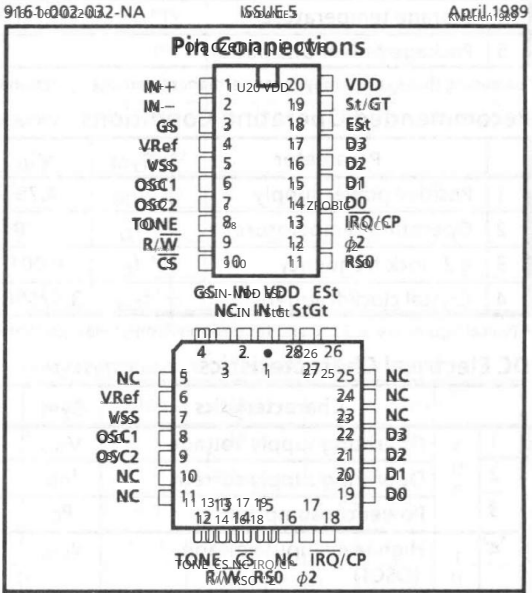
- Complete DTMF transmitter/receiver
- Central office quality
- Low power consumption
- Microprocessor port
- Adjustable guard time
- Interrupt or burst mode
- Call progress mode

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Description

The MT8880 is a monolithic DTMF transceiver with call progress filter. Fabricated in Mitel's ISO2-CMOS technology, which provides low power dissipation and high reliability. The DTMF receiver is based on the industry standard MT8870 monolithic DTMF receiver. For the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones. A standard microprocessor bus is provided and is directly compatible with 6800 series microprocessors. The MT8880-1 is functionally identical to the MT8880 except for the performance of the receiver section which is enhanced to accept lower signal levels and specified guard time. The MT8880-2 is electrically identical to the MT8880 but does not offer the call progress function.



Ordering Information

MT8880/-1/-2AE	20 Pin Plastic DIP
MT8880/-1/-2AC	20 Pin Ceramic DIP
MT8880/-1/-2AP	28 Pin Plastic PLCC

-40°C to +85°C

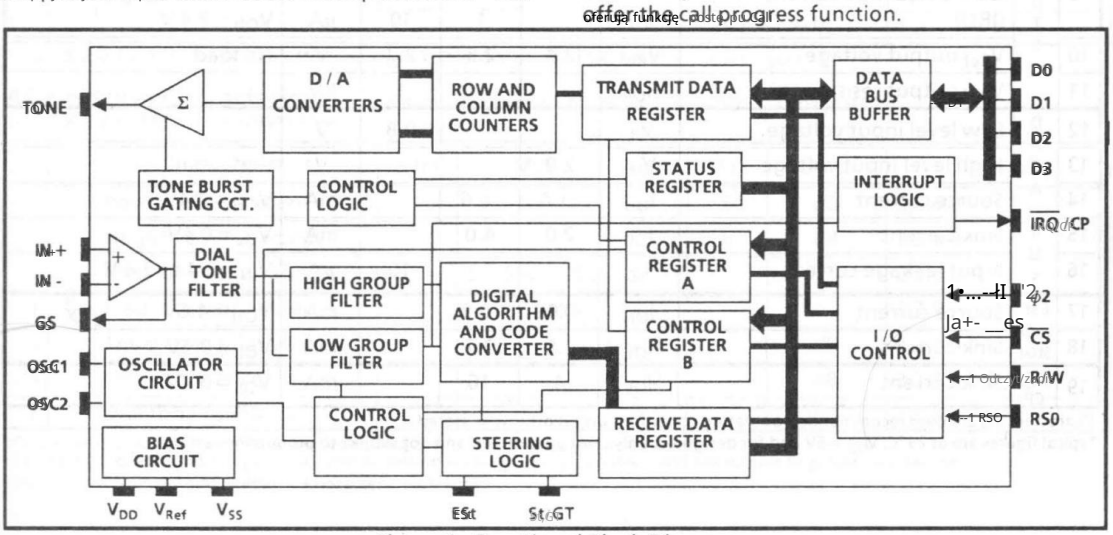


Figure 1 Functional Block Diagram

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Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
4	Storage temperature	T_{ST}	-65	+150	°C
5	Package power dissipation	P_D		1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ†	Max	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_{OP}	-40		+85	°C	
3	Φ2 clock frequency	f_C	0.001		1.0	MHz	
4	Crystal clock frequency	f_{CLK}	3.575965	3.579545	3.583124	MHz	

† Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† f_{CLK} = 3.579545 MHz, $\phi 2$ = 1 MHz, V_{SS} = 0 V.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	SUP	Operating supply voltage	V_{DD}	4.75	5.00	5.25	V	
2		Operating supply current	I_{DD}			10	mA	
3		Power consumption	P_C			52.5	mW	
4	INPUTS (OSC1)	High level input voltage	V_{IHO}	3.5			V	
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	
6		Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V	V_{DD} = 5 V
7	OUTPUTS (OSC2)	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load
8		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load
9		Output leakage current (IRQ)	I_{OZ}		1	10	μA	V_{OH} = 2.4 V
10		V_{Ref} output voltage	V_{Ref}	2.4	2.5	2.7	V	No load
11		V_{Ref} output resistance	R_{OR}			1	kΩ	
12	DATA BUS	Low level input voltage	V_{IL}			0.8	V	
13		High level input voltage	V_{IH}	2.0			V	
14		Source current	I_{OH}	-1.4	-6.6		mA	V_{OH} = 2.4V
15		Sink current	I_{OL}	2.0	4.0		mA	V_{OL} = 0.4V
16		Input leakage current	I_{IZ}			10	μA	V_{IN} = 0.4 to 2.4 V
17	ESt and StD	Source current	I_{OH}	-0.02	-0.9		mA	V_{OH} = 4.6V
18		Sink current	I_{OL}	1.0	2.7		mA	V_{OL} = 0.4V
19	IRQ/CP	Sink current	I_{OL}	4	16		mA	V_{OL} = 0.4V

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25 °C, V_{DD} = 5V and for design aid only: not guaranteed and not subject to production testing.

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Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated. $V_{SS} = 0$ V, $V_{DD} = 5$V, $T_O = 25°C$.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		±0.100		nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR	60			dB	1 kHz
5	Common mode rejection	CMRR	60			dB	$-3.0\ V \le V_{IN} \le 3.0\ V$
6	DC open loop voltage gain	A_{VOL}	65			dB	
7	Unity gain bandwidth	BW	1.5			MHz	
8	Output voltage swing	V_O	4.5			V_{pp}	$R_L \ge 100$ kΩ to V_{SS}
9	Allowable capacitive load (GS)	C_L		100		pF	
10	Allowable resistive load (GS)	R_L	50			kΩ	
11	Common mode range	V_{CM}	3.0			V_{pp}	No Load

‡Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

MT8880-1 AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ	Max	Units	Notes*
1	R X (Sygnał X)	Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9
				21.8			mVrms	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mVrms	1,2,3,5,6,9
2		Input Signal Level Reject		-37			dBm	1,2,3,5,6,9
				10.9			mVrms	1,2,3,5,6,9

†$V_{DD} = 5$ V, $V_{SS} = 0$, $T_A = 25°C$, $f2 = 1$ MHz and $f_c = 3.579545$ MHz using test circuit shown in Figure 15.

MT8880/8880-2 AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	R X (każdy ton kompozytowy sygnał)	Valid Input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mVrms	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mVrms	1,2,3,5,6,9

†$V_{DD} = 5$ V, $V_{SS} = 0$, $T_A = 25°C$, $f2 = 1$ MHz i $f_c = 3.579545$ MHz using test circuit shown in Figure 15.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

$V_{SS} = 0$ V, $f2 = 1$ MHz i $f_c = 3.579545$ MHz.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	R X (odchylenie częstotliwości X)	Positive twist accept				6	dB	2,3,6,9
2		Negative twist accept				6	dB	2,3,6,9
3		Freq. deviation accept		±1.5% ± 2Hz				2,3,5,9
4		Freq. deviation reject		±3.5%				2,3,5
5		Third tone tolerance			-16		dB	2,3,4,5,9,10
6		Noise tolerance			-12		dB	2,3,4,5,7,9,10
7		Dial tone tolerance			22		dB	2,3,4,5,8,9,11

‡Characteristics are over recommended operating conditions unless otherwise stated

‡Typical figures are at 25°C, $V_{DD} = 5$ V and for design aid only: not guaranteed and not subject to production testing

*See "Notes" following AC Electrical Characteristics Tables

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AC Electrical Characteristics† - Call Progress - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Charakterystyka elektryczna prądu przemiennego - Call Progress - Napięcie dla podanego względem uziemienia (V_{SS}), chyba że podano inaczej)

V_{SS} 0V ± 2% unless otherwise stated, f_C = 3.579545 MHz ±0.1%

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1		Lower freq. (ACCEPT)	f_{LA}		320		Hz	@ −25 dBm
2		Upper freq. (ACCEPT)	f_{HA}		510		Hz	@ −25 dBm
3		Lower freq. (REJECT)	f_{LR}		290		Hz	@ −25 dBm
4		Upper freq. (REJECT)	f_{HR}		540		Hz	@ −25 dBm

Characteristics are over recommended operating conditions unless otherwise stated

† Typical figures are at 25°C, V_{DD} = 5V and for design aid only: not guaranteed and not subject to production testing

*See "Notes" following AC Electrical Characteristics Tables

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	RX	Tone present detect time	t_{DP}	3	11	14	ms	Note 12
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 12
3		Tone duration accept	t_{REC}			40	ms	User adjustable*
4		Tone duration reject	t_{REC}	20			ms	User adjustable*
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable*
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable*
7		Delay St to StD_3	t_{PStD3}		13		µs	
8		Delay St to RX_{RX}	t_{PSRX}		8		µs	
9	TX	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
10		Tone pause duration	t_{PS}	50		52	ms	DTMF mode
11		Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
12		Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
13	TONE OUT	High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L = 10kΩ
14		Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L = 10kΩ
15		Pre-emphasis	dB_P		2	3	dB	R_L = 10kΩ
16		Output distortion (single tone)	THD		-25		dB	25 kHz Bandwidth R_L = 10 kΩ
17		Frequency deviation	f_D	±0.7		±1.5	%	f_C=3.579545 MHz
18		Output load resistance	R_{LT}	10		50	kΩ	
19	MPU INTERFACE	Φ2 cycle period	t_{CYC}	1		1000	µs	
20		Φ2 high pulse width	t_{CH}	450			ns	
21		Φ2 low pulse width	t_{CL}	430			ns	
22		Φ2 rise and fall time	t_{R,t_F}			25	ns	
23		Address, R/$\overline{W}$ hold time	$t_{AH,t_{RWH}}$	26			ns	
24		Address, R/$\overline{W}$ set up time (before Φ2)	$t_{AS,t_{RWS}}$	23			ns	
25		Data hold time (read)	t_{DHR}	22			ns	*
26		Φ2 to valid data delay (read)	t_{DDR}			290	ns	200 pF load
27		Data set up time (write)	t_{DSW}	45			ns	
28		Data hold time (write)	t_{DHW}	10			ns	
29		Input Capacitance (data bus)	C_{IN}		5		pF	
30		Output Capacitance ($\overline{IRQ}$/CP)	C_{OUT}		5		pF	

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AC Electrical Characteristics† (Cont'd)- Voltages are with respect to ground (V$_{SS}$) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
31	DTMF	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
32		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
33		Clock input duty cycle	t_{HLCL}			110	ns	Ext. clock
34		Clock input duty cycle	DC$_{CLO}$	40	50	60	%	Ext. clock
35		Capacitive load (OSC2)	C_{LO}			30	pF	

† Timing is over recommended temperature & power supply voltages. f_C = 3.579545 MHz

‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

* The data bus output buffers are no longer sourcing or sinking current by t_{DHR}.

See Figure 7 regarding guard time adjustment.

NOTES: 1) dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2) Digit sequence consists of all 16 DTMF tones.
3) Tone duration = 40 ms. Tone pause = 40 ms.
4) Nominal DTMF frequencies are used.
5) Both tones in the composite signal have an equal amplitude.
6) The tone pair is deviated by ± 1.5 % ± 2 Hz.
7) Bandwidth limited (3 kHz) Gaussian noise.
8) The precise dial tone frequencies are 350 and 440 Hz (± 2 %).
9) For an error rate of less than 1 in 10,000.
10) Referenced to the lowest amplitude tone in the DTMF signal.
11) Referenced to the minimum valid accept level.
12) For guard time calculation purposes.

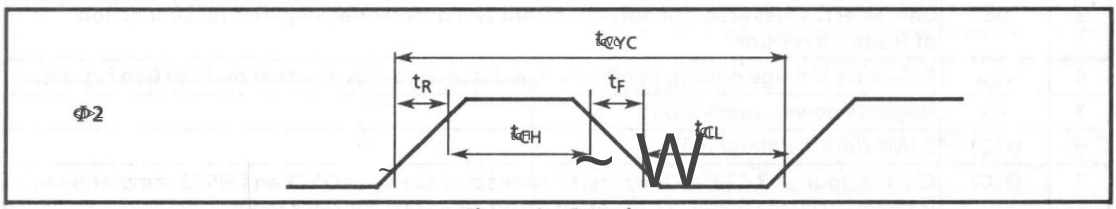

Figure 2 - Φ2 Pulse

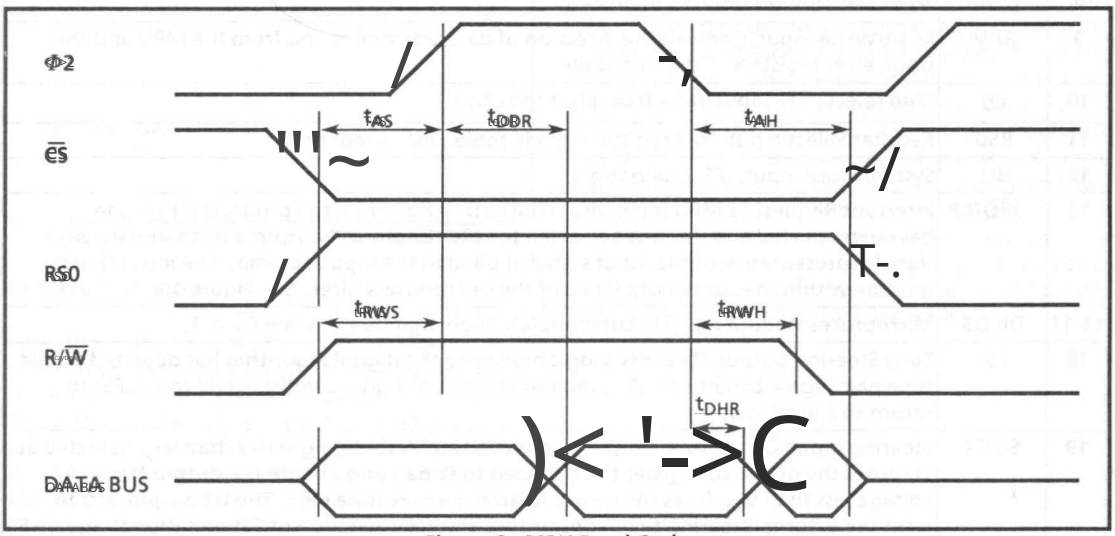

Figure 3 - MPU Read Cycle

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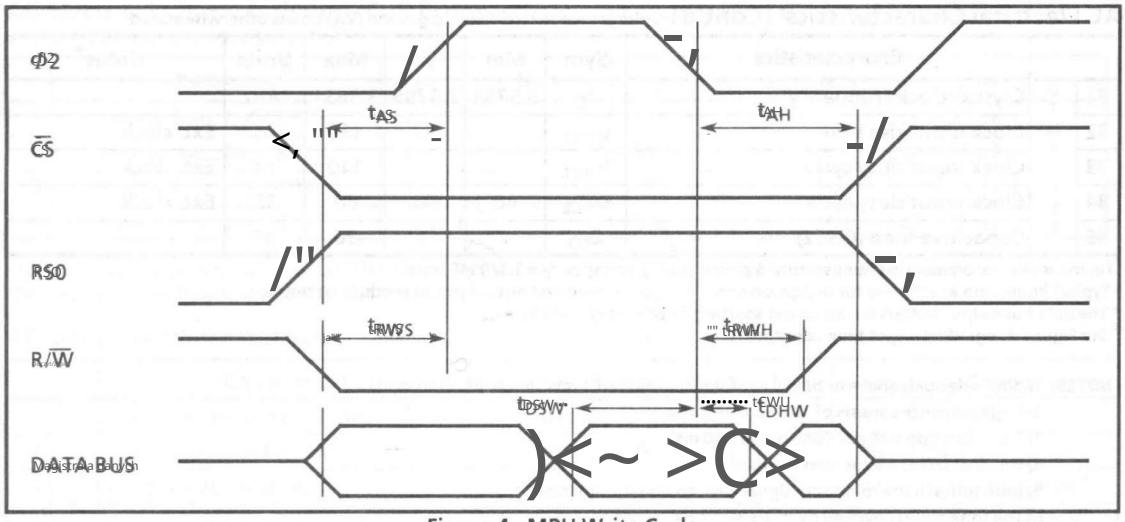

Figure 4 - MPU Write Cycle

Figure 4 - Cykl zapisu MPU

Pin Description

Pin #	Name	Description
1	IN+	Non-inverting op-amp input.
2	IN−	Inverting op-amp input.
3	GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.
4	V_{Ref}	Reference Voltage output, nominally $V_{DD}/2$, is used to bias inputs at mid-rail (see Fig. 15).
5	V_{SS}	Negative power supply input.
6	OSC1	DTMF clock oscillator input.
7	OSC2	Clock output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is clock input.
8	TONE	Dual Tone Multi Frequency output.
9	R/$\overline{W}$	Read/Write input. Controls the direction of data transfer to and from the MPU and the transceiver registers. TTL compatible.
10	$\overline{CS}$	Chip select TTL input ($\overline{CS}$ = 0 to select the chip).
11	RS0	Register select input. See register decode table. TTL compatible.
12	Φ2	System Clock input. TTL compatible.
13	$\overline{IRQ}/CP$	Interrupt Request to MPU (open drain output). Also, when call progress (CP) mode has been selected and interrupts enabled the $\overline{IRQ}/CP$ pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 10.
14-17	D0-D3	Microprocessor data bus (TTL compatible). High impedance when $\overline{CS}$ = 1.
18	ESt	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition) and a logic low if the detected signal condition will cause ESt to return to a logic low.
19	St/GT	Steering Input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St.
20	V_{DD}	Positive power supply input.

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Functional Description

The MT8880 integrated DTMF transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator which employs a burst counter such that precise tone bursts and pauses can be synthesized. A call progress mode can be selected such that frequencies within the specified passband may be detected. A standard microprocessor interface allows access to an internal status register, two control registers and two data registers.

Input Configuration

The input arrangement of the MT8880 provides a differential input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 5.

Figure 6 shows the necessary connections for a differential input configuration.

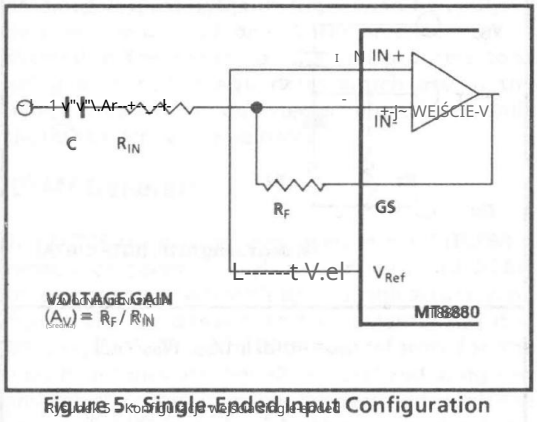

Figure 5 - Single-Ended Input Configuration

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Fig. 9). The low group filter also incorporates notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

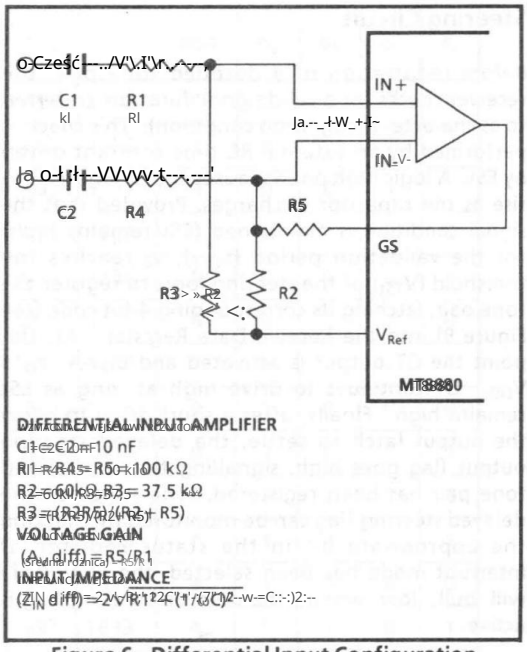

Figure 6 - Differential Input Configuration

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation due to talk-off. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

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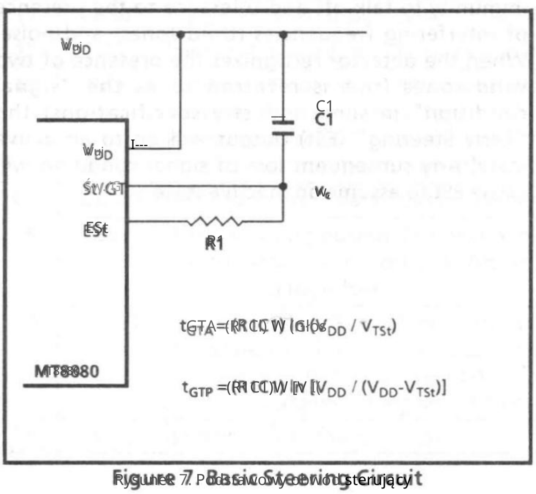
Obwód sterujący

Przed zarejestrowaniem zdekodowanej pary tonów, odbiornik sprawdza, czy czas trwania sygnału jest prawidłowy (tzw. jako warunek rozpoznawania znaków). To jest sprawdzenie wykonywane przez zewnętrzną stałą czasową RC sterowaną przez ESt. Wysoki poziom logiczny ESt powoduje, że v_c (patrz rysunek 7) wzrasta w miarę rozładowywania się kondensatora. Pod warunkiem, że stan sygnału jest utrzymywany (ESt pozostaje wysoki) w okresie walidacji (t_{GTP}), v_c osiąga próg (V_{TSt}) logiki sterowania w celu zarejestrowania pary tonów, zatrzaskując odpowiadający jej 4-bitowy kod (patrz Rysunek 9) do rejestru danych odbiorczych. W tym momencie punkt, w którym wyjście GT jest aktywowane i napędza v_c do V_{DD}. GT nadal będzie jeździć wysoko, dopóki ESt pozostaje wysoki. W końcu, po krótkim opóźnieniu, aby umożliwić zatrzask wyjściowy do ustalenia, opóźniony sterowanie flaga wyjściowa przechodzi w stan wysoki, sygnalizując, że odebrano para tonów została zarejestrowana. Status Opóźnioną flagę sterowniczą można monitorować, sprawdzając odpowiedni bit w rejestrze statusu. Jeśli Wybrano tryb przerwania, pin IRQ/CP będzie pociągnij nisko, gdy opóźniona flaga skrętu zostanie aktywna.

Zawartość zatrzasku wyjściowego jest aktualizowana na aktywnym opóźnionym sterowaniu. Te dane są przesyłane prezentowane do czterobitowego dwukierunkowego, gdy magistrala danych odczytywany jest rejestr danych odbiorczych. Obwód sterujący działa odwrotnie, aby sprawdzić pauzę między cyfrowymi między sygnałami. W ten sposób, jak również odrzucanie sygnałów zbyt krótkich, aby można je było uznać za ważne, odbiornik będzie tolerował przerwy w sygnale (spadek (out) zbyt krótki, aby uznać go za ważną pauzę. Ten obiekt wraz z możliwością wyboru stałe czasowe sterowania pozwalają zewnętrznie, projektantowi umożliwiają dostosowanie spełniać szeroką gamę wydajności do różnorodnych wymagań systemowych.



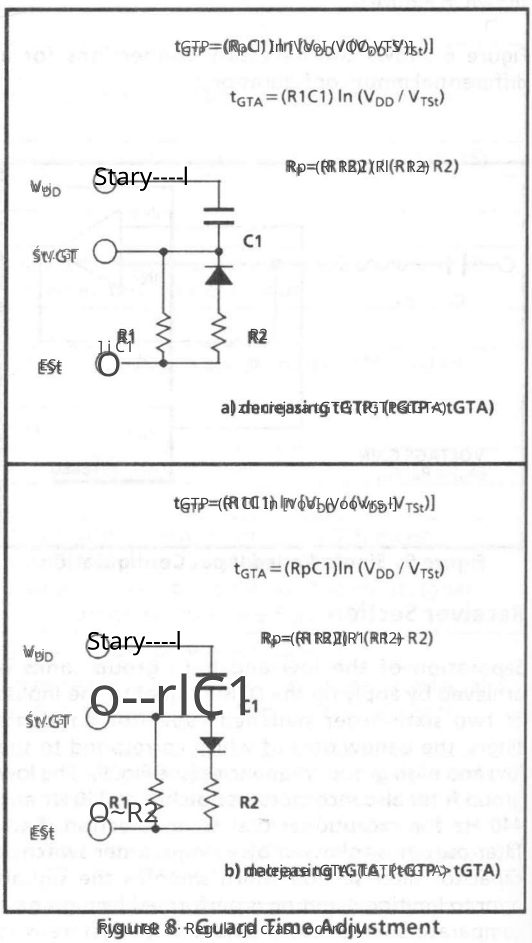
Rysunek 7. Podstawowy obwód sterujący

Regulacja czasu ochrony

Proste sterowanie obwód pokazany na rysunku 7 jest odpowiednie dla większości zastosowań. Wartości komponentów wybiera się według wzoru:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

Wartość t_{DP} jest parametrem urządzenia (patrz AC Charakterystyki elektryczne) i t_{REC} jest wartością minimalną czas trwania sygnału, który ma zostać rozpoznany przez odbiornik. A dla większości zaleca się wartość C1 wynoszącą 0,1 µF aplikacje, pozostawiając R1 do wyboru przez projektant. Mogą być różne układy kierownicze służy do niezależnego wyboru godzin warty dla ton obecny (t_{GTP}) i ton nieobecny (t_{GTA}). Może to być konieczne, aby spełnić specyfikacje systemu, które umieścić oba limity akceptacji i odrzucenia na obu tonach czas trwania i przerwa cyfrowa. Czas ochrony regulacja pozwala również projektantowi dostosować system parametry takie jak wyłączenie mowy i odporność na zakłócenia.



Rysunek 8 · Regulacja czasu ochrony

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Increasing TREC improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short TREC with a long TDO would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop outs are required. Design information for guard time adjustment is shown in Figure 8. The receiver timing is shown in Figure 11 with a description of the events in Figure 13.

Call Progress Filter

A call progress mode using the MT8880/MT8880-1, can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The MT8880-2 does not offer the call progress function. The call progress tone input and DTMF input are common however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 5). Figure 10 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input which are within the 'accept' bandwidth limits of the filter are hard-limited by a high gain comparator with the IRQ/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analysed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the IRQ/CP pin will remain low.

DTMF Generator

The DTMF transmitter employed in the MT8880 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal data conforming to the encoding format shown in Figure 9 must be written to the transmit data register. Note that this is the same code as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically the high group to low group

DIGIT	D_3	D_2	D_1	D_0	f_{LOW}	f_{HIGH}
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

0 = LOW LOGIC LEVEL, 1 = HIGH LOGIC LEVEL

Figure 9 - Functional Encode/Decode Table

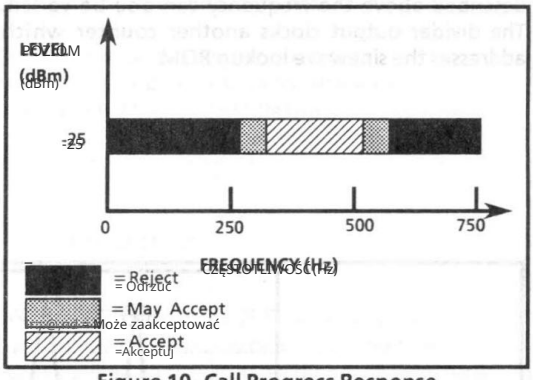

Figure 10 - Call Progress Response

amplitude ratio (twist) is 2 dB to compensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify time segment length which will ultimately determine the

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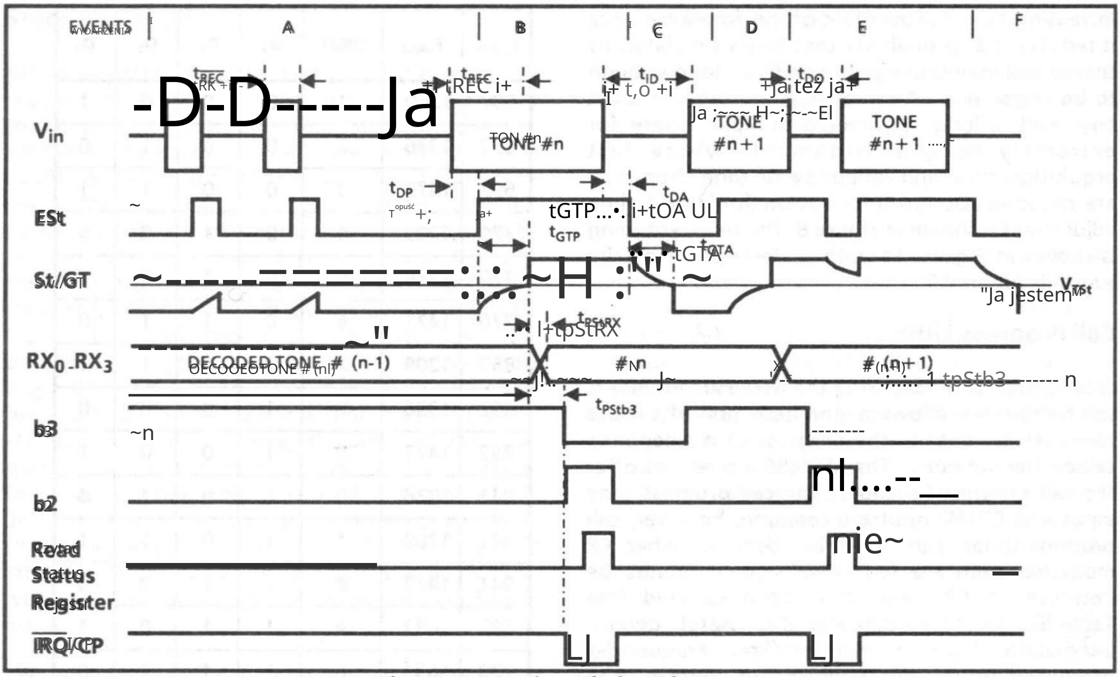
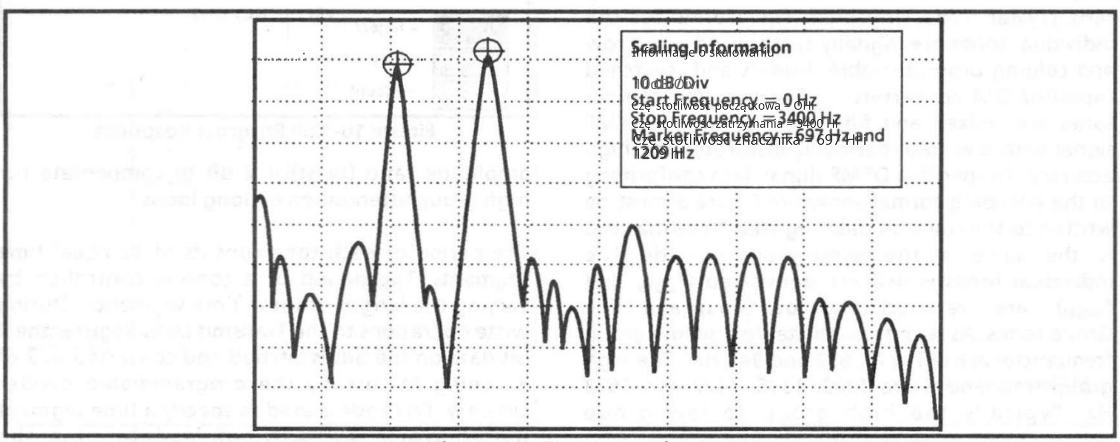


Rysunek 11 - Diagram czasowy odbiornika

częstotliwość tonu. Kiedy dzielnik osiągnie odpowiednią liczbę ustaloną na podstawie danych wejściowych kod, wysyłany jest impuls resetujący licznik i zaczyna mierzyć ponownie. Liczba segmentów czasowych jest ustalona na 32, jednakże poprzez zmianę długości segmentu jako jak opisano powyżej, częstotliwość może być również zmieniona. Wyjście dzielnika taktuje inny licznik, który adresuje pamięć ROM wyszukiwania fali sinusoidalnej.

Tabela wyszukiwania zawiera kody, które są używane przez Konwerter C/A z przełączanym kondensatorem w celu uzyskania dyskretne i wysoce dokładne poziomy napięcia DC. Dwa identyczne obwody są używane do produkcji wierszy i kolumn tonów, które są następnie mieszane przy użyciu niskiego wzmacniacz sumujący szum. Opisany oscylator nie wymaga części „rozruchu” jak w przypadku innych DTMF generatory, ponieważ oscylator kwarcowy jest uruchomiony nieprzerwanie, zapewniając wysoki poziom tonu dokładność. Filtr ograniczający przepustowość jest włączony szeregowo w celu tłumienia zniekształceń produkty powyżej 8 kHz. Można to zobaczyć na rysunku 12 że produkty zniekształceń są bardzo niskie amplituda.



Rysunek 12 - Wykres widma

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Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms ±1 ms, which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, a secondary burst/pause time is available such that this interval is extended to 102 ms ±2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In certain applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation and distortion measurements. Refer to Control Register B description for details.

Distortion Calculations

The MT8880 is capable of producing precise tone bursts with minimal error in frequency (see Table 1). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to V_{2f} .... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H

3

EXPLANATION OF EVENTS

- A) TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
- B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
- C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
- D) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
- E) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
- F) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ALSO INDICATES THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
IRQ/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 13 - Description of Timing Events

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$$THD(\%) = 100 \frac{\left(\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \ldots . V_{nf}^2}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

Równanie 1. THD (%) dla pojedynczego tonu

$$THD(\%) = 100 \frac{\left(\sqrt{V_{2L}^2 + V_{3L}^2 + \ldots . V_{nL}^2 + V_{2H}^2 + V_{3H}^2 + .. V_{nH}^2 + V_{IMD}^2}\right)}{\sqrt{V_L^2 + V_H^2}}$$

Equation 2. THD (%) For a Dual Tone

Równanie 2. THD (%) dla tonu dwutonowego

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		% ERROR
	DESIRED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 1. Actual Frequencies Versus Standard Requirements

correspond to the low group amplitude and high group amplitude respectively and V^2_{IMD} is the sum of all other intermodulation components. The internal switched capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 12.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal being a resonant frequency of 3.579545 MHz. A number of MT8880 devices can be connected as shown in Figure 14 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer (capacitive coupling) with the OSC2 outputs left unconnected.

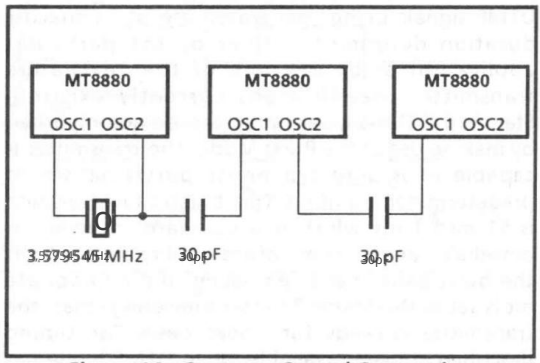

Figure 14. Common Crystal Connection

Microprocessor Interface

The MT8880 employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, ie; data transfer, transceiver control and transceiver status. There are two registers associated with data transfer operations. The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read only register. The data entered in the Transmit Data Register will determine which tone pair is to be generated (see Figure 9 for coding details). Data can only be written to the transmit register. Transceiver control is accomplished with two Control Registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. A software reset must be included at the beginning of all programs to initialize the control registers after power up or power reset (see Figure 18). Refer to Tables 3, 4, 5 and 6 for details concerning the Control Registers. The IRQ/CP pin can be programmed such that it will provide an interrupt request signal upon validation of DTMF signals or when the transmitter is ready for more data (Burst mode only). The IRQ/CP pin is configured as an open drain output device and as such requires a pull up resistor (see Figure 15).

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RS0	R/$\overline{W}$	FUNCTION
0	0	Write to Transmit Data Register
0	1	Read from Receive Data Register
1	0	Write to Control Register
1	1	Read from Status Register

Table 2 - Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 3 - CRA Bit Positions

b3	b2	b1	b0
C/$\overline{R}$	S/$\overline{D}$	TEST	BURST

Table 4 - CRB Bit Positions

BIT	NAME	FUNCTION	DESCRIPTION
b0	TOUT	TONE OUTPUT	A logic '1' enables the tone output. This function can be implemented in either the burst mode or non-burst mode.
b1		MODE CONTROL	In DTMF mode (logic '0') the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1') a 6th order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones which are within the specified bandwidth will be presented at the $\overline{IRQ}$/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 = 1). Also, when the CP mode and BURST mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode of operation has been selected.
b2	IRQ	INTERRUPT ENABLE	A logic '1' enables the INTERRUPT mode. When this mode is active and the DTMF mode has been selected (b1 = 0) the $\overline{IRQ}$/CP pin will pull to a logic '0' condition when either 1) a valid DTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (BURST mode only).
b3	RSEL	REGISTER SELECT	A logic '1' selects Control Register B on the next Write cycle to the Control Register address. Subsequent Write cycles to the Control Register are directed back to Control Register A.

Table 5 - Control Register A Description

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BIT	NAME	FUNCTION	DESCRIPTION
b0	BURST	BURST MODE	A logic '0' enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Register resulting in a tone burst of a specific duration (see AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Register is ready for further instructions and an interrupt will be generated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic '1') tone bursts of any desired duration may be generated.
b1	TEST	TEST MODE	By enabling the test mode (logic '1'), the IRQ/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 11 (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1 = 0) before test mode can be implemented.
b2	S/$\overline{D}$	SINGLE/DUAL TONE GENERATION	A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single tone generation is enabled (logic '1'), either row or column tones (low group or high group) can be generated depending on the state of b3 in Control Register B.
b3	C/$\overline{R}$	COLUMN/ROW TONES	When used in conjunction with b2 (above) the transmitter can be made to generate single row or single column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies.

Table 6 - Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) and/or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 7 - Status Register Description

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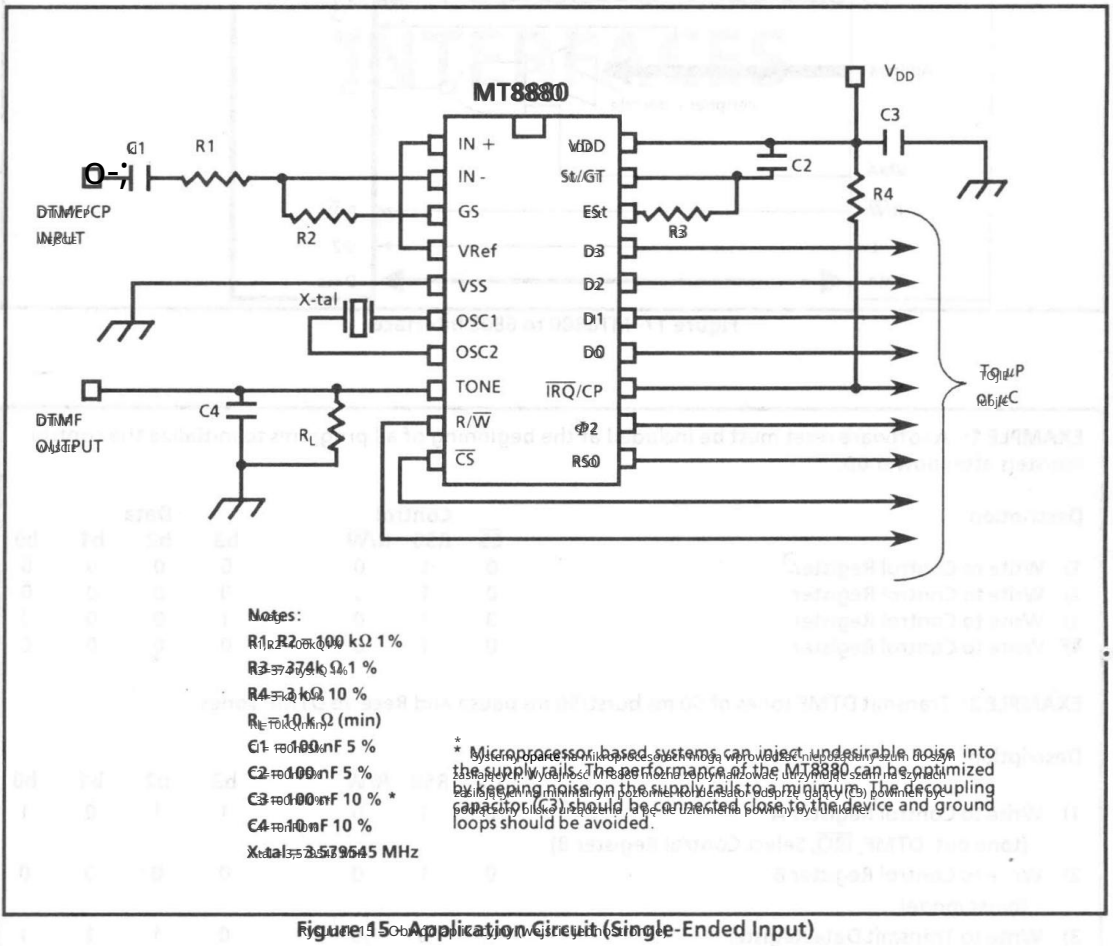

Figure 15 - Application Circuit (Single-Ended Input)

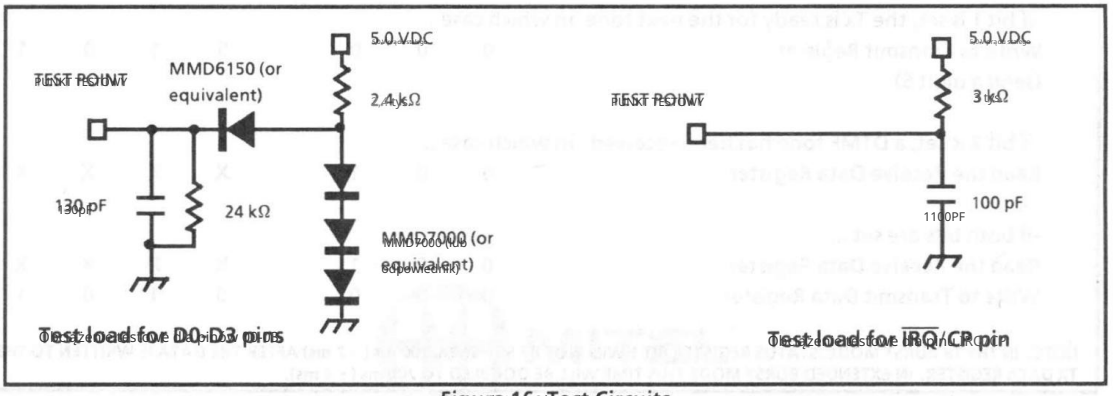

Figure 16 - Test Circuits

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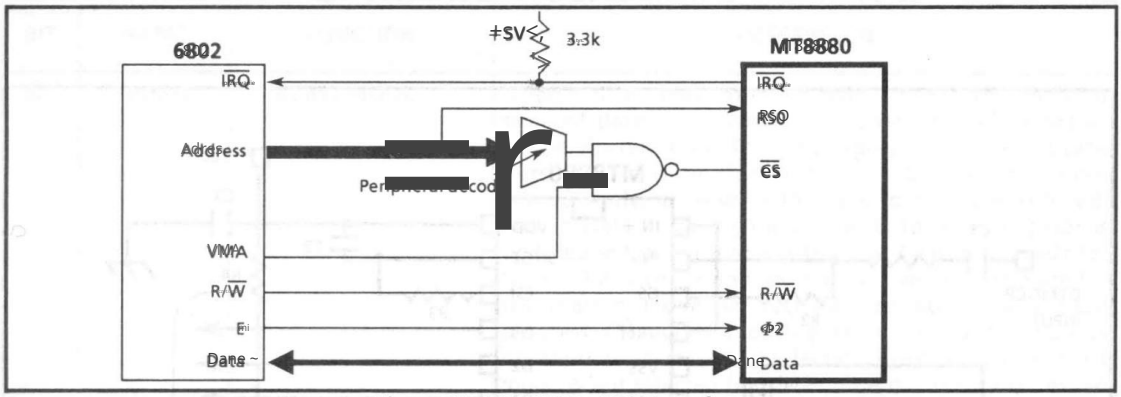

Figure 17. MT8880 to 6802 Interface

EXAMPLE 1: A software reset must be included at the beginning of all programs to initialize the control registers after power up:

Description	Control			Data			
	CS	RS0	R/W	b3	b2	b1	b0
1) Write to Control Register	0	1	0	0	0	0	0
2) Write to Control Register	0	1	0	0	0	0	0
3) Write to Control Register	0	1	0	1	0	0	0
4) Write to Control Register	0	1	0	0	0	0	0

EXAMPLE 2: Transmit DTMF tones of 50 ms burst / 50 ms pause and Receive DTMF Tones

Description	CS	RS0	R/W	b3	b2	b1	b0
1) Write to Control Register A (tone output, DTMF, IRQ, Select Control Register B)	0	1	0	1	1	0	1
2) Write to Control Register B (burst mode)	0	1	0	0	0	0	0
3) Write to Transmit Data Register (send digit 7)	0	0	0	0	1	1	1
wait for an interrupt or poll Status Register							
4) Read the Status Register	0	1	1	X	X	X	X
if bit 1 is set, the Transmit Data Register is ready for the next tone, in which case							
Write to Transmit Register (send digit 5)	0	0	0	0	1	0	1
if bit 2 is set, a DTMF tone has been received, in which case							
Read the Receive Data Register	0	0	1	X	X	X	X
if both bits are set ...							
Read the Receive Data Register	0	0	1	X	X	X	X
Write to Transmit Data Register	0	0	0	0	1	0	1

NOTE: IN THE BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (± 2 ms) AFTER DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 18. Application Hints

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LINE AND TRUNK INTERFACES

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MH88500

Hybrid Subscriber Line Interface Circuit (SLIC)

September 1981

Features

- Differential to single ended conversion
- No transformers required
- Minimum installation space
- Off-hook detection and LED indicator drive
- Relay drive output
- Battery and ringing feed to line
- Logic Interface - MUTE, OFHK, RC
- Mute of incoming audio
- Dial pulse detection
- Voltage surge protection

Applications

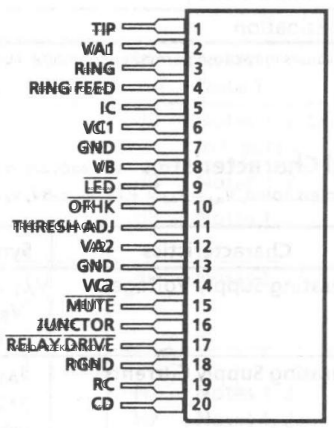
Interface for:

- PABX
- Intercoms
- Key Systems

Description

The Mitel MH88500 Subscriber Line Interface Circuit provides complete interface between the telephone line and a speech switch requiring only a single bidirectional switch per crosspoint. The functions provided by the MH88500 include bidirectional differential to single ended conversion in the speech path, line battery feed, ringing feed and loop and dial pulse detection. The device is fabricated using thick film hybrid technology in a 20-pin 'single in line' package allowing optimum circuit board packing density.

Pin Connections



Ordering Information

MH88500-20 Pin SIL Package

0°C to 70°C

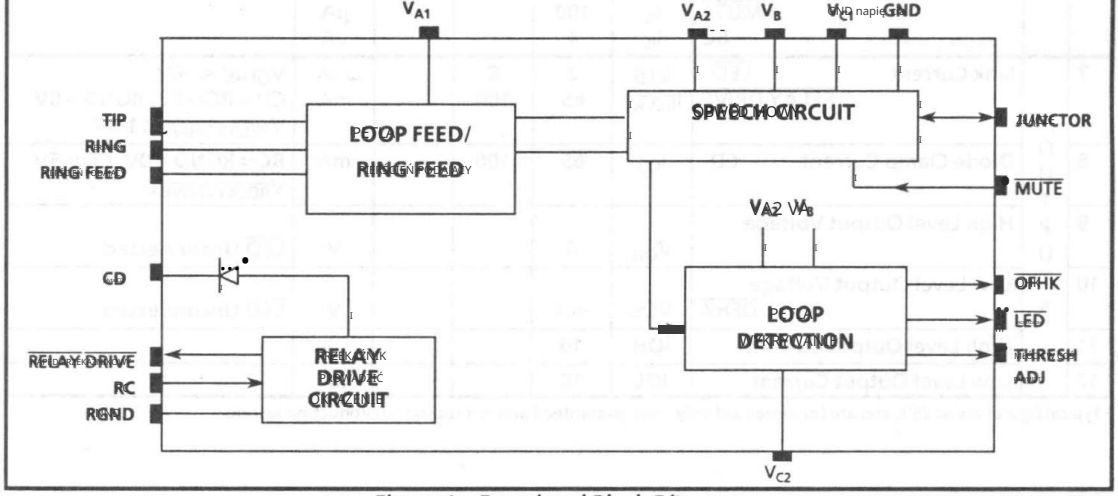


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne wartości bezwzględne*

	Parameter	Symbol	Min	Max	Units
1	Voltage Supplies V_{A1}, V_{A2}, V_B, V_{C1}, V_{C2} to GND	V_{A1}, V_{A2} V_B V_{C1}, V_{C2}	-18 -35	+18	
2	Clamp Diode Breakdown Voltage V_{Ref} to RGND	V_{RGD}		+15	
3	Operating Temperature	T_{AMB}	0	+70	°C
4	Storage Temperature	T_{STG}	-40	+100	°C
5	Power Dissipation	P_D		1.2	Watt

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

Charakterystyka elektryczna prądu stałego (napięcia odniesione do masy (Vss), T_A od 0 do +70°C, chyba że podano inaczej

Test Conditions (unless noted otherwise) $V_{A1} = V_{A2} = V_B = V_{C1} = V_{C2} = 24V$.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	SUPPLY	Operating Supply Voltages Napięcia zasilania roboczego	V_{A1}, V_{A2} V_B V_{C1}, V_{C2}	-13 -25		-13 -25	V V V	
2		Operating Supply Currents Prądy robocze zasilania	I_{A1} I_{A2} I_B I_{C1} I_{C2}		7 8 6 .2 .1		mA mA mA mA mA	
3	INPUTS	High Level Input Voltage Wysoki poziom napięcia wejściowego $\overline{MUTE}$ RC	V_{IH} V_{IH}	4.2 3			V V	
4		Low Level Input Voltage Niski poziom napięcia wejściowego $\overline{MUTE}$ RC	V_{IL} V_{IL}			.8 1	V V	
5		High Level Input Current Prąd wejściowy o wysokim poziomie $\overline{MUTE}$ RC	I_{IH} I_{IH}	-28 700			µA µA	
6		Low Level Input Current Prąd wejściowy o niskim poziomie $\overline{MUTE}$ RC	I_{IL} I_{IL}	100 1			µA µA	
7	OUTPUTS	Sink Current Prąd zaciskowy $\overline{LED}$ $\overline{RELAY\ DRIVE}$	$I_{\overline{LED}}$ $I_{\overline{RELAY\ DRIVE}}$	2 65	6 100		mA mA	$V_{OH} = V_{\overline{LED}} < -6V$ CD=RC=5V, RGND=0V $V_{\overline{RELAY\ DRIVE}} < 1.5V$
8		Diode Clamp Current Prąd zaciskowy diodowego CD	I_{CD}	65	100		mA	RC=RGND=0V, CD=5V $V_{\overline{RELAY\ DRIVE}} >$
9		High Level Output Voltage Wysoki poziom napięcia wyjściowego	V_{OH}	6			V	Dioda LED podłączona $\overline{LED}$ Unconnected
10		Low Level Output Voltage $\overline{OHMKOM}$	V_{OL}			-6.5	V	Dioda LED podłączona $\overline{LED}$ Unconnected
11		High Level Output Current Wysoki poziom prądu wyjściowego	I_{OH}	10			µA	
12		Low Level Output Current Niski poziom prądu wyjściowego	IOL	10			µA	

†Typical figures are at 25°C and are for design aid only - not guaranteed and not subject to production testing.

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AC Electrical Characteristics[†]

Voltages are with respect to ground (V_{SS}), $T_A = 25°C$, unless otherwise stated.
Test Conditions unless otherwise stated, $V_{AZ} = +7V$, $V_B = -8V$, $V_{C1} = V_{C2} = -24V(\pm 5\%)$.

	Characteristics		Sym	Min	Typ[‡]	Max	Units	Test Conditions
1	Junctor to differential output (tip-ring) gain.		A_{JL}	2.18	2.25	2.32	V/V	1kHz, 400mV$_{RMS}$ Source on Pin 16. Note 2.
2	Differential Input (tip, ring) to junctor gain.		A_{LJ}	0.303	0.312	0.321	V/V	1kHz, 1V$_{RMS}$. Source applied on pins 1&3. Notes 1,2.
3	On/Off Hook Detection Threshold.	Loop Resist	R_{Thresh}	4.0	5.4	6.0	kΩ	Note 1.
		Loop Current	I_{Thresh}	3.6	4.0	5.3	mA	Note 1.
4	Trans Hybrid Loss				55		dB	Notes 1,2. See test circuit in Figure 2.
5	Passband Linearity				±1		dB	Notes 1, 2.
6	Power Supply Rejection Ratio (V_C to Junctor)		PSRR		40		dB	Notes 1, 2.
7	Common Mode Rejection Ratio (Tip and Ring to Junctor)		CMRR		40		dB	Notes 1, 2.
8	Low Frequency Cutoff (3dB)	Junctor to Line	F_{LJ}		53		Hz	Notes 1, 2.
		Line to Junctor	F_{JL}		20		Hz	Notes 1, 2.
9	High Frequency Cutoff (3dB)	Line to Junctor	F_{HLJ}		800		kHz	Notes 1, 2.
		Junctor to Line	F_{HJL}		500		kHz	Notes 1, 2.
10	Longitudinal Balance				65		dB	Note 1.
11	Tip (or ring) to ground AC input impedance		Z_I		300		Ω	
12	Junctor output impedance		Z_{OJ}		604		Ω	

‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

Note 1: 754 ohms connected between JUNCTOR (pin 16) and 0 volts.

Note 2: 604 ohms connected between TIP (pin 1) and RING (pin 3).

4

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Pin Description

Pin #	Name	Description
1	TIP	Connection to Telephone "TIP" Wire.
2	V_{A1}	Positive Line Feed Supply Voltage. Normally connected to V_{A2}.
3	RING	Connection to Telephone "RING" Wire.
4	RING FEED	Negative Line Feed Voltage and Ringing Input. Normally connected to ring relay.
5	IC	Internal Connection. Leave open circuit. Use for testing only.
6	V_{C1}	Sense Input. Normally connected to negative line feed voltage supply.
7	GND	Analog Ground (0V). Internally connected to pin 13.
8	V_B	Negative Analog Supply Voltage.
9	$\overline{LED}$	LED Drive Output (Off-Hook condition, logic low).
10	$\overline{OFHK}$	Logic Low Output. Indicates closed loop condition (Off-Hook and dial pulsing).
11	THRESH ADJ.	Allows adjustment of OFHK detection threshold.
12	V_{A2}	Positive Analog Supply Voltage. Normally connected to V_{A1}.
13	GND	Analog Ground (0V). Internally connected to pin 7.
14	V_{C2}	Loop Detector Voltage Supply. Connect to negative line feed voltage supply.
15	$\overline{MUTE}$	Input Mutes the Incoming Audio. Active low.
16	JUNCTOR	Receive/transmit audio speech path (referenced to 0V GND).
17	$\overline{RELAY}$ $\overline{DRIVE}$	Relay Driver Output. Open collector sinks current when RC is high. Diode clamp protected.
18	RGND	Ground for Relay Drive Circuit.
19	RC	Relay Control Input. Active high.
20	CD	Clamping Diode. Normally connected to relay positive supply voltage.

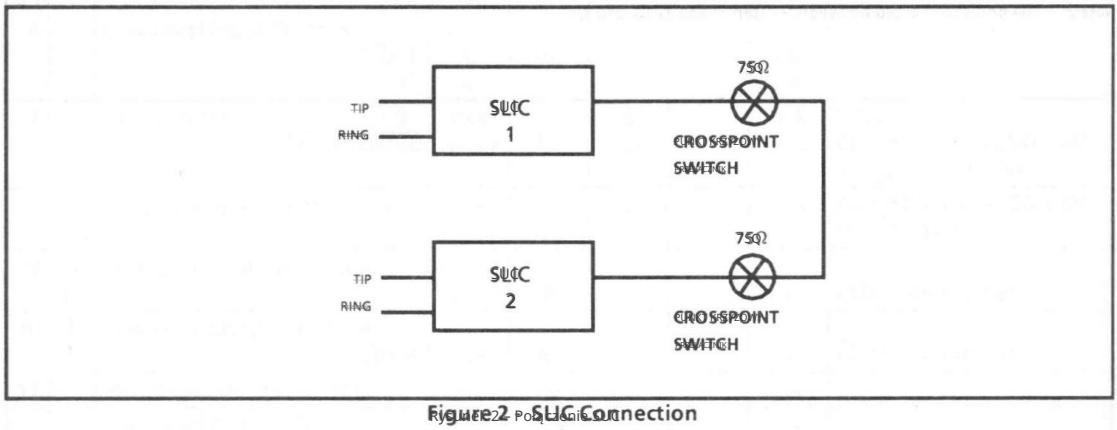

Figure 2 SLIC Connection

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Functional Description

Speech Circuit

The speech circuit converts the bidirectional TIP and RING line pair to a bidirectional single ended internal channel. Figure 2 illustrates a typical connection between two SLIC's through two crosspoint switches. This configuration gives optimum transhybrid loss as seen from Figure 3 given that the output impedance of the junctor line is 600 Ω.

The $\overline{MUTE}$ input signal mutes signals coming from TIP and RING to the junctor while allowing the signal from the junctor, to be transmitted.

Loop Detection

The loop detection circuit determines whether a low external impedance across TIP and RING is to be recognized as an off-hook condition. (The threshold impedance is 5.4 kΩ with no adjustment.) This threshold level can be adjusted by the use of external resistors as shown in Figure 5. OFHK has low output drive capability so it may drive CMOS operating with different power supplies.

Line Feed/Ring Feed Circuit

The line feed circuit provides loop current and the ability to apply ringing voltage to TIP and RING. The impedance from RING FEED to GND is 600Ω which gives the loop current as:

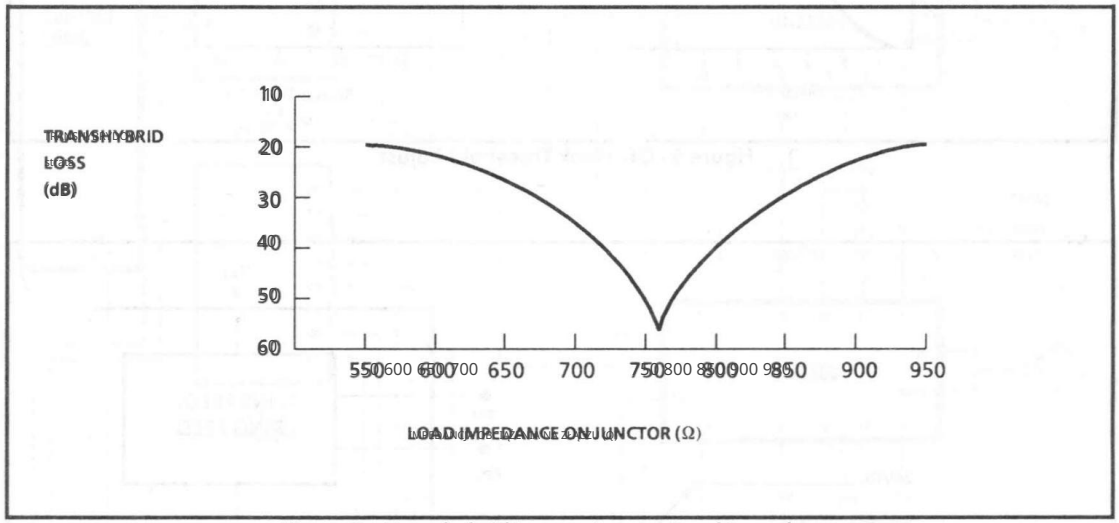

Figure 3 - Transhybrid Loss vs Junctor Load Impedance

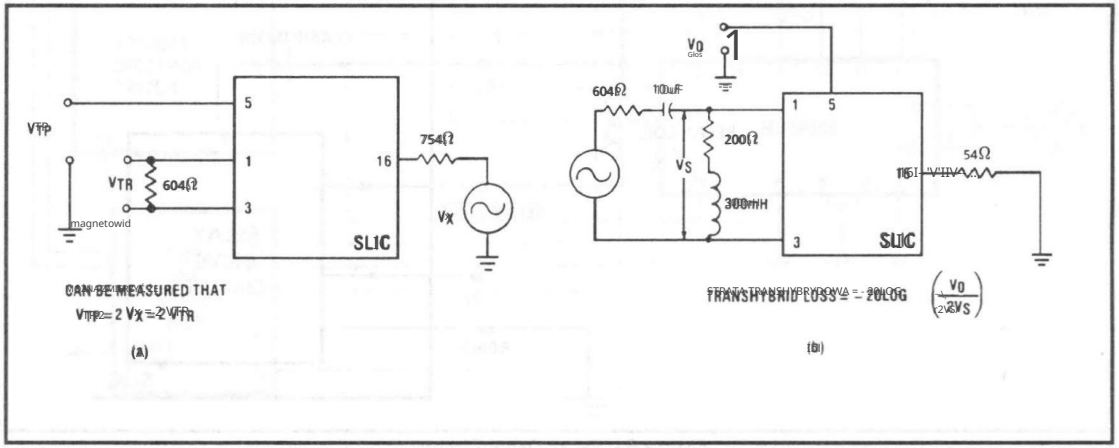

Figure 4 - Transhybrid Loss Test Circuit

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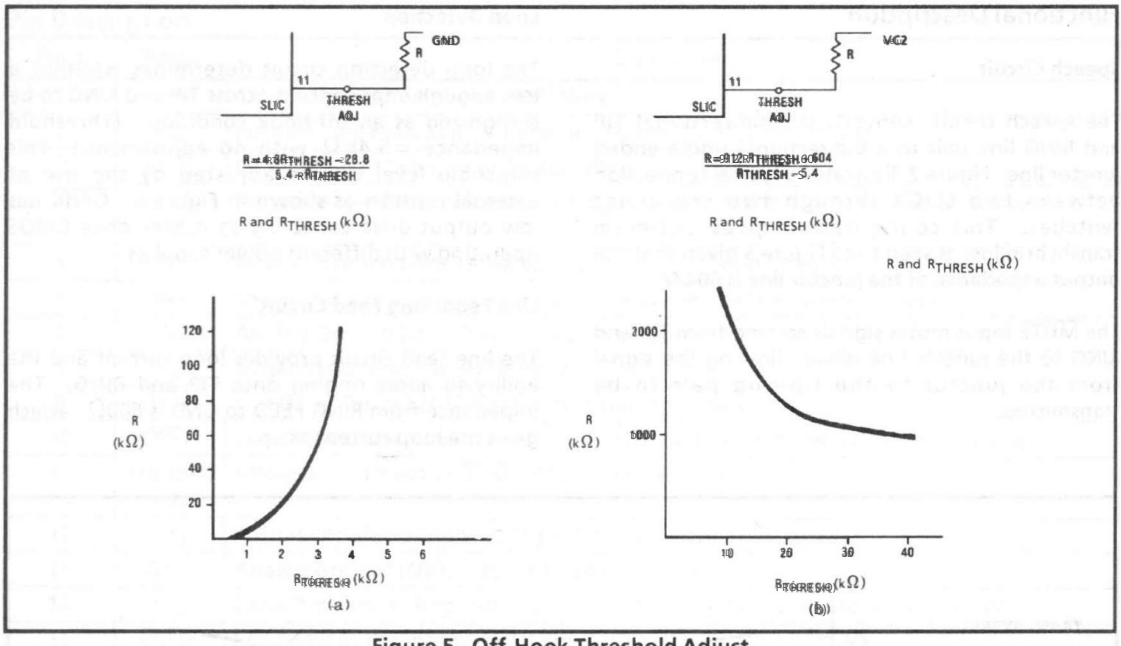

Figure 5 - Off-Hook Threshold Adjust

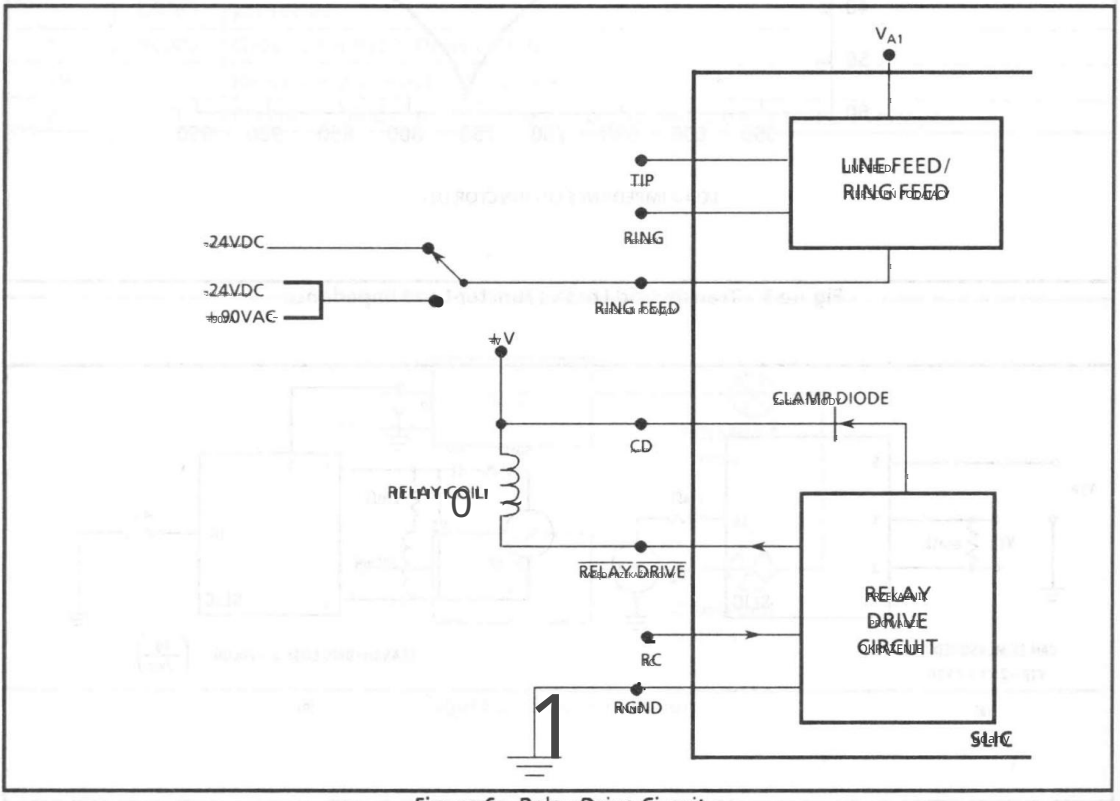

Figure 6 - Relay Drive Circuit

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Voltage at RING FEED pin — AMP
Telephone Impedance — 600

The positive supply for the line feed circuit is V_{A1} through the loop current is determined from RING FEED and GND.

Relay Drive Circuit

The relay drive circuit switches ringing into RING FEED (Fig. 6). The diode is present to suppress voltage transients during relay switching caused by the inductive coils of the relay. Ringing Voltage includes AC ringing (90V typically) and DC line feed voltage (24V typically).

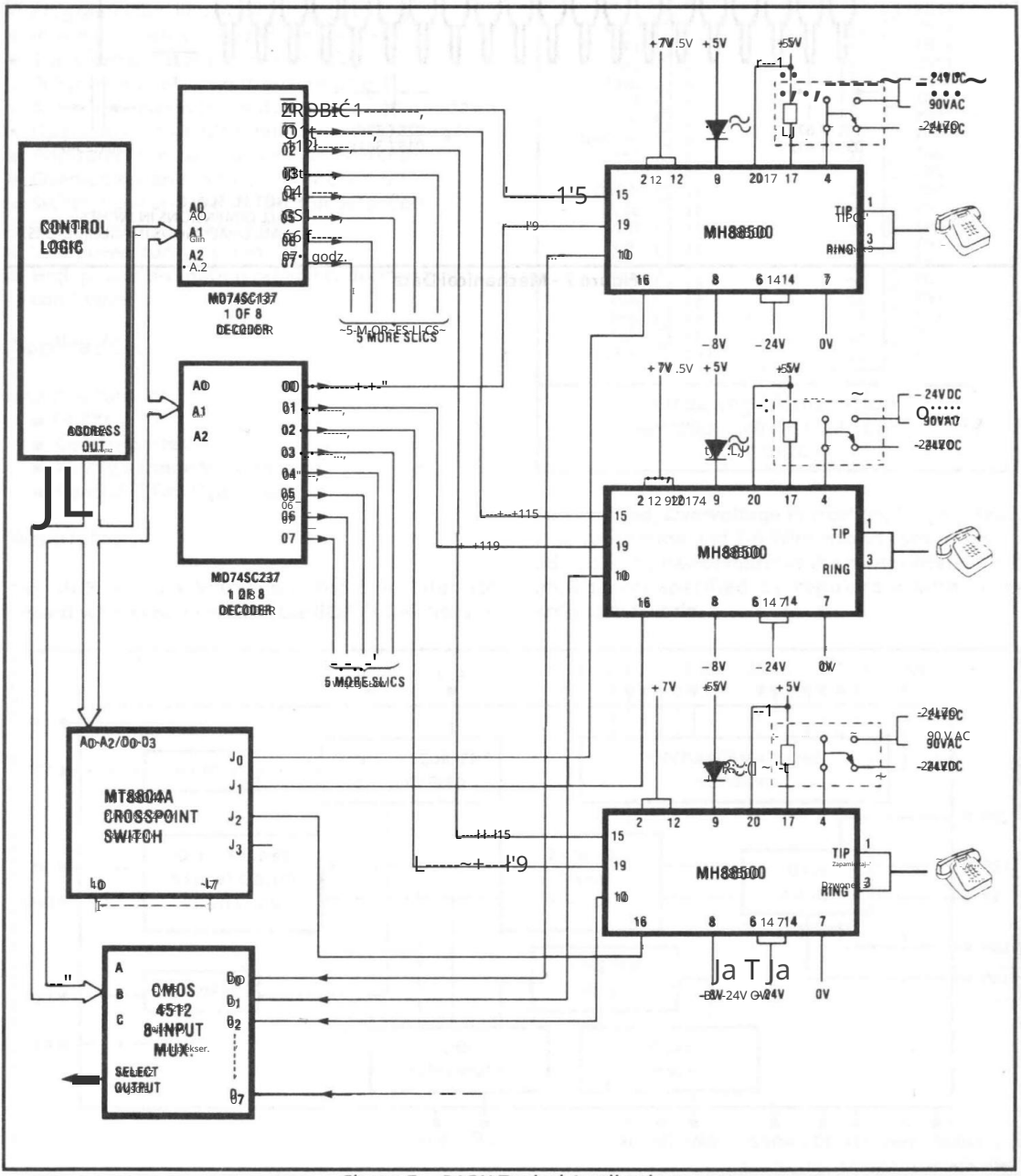

Figure 7 - PABX Typical Application

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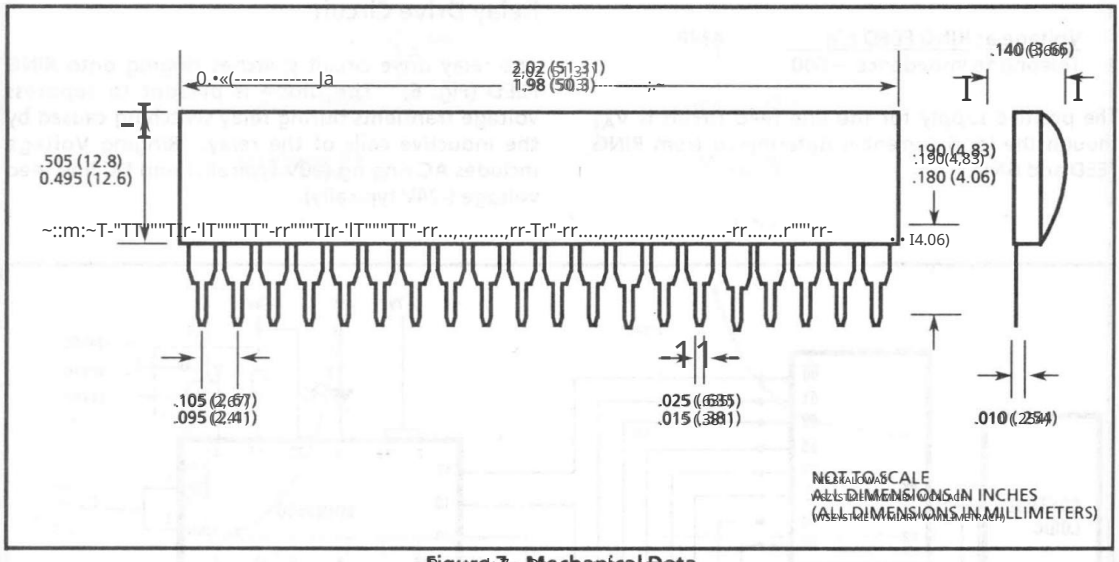

Figure 7 - Mechanical Data

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9161-002-129-NA ISSUE 3 November 1990
Wydanie 3 Listopad

Features
Cechy

- Programmable line impedance matching
  Programowalne dopasowanie impedancji linii
- Internal complex impedance networks
  Sieci złożonej impedancji wewnętrznej
- Transformerless 2-4 wire conversion
  Konwersja 2-4 przewodów bez transformatora
- Programmable transmit/receive gain
  Programowalny wzmocnienie nadawania/odbioru
- Accommodates worldwide transmission standards
  Dostosowuje się do międzynarodowych standardów transmisji
- Operates with a wide range of battery voltages
  Działa z szerokim zakresie napięć baterii zasilających
- Adjustable constant current battery feed
  Regulowany stały prąd zasilania z akumulatorów
- Overvoltage and short circuit protection
  Zabezpieczenie przeciwprzepięciowe i przeciwzwarciowe
- Switch hook and ground button detection
  Wykrywanie przełącznika haczykowego i przycisku uziemienia
- Ring trip filter and relay driver
  Filtr odsłuchowy i sterownik przekaźnika
- Low power consumption
  Niskie zużycie energii
- High power dissipation capability during fault conditions
  Duża zdolność rozpraszania mocy w przypadku awarii

Applications
Zastosowania

Line interface for:
Interfejs linii dla:

- PABXs
  Centrale PABX
- Control Systems
  Systemy sterowania
- Key Telephone Systems
  Klucze systemy telefoniczne
- Central Office Equipment
  Sprzęt centralnego biura

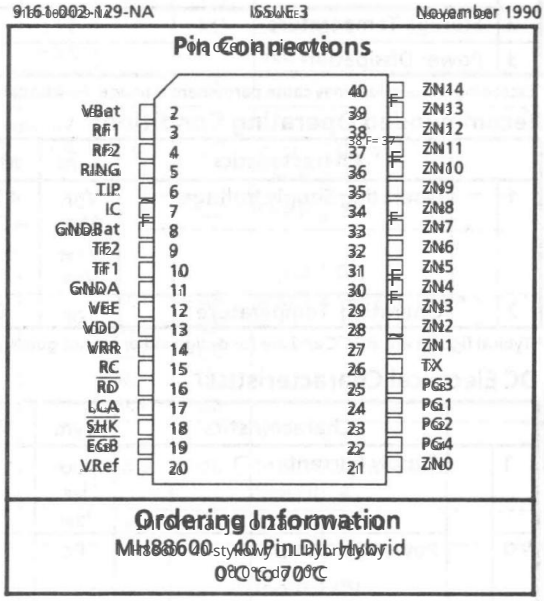
Description
Opis

The MH88600 is a SLIC (Subscriber Line Interface Circuit) which provides all of the BORSHT functions of
MH88600 to jest SLIC (Subscriber Line Interface Circuit), który zapewnia wszystkie funkcje BORSHT

Battery Feed, Overvoltage Protection, Ringing Feed, Line Supervision and 2-4 Wire Hybrid conversion. In addition, the device matches the many different line impedances specified by regulatory authorities around the
Zasilanie akumulatorowe, zabezpieczenie przepięciowe, dzwonienie, nadzór linii i hybrydowe 2-4 przewody. Ponadto urządzenie dopasowuje się do wielu różnych impedancji linii określonych przez organy regulacyjne na całym świecie

world.

Pin Connections
Połączenia pinów



Ordering Information
Informacje do zamówienia

MH88600 40 Pin DIL Hybrid
MH88600 40-stykowy DIL hybrydowy
0°C to 70°C

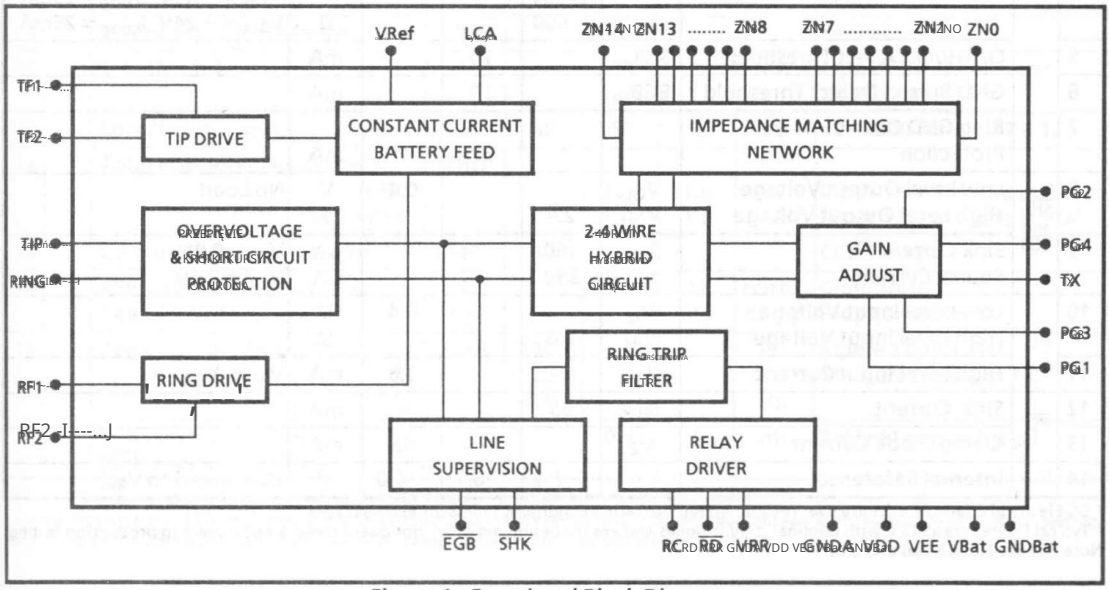


Figure 1 - Functional Block Diagram
Rysunek 1 - Schemat funkcjonalny bloków

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Absolute Maximum Ratings*

Absolute Maximum Ratings* – Napięcia na podanych są względem GNDA.

Voltages are with respect to GNDA.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages (GNDA = GNDBat)	V_{DD}		15	V
		V_{EE}	-15		V
		V_{Bat}	-80		V
		V_{RR}		40	V
2	Storage Temperature	T_S	-55	125	°C
3	Power Dissipation	P_D		4	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Zalecane warunki pracy – Napięcia zasilania są podane względem GNDA.

Voltages are with respect to GNDA.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Operating Supply Voltage	V_{DD}	4.75	5	5.25	V	
		V_{EE}	-5.25	-5	-4.75	V	
		V_{Bat}	-72	-48	-24	V	
		V_{RR}		5	24	V	
2	Operating Temperature	T_{OP}	0		70	°C	

† Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

DC Electrical Characteristics†

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1		Supply Current	I_{DD}		5.0	10.0	mA	
			I_{EE}		3.0	7.0	mA	
			I_{Bat}			4.5	mA	R_{LOOP} = Open Cct, V_{Bat} = -48V
2		Power Consumption	P_C			305	mW	Standby
						755	mW	$R_{LOOP} = 1200\ \Omega$
						1556	mW	$R_{LOOP} = 0\ \Omega$, V_{Bat} = -48V
3		Constant Current Battery Feed ①	I_{LOOP}	18	20	22	mA	LCA = -5.4V
			I_{LOOP}	21	25	30	mA	LCA shorted to V_{Ref}
4		Maximum Operating Loop Resistance ①	R_{LOOP}	2000			Ω	V_{Bat} = -48V, I_{LOOP} = 20mA
				800			Ω	V_{Bat} = -24V, I_{LOOP} = 20mA
				1560			Ω	V_{Bat} = -48V, I_{LOOP} = 25mA
				600			Ω	V_{Bat} = -24V, I_{LOOP} = 25mA
5		Off-Hook Detect Threshold	SHK_{th}		10		mA	
6		GND Button Detect Threshold	EGB_{th}		10		mA	
7		Ring GND Over-Current Protection			32	41	mA	
8	SHK and EGB	Low Level Output Voltage	V_{OL}			0.4	V	No Load
		High Level Output Voltage	V_{OH}	2.4			V	
9		Sink Current	I_{OL}	160			µA	V_{OL} = 0.8V
		Source Current	I_{OH}	390			µA	V_{OH} = 2.0V
10	RD	Low Level Input Voltage	V_{IL}			0.4	V	
		High Level Input Voltage	V_{IH}	2.4			V	
11		High Level Input Current	I_{IH}			1.5	mA	$V_{IH} = V_{DD}$
12	RD	Sink Current	I_{RLY}	65			mA	
13		Clamp Diode Current	I_{CD}			65	milliamperes	
14		Internal Reference	V_{Ref}	-7.4	-6.7	-6.0	V	LCA shorted to V_{Ref}

Parametry elektryczne są podane dla zalecanych warunków pracy, chyba że podano inaczej.

† Typical figures are at 25°C with nominal ±5V supplies and are for design aid only, not guaranteed & not subject to production testing.

Note ① See Figures 2(a) and 2(b).

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AC Electrical Characteristics

AC Electrical Characteristics - Voltages are with respect to GND unless otherwise stated.
Charakterystyka elektryczna prądu zmiennego - Napięcia podane względem uziemienia (GND), chyba że podano inaczej.

	Characteristics / Charakterystyka	Sym	Min	Typ	Max	Units / Jednostki	Test Conditions / Warunki testowe
1	Ringing Voltage / Napięcie dzwonka	V_R			105	V_{rms}	See Fig. 5 / Zobacz rys. 5
2	Ringer Equivalence No. / Numer ekwiwalentu dzwonka	REN			5		
3	Ring Trip Detect Time / Czas wykrywania wyzwalania				200	ms / milisekundy	
4	Input Impedance at PG4 / Impedancja wejściowa przy PG4	Z_{RX}		112		kΩ	See Fig. 4 / Zobacz rys. 4
	at VRX / przy VRX			RRX			See Fig. 3 / Zobacz rys. 3
5	Output Impedance at TX / Impedancja wyjściowa przy TX	Z_{TX}		3		Ω	
6	Gain 2-wire to TX: / Wzmocnienie 2-żyłowe do TX:						
	Fixed Gain / Stałe wzmocnienie	A_{TX}	+3.5	+4	+4.5	dB	Input 1.0V at 1 kHz / Wejście 1,0 V przy 1 kHz See Fig. 4 / Zobacz rys. 4
	Programmable Range / Zakres programowalny	R_{TX}	-12		+6	dB	See Fig. 3 / Zobacz rys. 3
	Frequency Response Gain relative to Gain @ 1 kHz / Wzmocnienie odpowiedzi częstotliwościowej w stosunku do wzmocnienia @ 1 kHz	A_{FTX}					Input 1.0V / Wejście 1,0 V 600Ω 2-Wire Impedance / 600Ω impedancja 2-przewodowa
	300 Hz		-0.75		0.1	dB	
	600 Hz		-0.1		0.1	dB	
	2400 Hz		-0.1		0.1	dB	
	3000 Hz		-0.3		0.1	dB	
	3400 Hz		-0.75		0.1	dB	
7	Gain RX to 2-wire: / Wzmocnienie RX do 2-żyłowego:						
	Fixed Gain / Stałe wzmocnienie	A_{RX}	-4.5	-4	-3.5	dB	Input 1.0V at 1 kHz / Wejście 1,0 V przy 1 kHz See Fig. 4 / Zobacz rys. 4
	Programmable Range / Zakres programowalny	R_{RX}	-12		+6	dB	See Fig. 3 / Zobacz rys. 3
	Frequency Response Gain relative to Gain @ 1 kHz / Wzmocnienie odpowiedzi częstotliwościowej w stosunku do wzmocnienia @ 1 kHz	A_{FRX}					Input 1.0V / Wejście 1,0 V 600Ω 2-Wire Impedance / 600Ω impedancja 2-przewodowa
	300 Hz		-0.75		0.1	dB	
	600 Hz		-0.1		0.1	dB	
	2400 Hz		-0.1		0.1	dB	
	3000 Hz		-0.3		0.1	dB	
	3400 Hz		-0.75		0.1	dB	
8	2-Wire Return Loss / Zwrotna strata 2-żyłowa	RL	30	36		dB	Input 1.0V at 200 Hz to 4 kHz / Wejście dB 1,0 V przy 200 Hz do 4 kHz
9	2-Wire Input Impedance / Impedancja wejściowa 2-żyłowa	Z_{in}					See Table 1 / Zobacz tabelę 1
10	Transhybrid Loss / Utrata transhybrydowa	THL	20	40		dB	Input 1.0V at 300 Hz to 3400 Hz at PG4 / Wejście dB 1,0 V przy 300 Hz do 3400 Hz przy PG4
11	Longitudinal Balance / Równowaga wzdłużna		48	60		dB	50 - 60 / 4000 Hz CCITT 0.121
12	Total Harmonic Distortion / Całkowite zniekształcenie harmoniczne	THD					
	at TX / przy TX			0.1	1.0	%	Input 1.0V at 1 kHz at 2-wire / 1,0% Wejście 1,0 V przy 1 kHz przy 2-przewodowym
	at 2-wire / przy 2-przewodowym			0.1	1.0	%	Input 1.0V at 1 kHz at PG4 / 1,0% Wejście 1,0 V przy 1 kHz na PG4
13	Common Mode Reject Ratio / Współczynnik odrzutu współnego trybu CMRR	CMRR	40				CCITT 0.121
14	Idle Channel Noise at Tx and 2-Wire / Szum kanału bezczynności przy Tx i 2-żyłowym	Nc Np		5	12 -75	dBrnC / dBrnp	C message / Psophometric
15	Power Supply Reject Ratio, V_{DD} / Współczynnik odrzucenia zasilania V_{DD}	PSRR	30			dB	Ripple 1Vpp 1 kHz / tętnienie 1Vpp 1 kHz
	V_{EE}		20			dB	Measure 2-wire or TX / pomiar dwuprzewodowy lub TX
	V_{EE} wł.:		30			dB	
16	Dial Pulse Distortion (SHK High to Low Time) / Zniekształcenie impulsu wybierania (SHK High do Low Time)	$\tilde{t}_d$		0.4	1	ms	2-Wire Loop at 1.2 kΩ / 2-żyłowa pętla przy 1,2 kΩ

AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
Charakterystyka elektryczna prądu zmiennego jest zgodna z zalecanymi warunkami pracy, chyba że podano inaczej.
Typical figures are at 25°C with nominal ±5V supplies and are for design aid only: not guaranteed & not subject to production testing.
Typowe wartości są przy 25°C z nominalnymi zasilaczami ±5V i służą tylko do celów projektowych: nie są gwarantowane i nie podlegają testom produkcyjnym.
Note 1: All of the above test conditions use all Z_{in} values as per Table 1 unless otherwise stated.
Uwaga 1: Wszystkie powyższe warunki testowe wykorzystują wszystkie wartości Z_{in} zgodnie z tabelą 1, chyba że podano inaczej.

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Pin Description

Pin #	Name	Description
1		No pin at this location.
2	V_{Bat}	Battery Supply Voltage (Negative).
3	RF1	Ring Feed (1). Connect to relay contact. See Figures 5 & 6.
4	RF2	Ring Feed (2). Connect to relay contact. See Figures 5 & 6.
5	RING	Connects to the "Ring" or "B" lead of the telephone line.
6	TIP	Connects to the "Tip" or "A" lead of the telephone line.
7	IC	Internal Connection.
8	GND$_{Bat}$	Battery Supply Ground (Positive). Connect to System Ground.
9	TF2	Tip Feed (2). Connect to TF1 for unbalanced ringing, see Figure 5. Connect to relay contact for balanced ringing, see Figure 6.
10	TF1	Tip Feed (1). Connect to TF2 for unbalanced ringing, see Figure 5. Connect to relay contact for balanced ringing, see Figure 6.
11	GNDA	Analog Ground. Normally connected to System Ground.
12	V_{EE}	Negative Power Supply Voltage. Normally -5V.
13	V_{DD}	Positive Power Supply Voltage. Normally +5V.
14	V_{RR}	Ringing Relay Clamp Diode. Connect to relay coil and to relay supply voltage (Positive). For +5V relay, connect to V_{DD}.
15	RC	Ring Control (Input). A logic high will activate the Ring Relay Drive if $\overline{SHK}$ is high.
16	$\overline{RD}$	Ring Relay Drive (Output). Connect to relay coil. A logic low will activate the relay by sinking current from V_{RR} through the relay coil.
17	LCA	Loop Current Adjust (Input). Loop current is proportional to the voltage at this input. Normally connected to V_{Ref}.
18	$\overline{SHK}$	Switch Hook Detect (Output). A logic low indicates an off-hook condition.
19	$\overline{EGB}$	Earth Ground Button (Output). A logic low indicates a grounded Ring lead condition.
20	V_{Ref}	Voltage Reference (Output). Normally connected to LCA for default loop current.
21	ZN0	Impedance Node 0. Connect to external network for impedance (Z_{in}) setting. See Table 2 and Figure 7.
22	PG4	Programming 4 (Input). Used for programmable gain and for default gain. Used as 4-Wire Receive Input for default gain. See Table 3 and Figures 3 and 4.
23	PG2	Programming 2 (Input). Used for programmable gain. Used with resistor for 4-Wire Receive Input. See Table 3 and Figure 3.
24	PG1	Programming 1 (Input). Used for programmable gain. See Table 3 and Figure 3.
25	PG3	Programming 3 (Input). Used for programmable gain and for default gain. See Table 3 and Figures 3 and 4.
26	TX	4-Wire Transmit Output.
27	ZN1	Impedance Node 1. Connect to other Impedance Nodes for impedance (Z_{in}) setting, see Table 1. Or, connect to external network for impedance (Z_{in}) setting, see Table 2 and Figure 7.
28	ZN2	Impedance Node 2. Connect to other Impedance Nodes for impedance (Zin) setting. See Table 1.
29	ZN3	Impedance Node 3. As per ZN2. See Table 1.
30	ZN4	Impedance Node 4. As per ZN2. See Table 1.
31	ZN5	Impedance Node 5. As per ZN2. See Table 1.
32	ZN6	Impedance Node 6. As per ZN2. See Table 1.
33	ZN7	Impedance Node 7. As per ZN2. See Table 1.

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Pin Description (continued)

Pin #	Name	Description
34	ZN8	**Impedance Node 8.** As per ZN2. See Table 1.
35	ZN9	**Impedance Node 9.** As per ZN2. See Table 1.
36	ZN10	**Impedance Node 10.** As per ZN2. See Table 1.
37	ZN11	**Impedance Node 11.** As per ZN2. See Table 1.
38	ZN12	**Impedance Node 12.** As per ZN2. See Table 1.
39	ZN13	**Impedance Node 13.** As per ZN2. See Table 1.
40	ZN14	**Impedance Node 14.** Connect to external network for impedance (Z_{in}) setting. See Table 2 and Figure 7

	Z_in Code	Z_in 2-Wire Input Impedance	Administration	ZN1 Link To:	ZN8 Link To:
1	600	600Ω	---	ZN7	---
2	UK	370Ω + 620Ω // 310nF	United Kingdom	ZN6	ZN13
3	D	220Ω + 820Ω // 115nF	Germany, Austria	ZN5	ZN12
4	NA	350Ω + 1000Ω // 210nF	Canada, USA	ZN4	ZN11
5	F	210Ω + 880Ω // 150nF	France	ZN3	ZN10
6	N	120Ω + 820Ω // 110nF	Norway	ZN2	ZN9
7	A	220Ω + 820Ω // 120nF	Australia	Use D Code	Use D Code

Table 1. Impedance Matching with Jumpers

Note 1. The above impedances are as suggested by the following references: BS6305 (UK), REG 3 (Australia), proposed NET4, FCC Part 68, and recommendations by the various Administrations. Confirm your impedance requirements before proceeding.

Note 2. All links to ZN1 and ZN8 should be as short as possible.

	Z_in Code	Z_in 2-Wire Input Impedance	Administration	Rs	Rp	C
1	---	600Ω + 2.16μF	---	6kΩ	1MΩ	216nF
2	ATT	900Ω + 2.16μF	AT&T	9kΩ	1MΩ	216nF
3	NTT	600Ω + 1.0μF	NTT	6kΩ	1MΩ	100nF
4	NZ	370Ω + 620Ω // 220nF	New Zealand	3.7kΩ	6.2kΩ	22nF

Table 2. Impedance Matching with External Components

Note 1. The above impedances are as suggested by reference CCITT Q.552. Confirm your impedance requirements before proceeding.

Note 2. For Rs, Rp & G calculations, G is set to 10, R is set to 5656.8Ω, refer to Figure 7 for additional information.

Transmit Gain (dB)	TRX Resistor Value (Ω)	Notes
+5.62	270k	
+4.0	No Resistor	Results in 0dB overall gain when used with Mitel A-law codec (i.e., MT8965).
+3.69	216k	Results in 0dB overall gain when used with Mitel μ-law codec (i.e., MT8964).
+2.1	180k	
0.0	141k	
-3.0	100k	

Receive Gain (dB)	RRX Resistor Value (Ω)	Notes
+6.6	33.1k	
+6.0	70.7k	
+3.0	100k	
+3.69	108k	Results in 0dB overall gain when used with Mitel μ-law codec (i.e., MT8964).
+4.0	No Resistor	Results in 0dB overall gain when used with Mitel A-law codec (i.e., MT8965).
+6.5	150k	

Table 3. Transmit and Receive Gain Programming

Note 1. See Figures 3 and 4 for additional details.

Note 2. Overall gain refers to the receive path of PCM to 2-Wire, and transmit path of 2-Wire to PCM.

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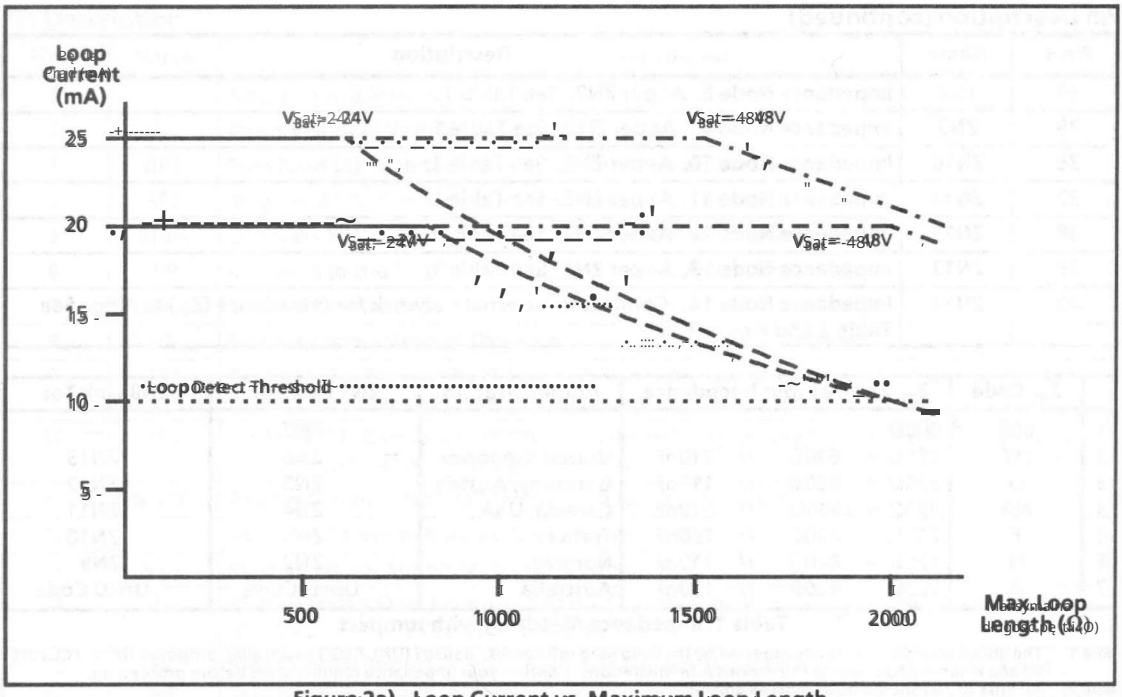

Figure 2a) Loop Current vs. Maximum Loop Length

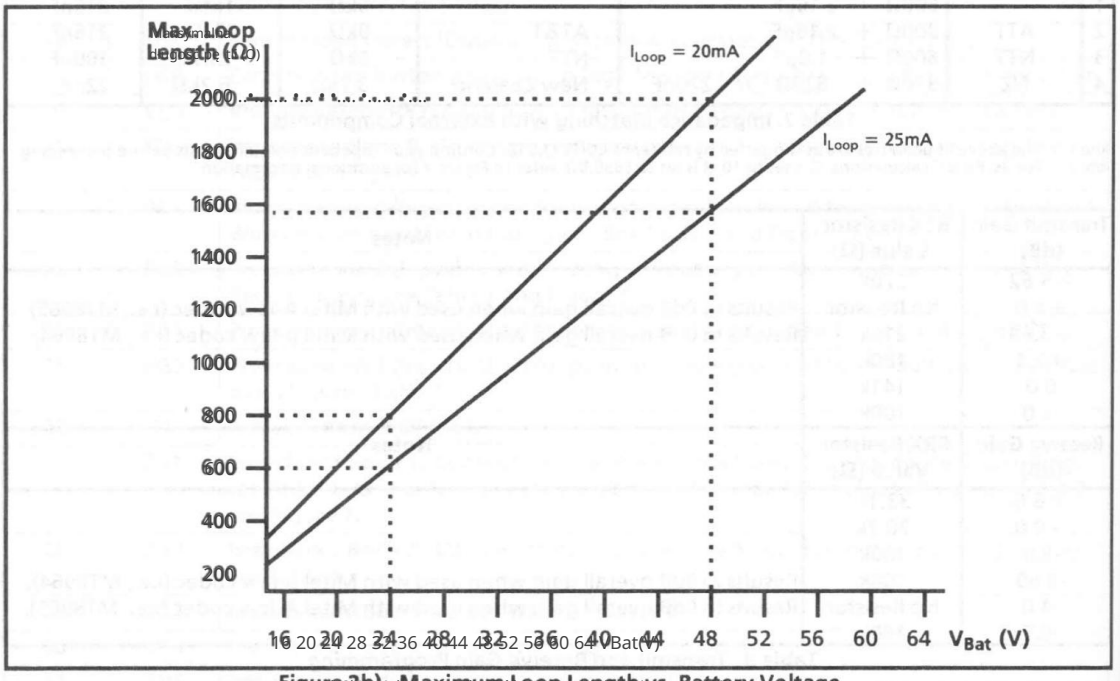

Figure 2b) Maximum Loop Length vs. Battery Voltage

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Functional Description

The BORSHT Functions

The MH88600 performs all of the BORSHT functions; Battery Feed, Overvoltage Protection, Ringing, Supervision, and Hybrid.

Battery Feed

The MH88600 provides the loop with constant DC current to power the telephone set. The voltage (negative) applied at the LCA pin determines the magnitude of the loop current.

$$I_{Loop} = 3.731 \times V_{LCA}\ mA\ (\pm 2mA)$$

Either the internal (V_{REF}) or an external negative voltage reference may be used to set the loop current.

Overvoltage Protection

The MH88600 is protected from short term (20ms) transients (<250V) between Tip and Ring, Tip and ground and Ring and ground. However, additional protection circuitry may be needed depending on the regulatory requirements which must be met. Normally simple external shunt protection as shown in Figures 5, 6 and 7, is all that is required.

Ringing

The MH88600 has the capability to accommodate both balanced and unbalanced ringing sources. Refer to Figure 6 for the Balanced Ringing Circuit and Figure 5 for the Unbalanced Ringing Circuit.

Supervision

The MH88600 is capable of detecting both Ground Button and Switch Hook conditions. The GFDO Ground Button detection (a logic low at the $\overline{GFDO}$ output) operates when an imbalance in Tip and Ring DC current exceeds an internal threshold level caused by a grounded Ring lead. Use of the $\overline{GFDO}$ output is restricted to the off-hook condition of the telephone. The Switch Hook detection operates (a logic low at the $\overline{SHK}$ output) when the DC loop current exceeds an internal threshold level.

The Ring Trip Detection Circuit prevents false off-hook detections due to the current associated with the AC ringing voltage and also due to large current transients when the ring voltage is switched in and out. In addition, the circuit prevents connection of the ringing source during off-hook conditions.

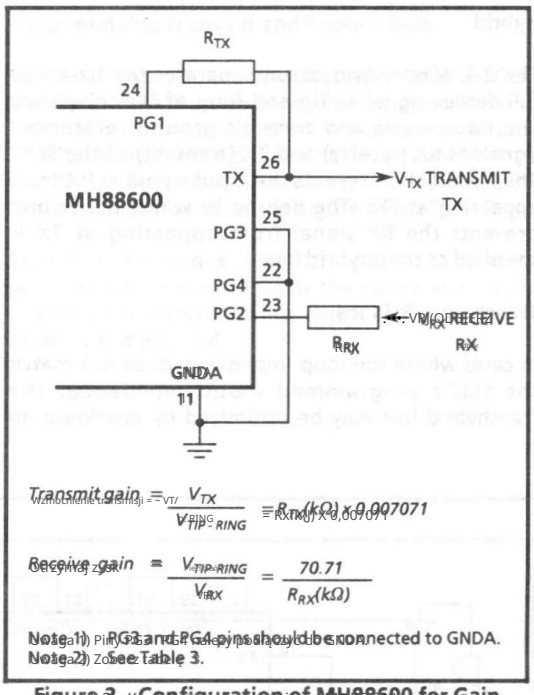

Figure 3 - Configuration of MH88600 for Gain Programming

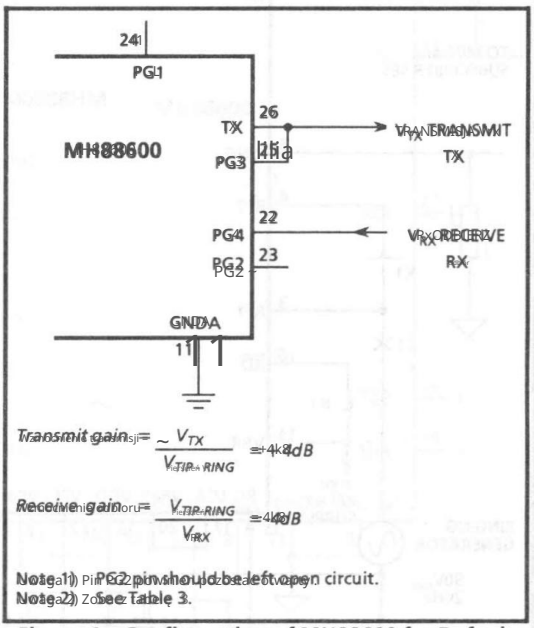

Figure 4 - Configuration of MH88600 for Default Gains

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Hybrid

The 2-4 Wire Hybrid circuit separates the balanced full duplex signal at Tip and Ring of the telephone line into receive and transmit ground referenced signals at RX (receive) and TX (transmit) of the SLIC. The Hybrid also prevents the input signal at RX from appearing at TX. The degree to which the Hybrid prevents the RX signal from appearing at TX is specified as transhybrid loss.

Transhybrid Balance

In cases where the loop impedance does not match the SLIC's programmed input impedance, the transhybrid loss may be optimized by providing an external circuit. Refer to the application circuit in Figure 8 for details.

Tip-Ring Drive Circuit

The audio input ground referenced signal at RX is converted to a balanced output signal at Tip and Ring. The output signal consists of the audio signal superimposed on the DC Battery Feed Constant Current. The Tip-Ring Drive Circuit is optimized for good 2-Wire longitudinal balance.

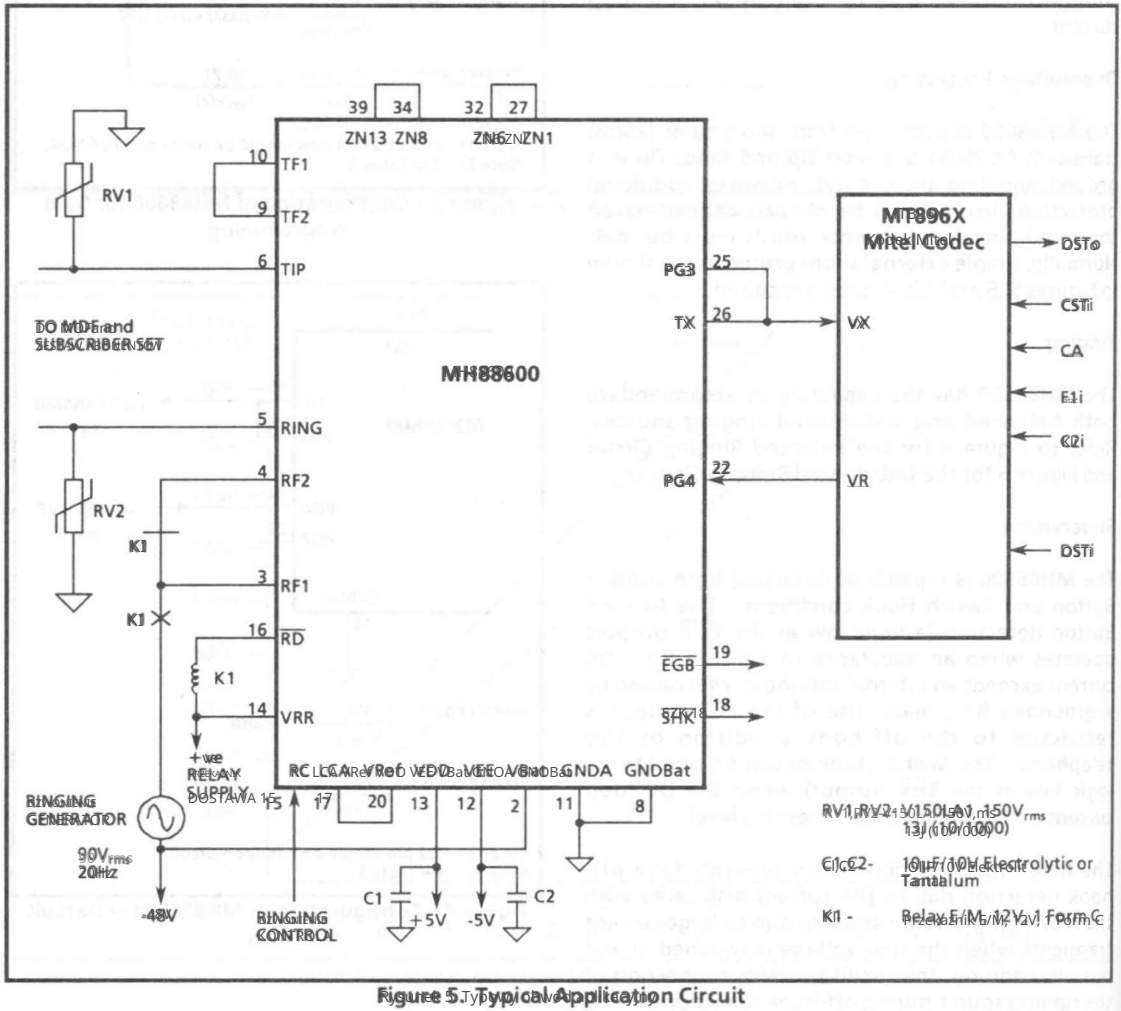

Figure 5. Typical Application Circuit

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Short Circuit Protection
Zabezpieczenie przed zwarciem

The MH88600 is protected from long term (infinite) short circuit conditions occurring between Tip and Ring, Tip and Ground, Ring and Ground, and Ring and Battery. The current is limited to the same value as the Constant Current Battery Feed.

MH88600 jest zabezpieczony przed długotrwałymi (nieskończonymi) warunkami krótkiego napięcia wystąpienia między końcówką a pierścieniem, końcówką a uziemieniem, pierścieniem a uziemieniem oraz pierścieniem a akumulatorem. Prąd jest ograniczony do tej samej wartości, co prąd stały akumulatora.

Programmable Line Impedance
Programowalna impedancja linii

The MH88600's Tip-Ring (Z_{TR}) impedance can be matched to the different impedances specified by different telephone administrations worldwide. This is accomplished by either linking specific pins as specified in Table 1, or by adding external components as shown in Figure 7 and Table 2.

Impedancję Tip-Ring (Z_{TR}) modelu MH88600 można dopasować do różnych impedancji stosowanych przez różne administracje telefoniczne na całym świecie. Można to osiągnąć, łącząc określone piny zgodnie ze specyfikacją z Tabeli 1 lub dodając komponenty zewnętrzne, jak pokazano na Rysunku 7 i Tabeli 2.

Programmable Transmit and Receive Gain
Programowany zysk nadawania i odbioru

Transmit Gain (TX to Tip-Ring) and Receive Gain (Tip-Ring to RX) can be programmed by connecting external resistors as indicated in Figure 3 and Table 3. Alternatively, the default Receive Gain of -4 dB and Transmit Gain of +4 dB can be obtained by connecting pins as shown in Figure 4 and Table 3.

Wzmocnienie nadawania (TX do Tip-Ring) i wzmocnienie odbioru (Tip-Ring do RX) można zaprogramować, podłączając zewnętrzne rezystory, jak pokazano na rysunku 3 i w tabeli 3. Alternatywnie, domyślne wzmocnienie odbioru wynoszące -4dB i wzmocnienie nadawania wynoszące +4 dB można uzyskać, podłączając piny, jak pokazano na rysunku 4 i w tabeli 3.

Note that RX is not a pin on the SLIC. The RX terminal will be either PG4 or the connection to the receive gain programming resistor R_{RX} shown in Figure 3 and Figure 4.

Należy pamiętać, że RX nie jest pinem na SLIC. Zacisk RX będzie albo PG4 lub połączeniem z rezystorem programującym wzmocnienie odbioru R_{RX} pokazanym na rysunku 3 i rysunku 4.

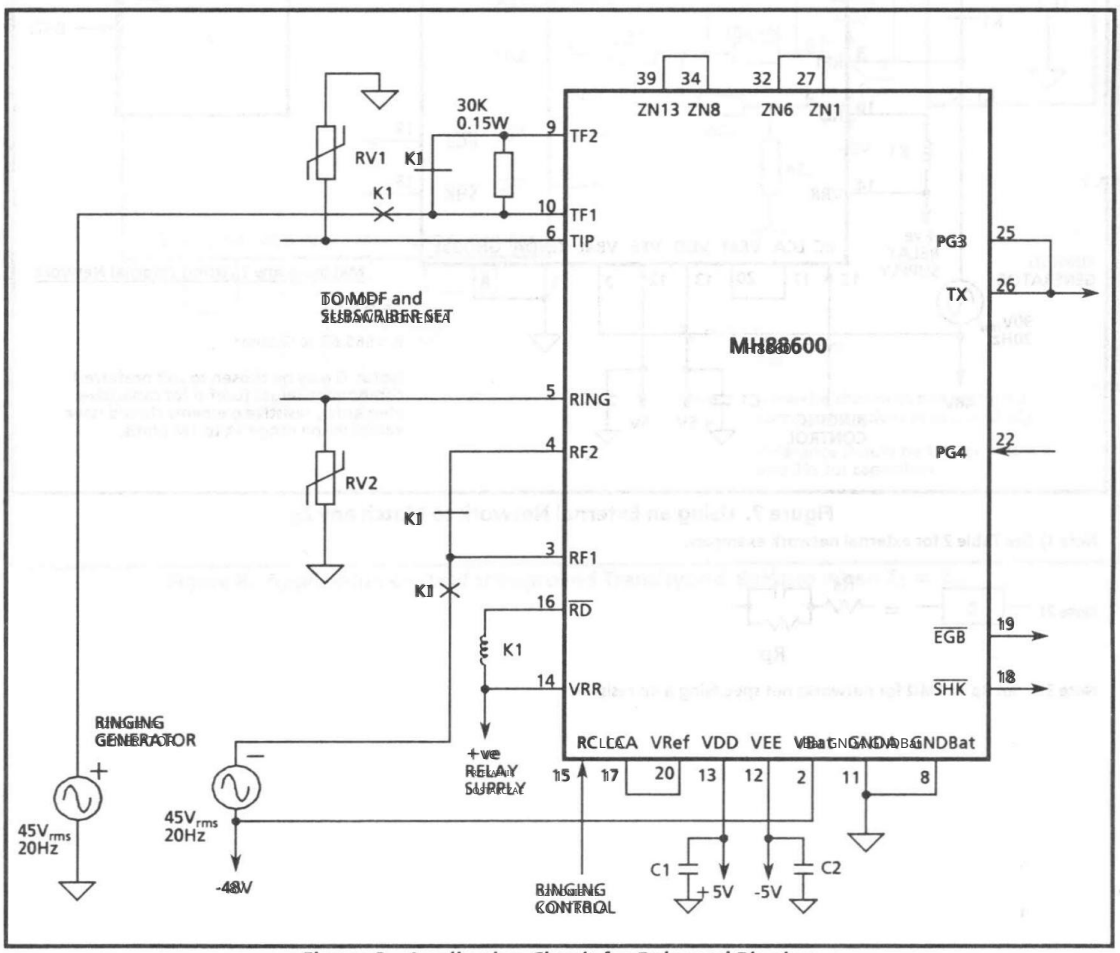

Figure 6. Application Circuit for Balanced Ringing
Rysunek 6. Układ aplikacyjny dla dzwonienia zrównoważonego

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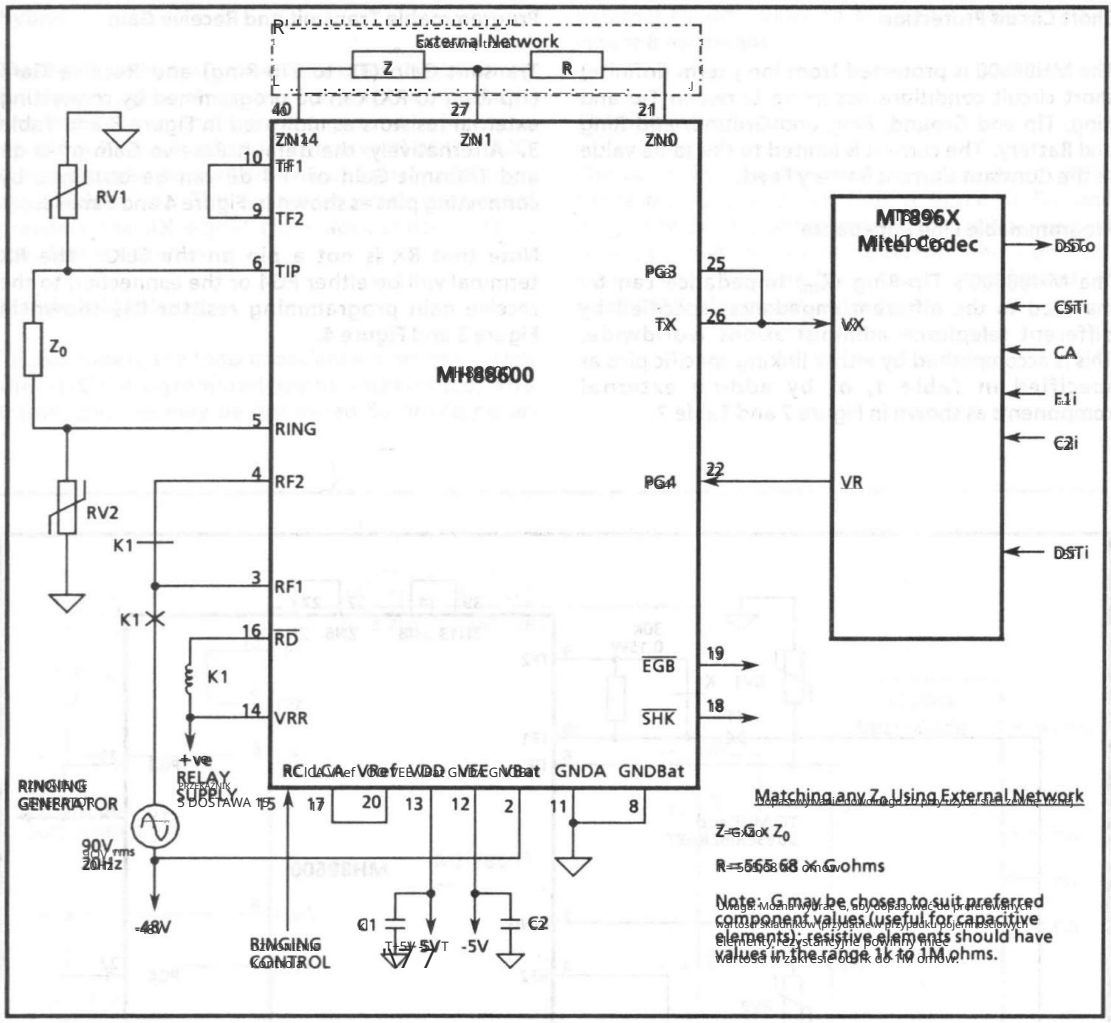
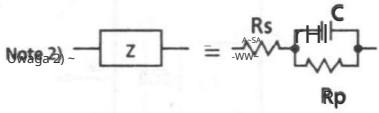


Figure 7. Using an External Network to Match any Z_0

Note 1) See Table 2 for external network examples.

Note 2)



Note 3) Set Rp = 1MΩ for networks not specifying a Rp resistor.

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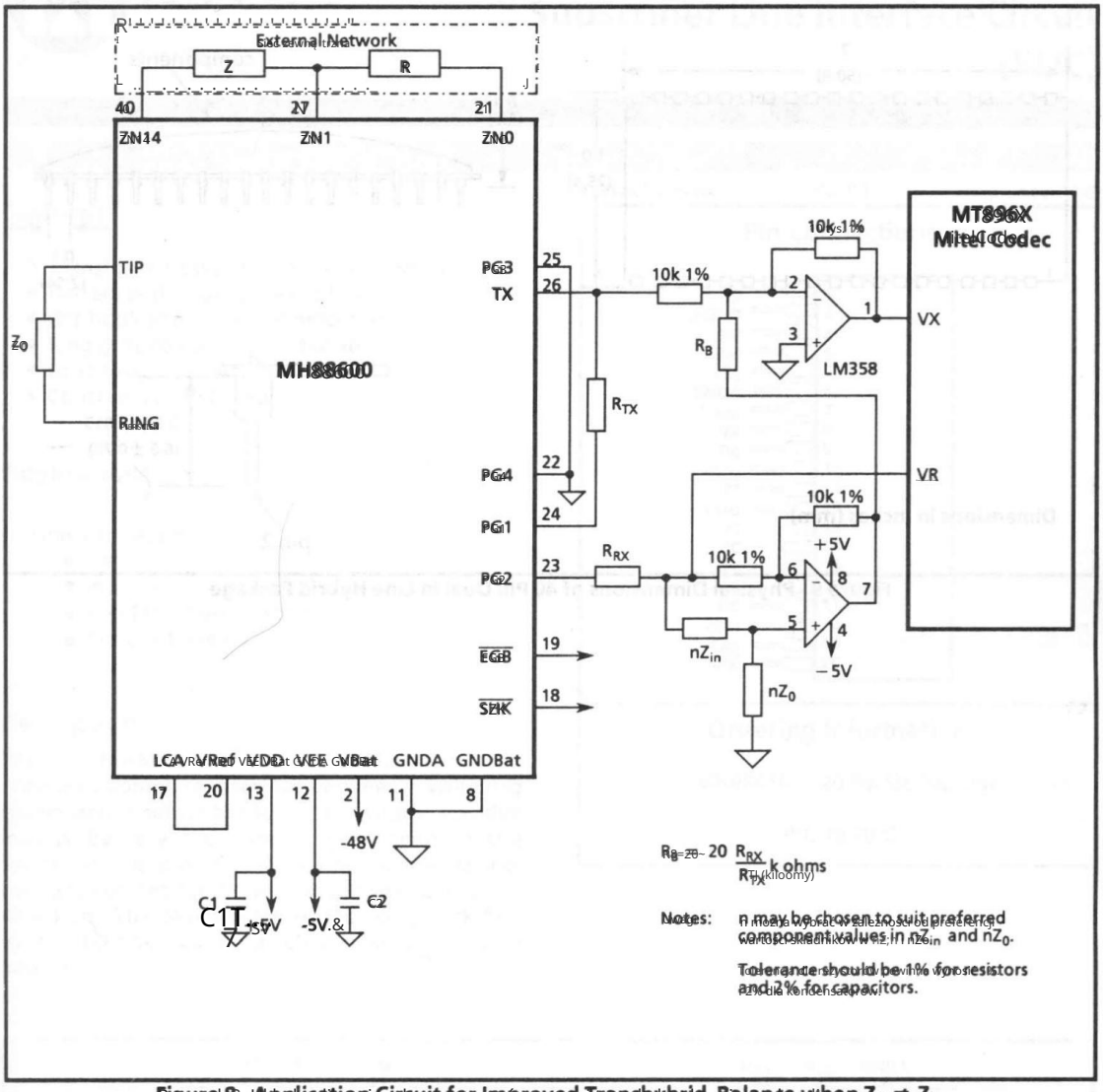

Figure 8. Application Circuit for Improved Transhybrid Balance when $Z_0 \neq Z_{in}$

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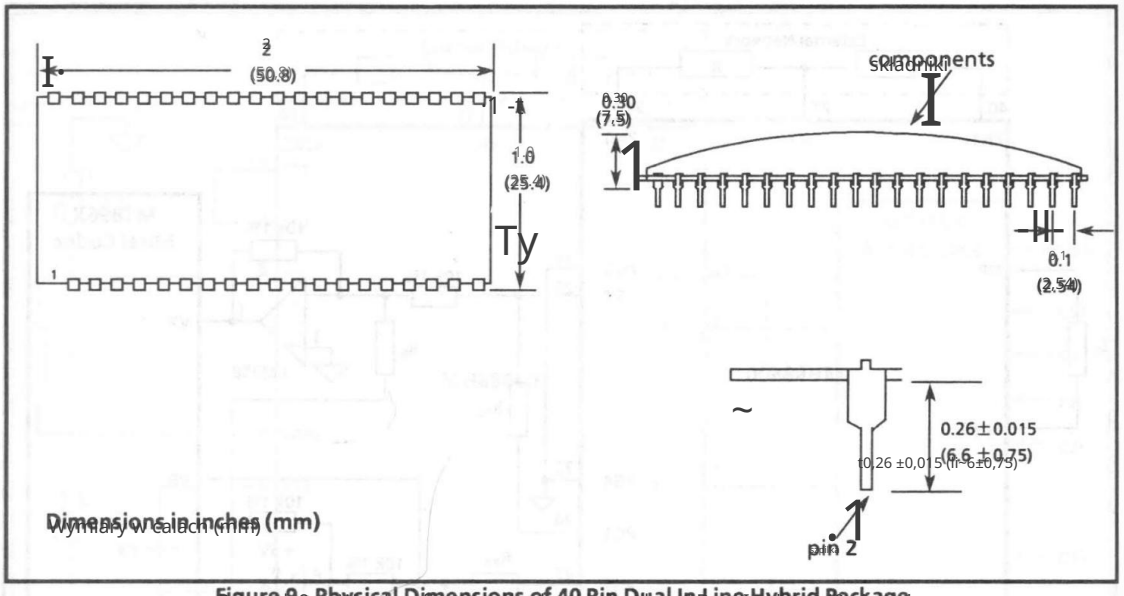

Figure 9 Physical Dimensions of 40 Pin Dual In Line Hybrid Package

Rysunek 9 — Wymiary fizyczne obudowy hybrydowej dual in line z 40 pinami

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MH88610

Subscriber Line Interface Circuit (SLIC)

9161-002-095-NA ISSUE 3 September 1989

Features

- Transformerless 2 wire to 4 wire conversion
- Battery and ringing feed to line
- Off-hook and dial pulse detection
- Ring ground over-current protection
- Loop length detection
- Constant current feed

Applications

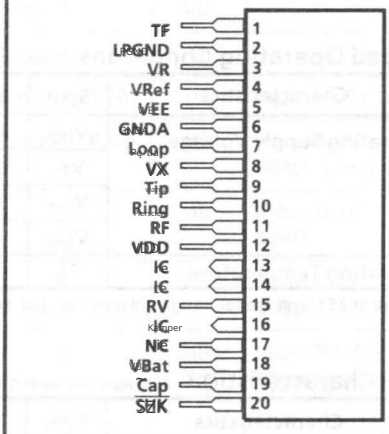
Line Interface for:

- PABX
- Intercoms
- Key Telephone Systems
- Control Systems

Description

The Mitel MH88610 Subscriber Line Interface Circuit provides a complete interface between a switching system and a subscriber loop. Functions provided include battery feed and ringing feed to the subscriber line, 2-wire to 4-wire hybrid interfacing, constant current feed, loop length and dial pulse detection. The device is fabricated using thick film hybrid technology in a 20 pin single-in-line package.

Pin Connections



Ordering Information

MH88610 20 Pin SIL Package

0°C to 70°C

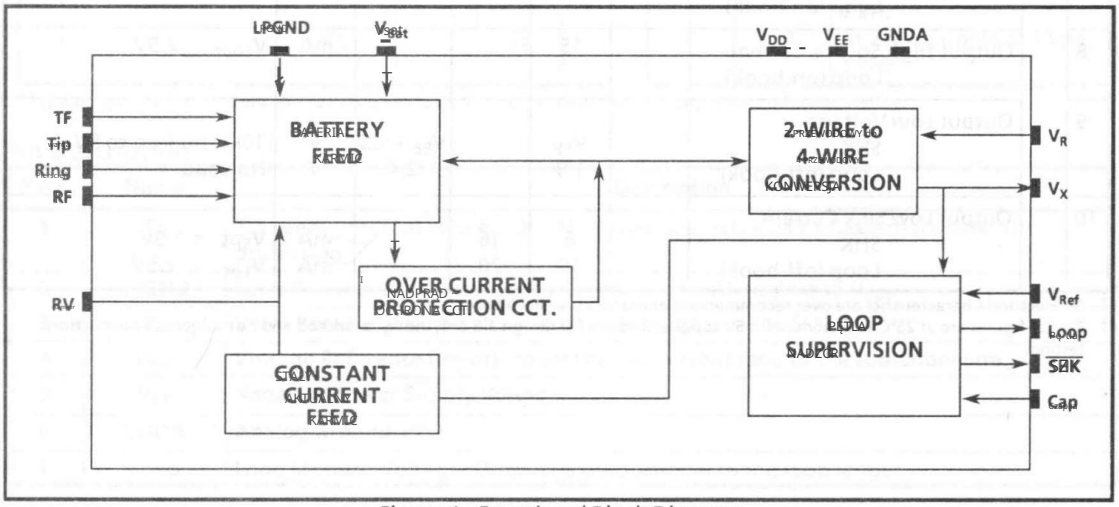


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Voltages are with respect to GNDA unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD}		+15	V
		V_{EE}	-15		V
	V_{SS} - GNDA	V_{Bat}	-80		V
2	Storage Temperature	T_{STG}	-40	100	°C
3	Package Power Dissipation	P_D		2	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Voltages are with respect to GNDA unless otherwise stated.

		Characteristics	Sym	Min	Typ†	Max	Units	Comments
1		Operating Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
			V_{EE}	-5.25	-5.0	-4.75	V	
			V_{Ref}		-1.1		V	
			V_{Bat}		-28		V	
2		Operating Temperature	T_O	0		70	°C	

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics‡

Voltages are with respect to GNDA unless otherwise stated.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1		Supply Current V_{DD}	I_{DD}		6.4	7.6	mA	
		V_{EE}	I_{EE}		-3.4	-5.0	mA	
2		Power Consumption	P_C			212	mW	Standby
						1110	mW	Active
3		Constant Current Line Feed	I_{Loop}	24	26	28	mA	
4		Operating Loop Resistance	R_{Loop}	800			Ω	V_{Bat} = -28V
5		Off-Hook Threshold			1200		Ω	V_{Bat} = -28V
6		Ring Ground Over-Current Protection			33	42	mA	
7		Output High Voltage $\overline{SHK}$ Loop (on-hook)	V_{DD}-2		V_{DD}		V	No Load
8		Output High Source Current $\overline{SHK}$ Loop (on-hook)		15			mA	V_{Loop} = 2.5V
9		Output Low Voltage $\overline{SHK}$ Loop (off-hook)	V_{EE}			V_{EE}+1.5	V	10kΩ pull up to 5V
					1.9	2.4	V	No Load
10		Output Low Sink Current $\overline{SHK}$ Loop (off-hook)		6	16		mA	V_{SHK} = 1.5V
				10	20		mA	V_{Loop} = 2.5V

‡ DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

†Typical figures are at 25°C with nominal ±5V supplies and are for design aid only: not guaranteed and not subject to production testing.

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AC Electrical Characteristics

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Ringing Voltage (RMS)	V_R			105	V_{RMS}	
2	Ringer Equivalence Number	REN			3		
3	Ring Trip Detect Time				200	ms	
4	Input AC Impedance 2-wire	Zin		600		Ω	
5	Input Impedance at V_R			230		kΩ	
6	Output Impedance at V_X			1		Ω	
7	Gain 2-wire to V_X		0.60	0.62	0.70	dB	Input 6dBm at 2-wire
8	Gain V_R to 2-wire		-6.75	-6.69	-6.65	dB	Input 1.0 V at V_R, 600Ω termination
9	2-wire Return Loss		20			dB	Input 0.5 V_{RMS} 1 kHz, 600Ω
10	Transhybrid Loss	THL	40			dB	Input 0.5 V_{RMS} 1 kHz at V_R 600Ω
11	Longitudinal Balance		45			dB	Input 0.5 V_{RMS} 1 kHz at metallic output voltage
12	Total Harmonic Distortion	THD					
	at V_X			0.1	1.0	%	Input 6dBm at 2-wire
	at Tip or Ring			0.1	1.0	%	Input 1.0 V at V_R
13	Common Mode Rejection Ratio 2-wire to V_X	CMRR	40			dB	Input 0.5 V_{RMS} 1 kHz at metallic output voltage
14	Idle Channel Noise (at V_X)	N_C			15	dBrnC	C Message
15	Power Supply Rejection Ratio	PSRR					
	V_{DD}		39			dB	At V_X, ripple at 1 V_{pp}, 1 kHz
	V_{DD}		37			dB	At 2-wire, ripple at 1 V_{pp}, 1 kHz
	V_{EE}		23			dB	At V_X, ripple at 1 V_{pp}, 1 kHz
	V_{EE}		23			dB	At 2-wire, ripple at 1 V_{pp}, 1 kHz

†Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Pin Description

Pin #	Name	Description
1	TF	**Tip Feed.** Internal connection. Normally connects a pair of external diodes for protection.
2	LPGND	**Loop Ground** is the system ground reference with respect to V_{Bat}.
3	V_R	**Voice Receive (Input)** is the 4-wire analog signal to the SLIC.
4	V_{Ref}	**Voltage Reference (Input)** to set the line current feed to the subscriber line.
5	V_{EE}	**Negative Power Supply Voltage.**
6	GNDA	**Analog Ground** (0V).
7	Loop	**Loop Monitor Voltage (Output)** is proportional to the loop length.

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Pin Description (continued)

Pin #	Name	Description
8	V_X	**Voice Transmit (Output)** is the 4-wire analog signal from the SLIC.
9	Tip	Connects to the "Tip" lead of the telephone line.
10	Ring	Connects to the "Ring" lead of the telephone line.
11	RF	**Ring Feed (Input)** is normally connected to ring relay for negative line feed voltage and ringing input.
12	V_{DD}	**Positive Power Supply Voltage**.
13	IC	**Internal Connection.** Pin cut short.
14	IC	**Internal Connection.** Pin cut short.
15	RV	**Ring Feed Voltage** connects to pin 11 (RF) through normally closed ring relay.
16	IC	**Internal Connection.** Pin cut short.
17	NC	**No Connection.**
18	V_{Bat}	**Negative Battery Feed Supply Voltage.**
19	Cap	Connects external capacitor and resistor to ground for ringing filter control.
20	$\overline{SHK}$	**Switch Hook Detect (Output)**. Digital output of an open-collector comparator. This output will go low (V_{EE}) when the subscriber line resistance falls below a set threshold value, indicating that the telephone set has gone off-hook. This output can be used to detect dial pulses or tone dialing.

Functional Description

The MH88610 performs a transformerless 2-wire to 4-wire conversion of the analog signal. The 2-wire circuit is the balanced line going to the subscriber loop, while the 4-wire circuit is the audio signal going to and from devices such as the voice codec or switching circuit. The SLIC also provides two status signals: switch hook ($\overline{SHK}$) and loop length (Loop). The Loop signal is an analog voltage which is proportional to the loop length and the $\overline{SHK}$ goes low when the telephone set is off-hook.

Constant Current Feed

The MH88610 employs a complex feedback circuit to supply a constant feed current to the line. This is done by sensing the sum of the voltages across the internal feed resistors and comparing it to an input reference voltage (V_{Ref}) that determines the constant feed current. This gives the loop current as:

$$I_{Loop} = \frac{V_{Ref}}{0.423} \text{ mA } (\pm 2 \text{ mA})$$

Switch Hook Detect

When the DC current exceeds an internal threshold level, the switch hook ($\overline{SHK}$) will go low. If the loop resistance is so high that V_{EE} can no longer supply the required amount of loop current as determined by the constant current supply circuit, the output of the switch hook ($\overline{SHK}$) will go to high impedance (open collector output) to indicate that the loop resistance is too high and the line is on hook.

Ringing and Ring Trip Detection

The MH88610 can withstand an off-hook condition during ringing. In Figure 2 a ringing signal (e.g., 90 V_{RMS} at 20 Hz) is applied to the line by disconnecting Pin 15 (RV) from pin 11 (RF), and connecting the ringing voltage at pin 11 (RF). During ringing, there is a large AC component which must be filtered out to give a true off-hook indication. For normal operation, a capacitor of 1.0 µF connected to pin 19 (Cap) will provide an adequate attenuation for 20 Hz ringing frequency.

Once an off-hook condition has been detected, an external circuitry will activate the relay (K1) to disconnect the ringing voltage from pin 11 (RF) and reconnect it to pin 15 (RV). At this time the SLIC will revert to constant current feed operation.

Current Limit

The Tip or Ring may accidentally short to ground. In such a case, current will only flow through the feed resistor. This high current will be sensed and reduced by the current limit circuit to a lower value to protect the internal circuitry.

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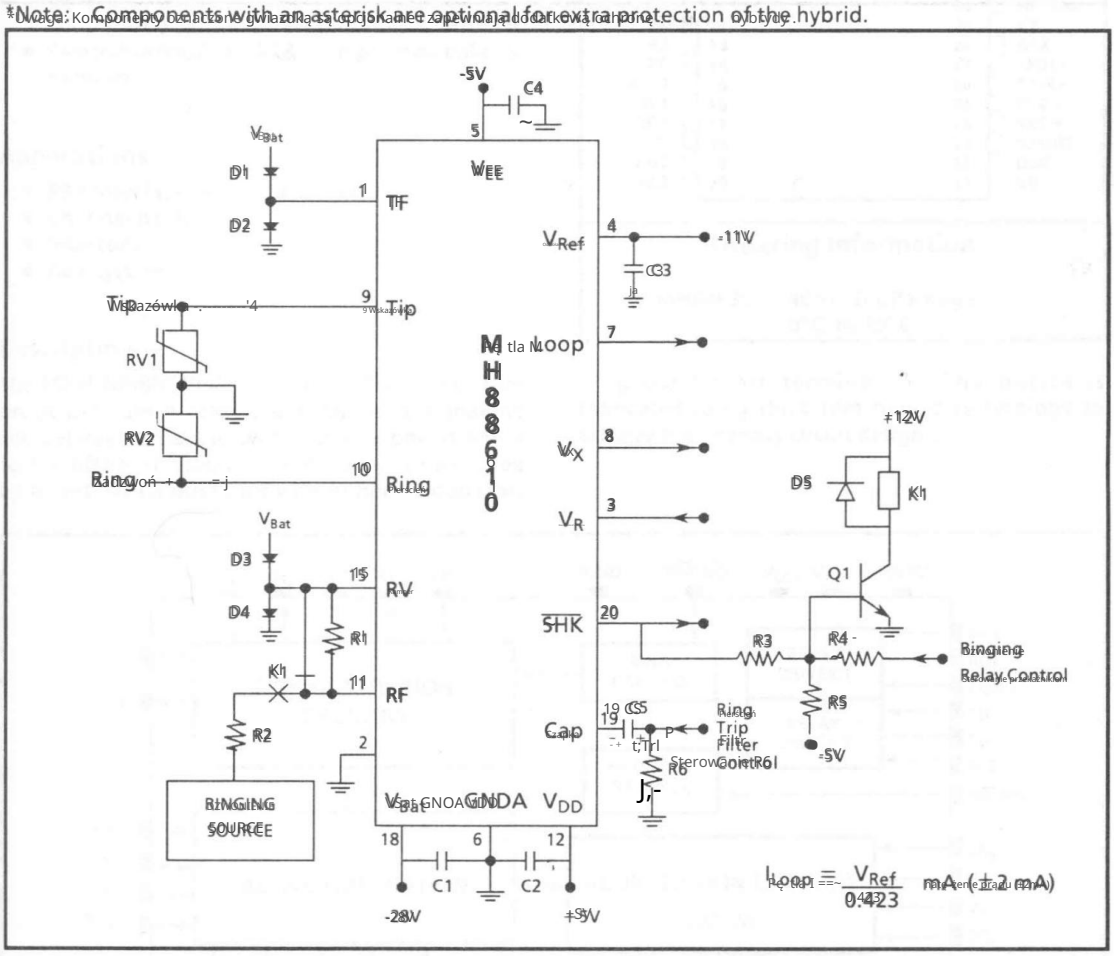
Components List

Lista składników

R1	= Resistor, ¼W, ±5%, 30.0 kΩ	D1*,D3*,D4*	= Diode Rect, 200V, 1A, IN4003
R2*	= Resistor, ¼W, ±5%, 750 Ω	D2	= Diode Rect, 200V, 1A, IN4003
R3	= Resistor, ¼W, ±5%, 3.9 kΩ	D5	= Diode, 75V, 0.2A, 0.5W, IN4148
R4	= Resistor, ¼W, ±5%, 4.7 kΩ	Q_1	= NPN, 2N2222 or equivalent
R5	= Resistor, ¼W, ±5%, 43 kΩ	K_1	= Relay, E/M, 12V, 1 Form C
R6	= Resistor, ¼W, ±5%, 470 kΩ	C1*,C2*,C3*,C4*	= Cap, Ceram, 0.1µF, 50V, 20%
RV1*,RV2*	= Varistor, 160V, 250V, 10J	C5	= Cap, Elec, 1.0µF, 16V, 10%

*Note: Components with an asterisk are optional for extra protection of the hybrid.

Uwaga: Komponenty oznaczone gwiazdką są opcjonalne zapewniają dodatkową ochronę hybrydy.



$$I_{Loop} = \frac{V_{Ref}}{0.423} \text{ mA } (\pm 2 \text{ mA})$$

Figure 2 - Zastosowanie Obwodu

Figure 2 - Application Circuit

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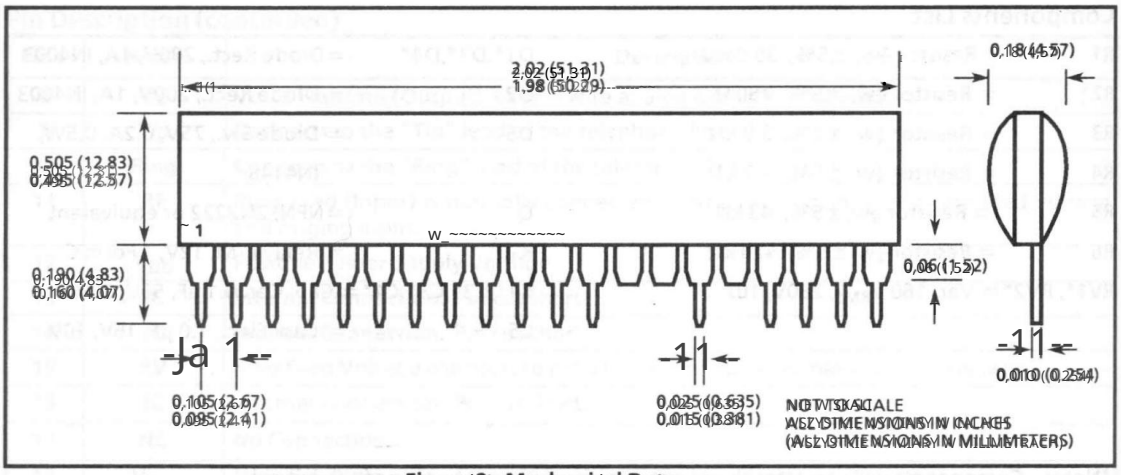

Figure 33 - Mechanical Data

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9116 bd 207-106-NA ISSUE 4 September 1990

Features

- Transformerless 2W to 4W conversion
- Line state detection outputs:
  - forward current
  - reverse current
  - ring ground
  - tip ground
  - ringing voltage
- Programmable audio transmit and receive gain
- Loop start or ground start termination
- Selectable 600Ω or AT&T compromise balance network

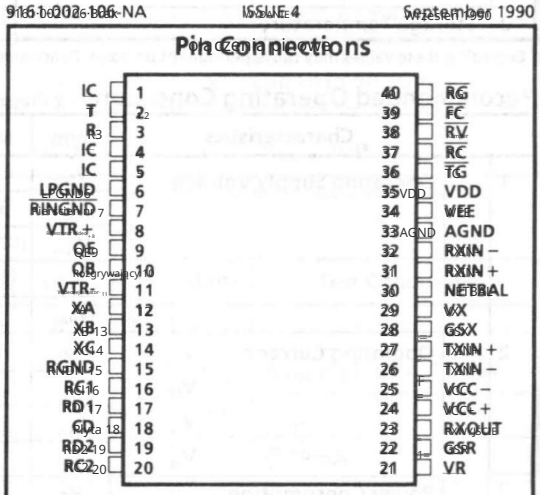
Applications

- PBX interface to Central Office
- Channel bank
- Intercom
- Key system

Description

The Mitel MH88630 Central Office Trunk Interface circuit provides a complete audio and signalling link between an audio switching equipment and a central office. The loop seize circuitry is controlled by an external input to provide either a loop start or ground start termination. The device is fabricated using thick film hybrid technology to achieve high density circuit design.

Pin Connections



Ordering Information

MH88630	40 Pin DIL Package
	0°C to 70° C

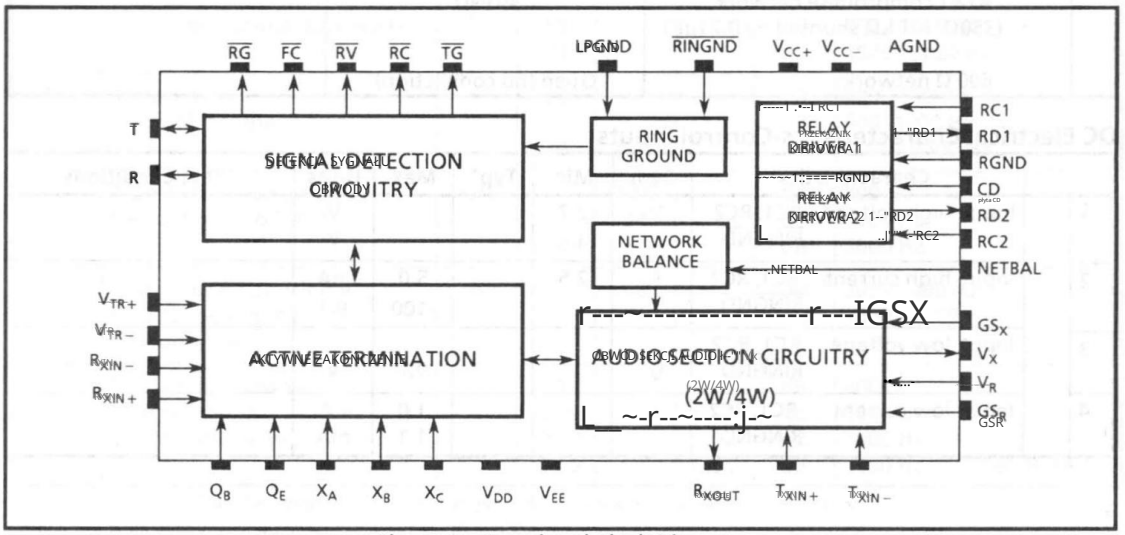


Figure 1 Functional Block Diagram

Machine Translated by Google

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD} - GNDD	-0.3	+6.0	V
		V_{EE} - GNDD	-6.0	+0.3	V
		V_{CC+} - GNDA		+18.0	V
		V_{CC-} - GNDA	-18.0		V
2	Storage Temperature	T_{STG}	-55	+125	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Voltages are with respect to GND unless otherwise stated.

	Characteristics	Sym	Min	Typ*	Max	Units	Comments
1	Operating Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
		V_{EE}	-5.25	-5.0	-4.75	V	
		V_{CC+}	11.4	12.0	12.6	V	
		V_{CC-}	-11.4	-12.0	-12.6	V	
		V_{BAT}		-48.0		V	
2	Operating Current V_{DD}	I_{DD}			6.0	mA	$\overline{RINGND}$ High
	V_{EE}	I_{EE}			-6.0	mA	
	V_{CC+}	I_{CC+}			8.0	mA	
	V_{CC-}	I_{CC-}			-8.0	mA	
3	Power Consumption	P_C			265	mW	
4	Operating Temperature	T_O	0		70	°C	

* Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

Control Inputs State Table

	Parameter	Active	Idle
1	RC1	Logic High	Logic Low
2	RC2	Logic High	Logic Low
3	$\overline{RINGND}$	Logic Low	Logic High
4	NETBAL AT&T compromise network (350Ω + 1kΩ shunted by 0.21µF) 600Ω network	AGND Open (no connection)	

DC Electrical Characteristics-Control Inputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Input high voltage RC1, RC2	V_{IH}	2.7			V	
	$\overline{RINGND}$		4.5			V	
2	Input high current RC1, RC2	I_{IH}	25		50	mA	
	$\overline{RINGND}$				-100	µA	
3	Input low voltage RC1, RC2	V_{IL}			0.7	V	
	$\overline{RINGND}$						
4	Input low current RC1, RC2	I_{IL}			1.0	µA	
	$\overline{RINGND}$				1.1	mA	

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DC Electrical Characteristics - TIP/RING Line State Outputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Output High Voltage (TG, RG, RV, FC, RG)			4.75		V	No load on output
2	Output High Current (TG, RG, RV, FC, RG)			0.17		mA	$V_{OH} \equiv 2.7V_{DC}$
3	Output Low Voltage (TG, RG, RV, FC, RG)			0.30		V	No load on output
4	Output Low Sink Current (TG, RG, RV, FC, RG)			0.40		mA	$V_{OL} \equiv 0.4V_{DC}$

* Typical figures are at 25°C with nominal V_{DD} and V_{EE} supplies. For design aid only, not guaranteed and not subject to production testing.

AC Electrical Characteristics - Audio Transmission

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Ringing Voltage	V_R	40	90	130	V_{RMS}	
2	Ringing Frequency			20		Hz	Ringing Type A, RS-464
3	Operating Loop Current	I_L	18		70	mA	
4	Off-Hook DC Resistance	R_T			300	Ω	@ 18mA
5	Operating Loop Resistance	R_L			2300	Ω	@ 18mA
6	On-Hook Leakage Current			3		µA	RING-GND = 5.0 V_{DC}
7	Ring Ground Sink Current	I_{RG}			100	mA	-48V with 200Ω in series on Ring lead
8	Tip and Ring AC Impedance			600		Ω	with 10kΩ + 1.0µF in parallel with Tip and Ring
9	Longitudinal Balance metallic to longitudinal		60 40			dB dB	200 - 1000 Hz 1000 - 4000 Hz
	longitudinal to metallic		58 53			dB dB	200 - 1020 Hz 1020 - 3020 Hz
10	Return Loss Trunk to Line		20 26 30			dB dB dB	200 - 500 Hz 500 - 1000 Hz 1000 - 3400 Hz
11	Transhybrid loss (single frequency into 600Ω)	THL		18.5 34 30		dB dB dB	200 Hz 1000 Hz 3000 Hz
12	Transhybrid loss (single frequency into AT&T Compromise)	THL		18 21		dB dB	200 - 1000 Hz 1000 - 4000 Hz
13	Frequency response (Output relative to 1kHz, V_{TR}/V_X and V_R/V_{TR})		-0.15 -0.10 -0.10 -0.15		0.05 0.05 0.05 0.05	dB dB dB dB	200 Hz 300 Hz 3000 Hz 3400 Hz

See Note 1

** Typical figures are at 25°C are for design aid only and not guaranteed or subject to production testing.

Note 1 - Input 0dBm at V_{TR} yields 0.775 V_{RMS} at V_R with 600Ω termination.

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AC Electrical Characteristics - Audio Transmission

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
14	Idle channel noise			8		dBrnC	C-Message
15	Power supply rejection ratio	PSRR		40		dB	
16	Analog signal overload level (adjustable gain)				6	dBm	1 kHz, 0dBm = 0.775V_{RMS} into 600Ω

* Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

Pin Description

Pin #	Name	Description
1	IC	Internal Connection. Must be left open circuit.
2	T	Tip (Input). Normally connected to the "TIP" lead of the C.O.
3	R	Ring (Input). Normally connected to the "RING" lead of the C.O.
4	IC	Internal Connection. Must be left open circuit.
5	IC	Internal Connection. Must be left open circuit.
6	LPGND	Loop Ground. This is the system ground reference with respect to -48 volts.
7	RINGND	Ring Ground (Input). For Ground Start Trunk only a logic low input will enable the trunk circuit to be grounded via the Ring lead through a low resistance (390Ω). This is a signal to the C.O. that the interface is seizing the line.
8	V_{TR}	Connects to the collector of an external transistor (Q1) and T_{XIN} (pin 26) via an external capacitor (C4).
9	Q_E	Connects to the emitter of an external transistor (Q1).
10	Q_B	Connects to the base of an external transistor (Q1).
11	V_{TR}	Connects to the T_{XIN} (pin 27) via an external capacitor (C1).
12	X_A	External relay contact (K1) connection from V_{TR} (pin 8) activated by loop seize control input (RC1).
13	X_B	External relay contact (K1) connection from X_A (pin 14) activated by loop seize control input (RC1).
14	X_C	External relay contact (K1) connection from X_B (pin 13) activated by loop seize control input (RC1).
15	RGND	Relay Ground.
16	RC1	Relay Control 1 (Input). A logic high will activate the relay (K1) to provide loop seize access to Tip and Ring.
17	RD1	Relay Driver 1 (Output). Open collector sinks current when RC1 is high. Diode clamp protected.
18	CD	Clamping Diode. Normally connects to the positive supply voltage.
19	RD2	Relay Driver 2 (Output). Open collector sinks current when RC2 is high. Diode clamp protected.
20	RC2	Relay Control 2 (Input). A logic high will activate the relay (K2) to provide proper biasing to the tip and ring. This input control is used for Ground Start Trunk only.
21	V_R	Audio Receive (Input). The 4-wire audio receive signal input to the interface.
22	G_{SR}	Gain Setting Receive (Input). Normally used to set the receive gain with an external resistor connected to R_{XOUT} (pin 23).
23	R_{XOUT}	Audio Receive Signal (Output). Connects to the R_{XIN} (pin 22) via an external decoupling capacitor (C3).

* (Component designations refer to Figure 2 unless otherwise stated)

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Pin Description†

Pin #	Name	Description
24	V_{CC+}	**Positive Analog Power Supply Voltage** (+12V).
25	V_{CC-}	**Negative Analog Power Supply Voltage** (−12V).
26	T_{XIN-}	**Transmit (Input) Differential audio signal from V_{TR}** (pin 8), via an external capacitor (C4).
27	T_{XIN+}	**Transmit (Input) Differential audio signal from V_{TR}** − (pin 11), via an external decoupling capacitor (C1).
28	GS_X	**Gain Setting Transmit (Input). Normally used to set the transmit gain with an** external resistor connected to V_X (pin 29).
29	V_X	**Audio Transmit (Output).** The 4-wire audio signal output from the interface.
30	NETBAL	**Network Balance (Input). When there is no connection (open), the network is** balanced at 600Ω. When this pin is grounded, the network is balanced at AT&T compromise.
31	R_{XIN-}	**Differential Receive (Input). Connects to analog ground via an external capacitor (C2).**
32	R_{XIN+}	**Differential Receive (Input). Connects to R_{XOUT}** (pin 23) via an external capacitor (C3).
33	AGND	**Analog Ground.**
34	V_{EE}	**Negative Power Supply** (−5V).
35	V_{DD}	**Positive Power Supply** (+5V).
36	$\overline{TG}$	**Tip Lead Ground Detect (Output).** Active low.
37	$\overline{RC}$	**Reverse Loop Current Detect (Output).** Active low.
38	$\overline{RV}$	**Ringing Voltage Detect (Output).** Active low.
39	$\overline{FC}$	**Forward Loop Current Detect (Output).** Active low.
40	$\overline{RG}$	**Ring Lead Ground Detect (Output).** Active low.

† Component designations refer to figure 2 unless otherwise stated.

Functional Description

The MH88630 is a Central Office Loop Start and/or Ground Start Analog Trunk Interface circuit providing complete audio and signalling link to the Central Office.

The trunk interface circuit performs transformerless 2- to 4-wire conversion between the 2-wire telephone loop and the 4-wire transmit and receive pairs of a voice switching system. The 4-wire connection can be interfaced to a filter/codec, such as the MT896X for use in a digital voice switched system.

Voiceband analog signals coming from the C.O., applied differentially across Tip and Ring, pass through a bridge rectifier and appear at V_{TR+} and V_{TR-} where they are actively terminated. Refer to Fig. 2 Application Circuit. External capacitors C1 and C4 couple the incoming signals into the balanced input of the receive audio circuitry via T_{XIN+} and T_{XIN-}. The receive gain is adjusted by feedback resistor R4. For best performance R4 should be physically located as close as possible to the GS_X pin. The gain adjusted receive signal appears at the V_X output pin.

Relay K1 is the loop seize relay which applies active line termination and also provides biasing of the current modulator circuitry. Activating and deactivating K1 provides dial pulsing. Q1 is the current modulator output transistor, referred to as the loop driver transistor.

Outgoing analog signals from the system are provided to the receive gain at the V_R input where they enter an amplifier section with the gain controlled by the selection of the T_X gain feedback resistor R3. For best performance R3 should be physically located as close as possible to the GS_R pin. The output of the amplifier, R_{XOUT}, is coupled to R_{XIN}, the current modulator circuitry, via C3. The balanced input to the current modulator is completed with the connection of C2 from R_{XIN+} to ground. Transmission across the C.O. is accomplished by modulating the loop with the outgoing analog signals. To ensure that the transmitted signals are not coupled to the receive circuitry, transhybrid loss is maximized. The impedance matching, performed by the balanced network, reduces power loss and

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signal reflections. The network balance input, NETBAL, provides the interface's 2-wire to 4-wire converter circuitry with the ability to match a 600Ω balance when feeding channel banks or when performing receive tests on the trunk circuit or the AT&T compromise. With the NETBAL input pin left open, the interface is balanced to 600Ω. If the NETBAL input pin is grounded, the interface is balanced against the AT&T compromise network consisting of 350Ω plus 1kΩ shunted by a 0.21μF capacitor. This is intended for typical North American C.O. connections.

The Tip and Ring also enter the balanced input of the signal detection circuitry which provides the signalling status outputs $\overline{TG}$, $\overline{RC}$, RV, $\overline{FC}$, and $\overline{RG}$.

For Ground Start signalling, relay K2 and resistors R1 and R2, are required. Activation of K2 is controlled by the relay control logic input signal RC2. In the idle state, K2 is closed connecting the -48 V supply to Tip and Ring through biasing resistors R1 and R2. Upon detection of $\overline{TG}$ or $\overline{RG}$, the system then pulls RC1 low, closing K1, then pulls RC2 low which opens K2 to remove the -48 volt supply from Tip and Ring.

In the Ground Start signalling environment, initiating a call to the C.O. is performed by the following sequence of events. The system provides a logic low on the ring ground input pin of the interface. This activates the circuitry which grounds the ring lead through a current limiting resistance. The C.O. recognizes the ground condition and connects the tip lead to ground. The interface senses this condition and the tip lead ground detect output switches to a logic low. The system then applies active line termination by closing K1 using RC1 and opens K2 using RC2. A call from the C.O. can be performed similarly. The C.O. can signal to the interface by pulling either Tip or Ring to ground potential, or by applying ringing voltage to the ring lead.

Signal Detection Circuitry

The signal detection circuitry provides the signalling status outputs. The system controlling the interface monitors these active low logic outputs.

$\overline{RV}$ is the Ringing Voltage Detect output. When the C.O. applies ringing voltage to the termination the trunk interface presents a 50ms debounced output at $\overline{RV}$ during the ringing burst period. This output will remain low for approximately 50ms after the C.O. removes the ringing voltage. Ringing voltage above 40 V_{RMS} at 20 Hz will be detected.

$\overline{TG}$ is the Tip Lead Ground detect output and $\overline{RG}$ is the Ring Lead Ground detect output. The $\overline{TG}$ and $\overline{RG}$ outputs provide a means of determining call origination or other handshaking functions. The high impedance detection circuitry of the interface will detect both Tip Ground and Ring Ground voltages above approximately −15.3V of true ground.

$\overline{RC}$ is the Reverse Loop Current detect output and $\overline{FC}$ is the Forward Loop Current detect output. The $\overline{RC}$ and $\overline{FC}$ outputs of the interface are used to determine the polarity of the Tip and Ring pair which the C.O. uses for signalling during the active (off-hook) state of the interface. When the loop is closed by the interface, the trunk is in the normal or unreversed state. Some C.O.'s may reverse the polarity of Tip and Ring, to indicate the talking state. The interface will detect this condition and $\overline{RC}$ will output a low level.

External Circuitry Requirements

The loop seize circuit is completed with the addition of external components Q1, C5, R5 and K1.

K1 is a DPST reed relay, that is activated by relay control signal RC1. When loop seizure is required, K1 is closed and the interface applies active termination across Tip and Ring. The relay should have a 0.5 amp contact capability and 12 V operation with a typical 500Ω coil resistance. To prevent back EMF from damaging the relay drive transistor (caused by the collapsing inductive coil of the relay), snubbing diode is provided externally. C5 and R5 provide relay contact noise filtering and transient noise suppression necessary for clamping inductive spikes created when the loop is closed during line seizure or dial pulsing.

Q1 provides current drive for the active termination, controlling the loop current flow of the current modulator circuitry. Device choice of a suitable transistor for Q1 is made based on worst case conditions which include fault conditions. A 350 volt, or higher, rating for Q1 is necessary to meet high voltage requirements. The Tip and Ring input protection varistors limit any high voltage spikes to approximately 200 volts. Under worst case conditions Q1 must be able to handle close to 100mA of collector current and dissipate two watts continuously. During pulse dialing, current spikes are generated due to the inductive nature of the loop. A 0.5 amp continuous collector current rating is therefore recommended to provide a safe margin.

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K2, R1 and R2 are required only for Ground Start applications. K2 is the same type of relay as K1 and is activated by RC2. Once again the snubbing diode is provided on the hybrid. R1 and R2 provide the -48V biasing during the ringing (loop closure) state.

R6 and C6 constitute the Dummy Ringer required for the SLIC trunk. These components are also part of the 600Ω input impedance.

Overvoltage protection may be required depending upon the interface application. For maximum protection it is recommended to place fuses in series with the Tip and Ring inputs of the interface followed by metal oxide varistors from Tip to Ground, Ring to Ground and Tip to Ring.

Component List

R1*, R2*	= 30.9kΩ, 1%, ¼w	
R3	= Transmit Gain Adjust Resistor = 301.5kΩ x Gain (V/V) - 100Ω Typical Value = 200kΩ, 1%, ¼w	
R4	= Receive Gain Adjust Resistor = 523.53Ω x Gain (V/V) Typical Value = 505kΩ, 1%, ¼w	
R5	= 510Ω, 5%, ¼w	
R6	= 10kΩ, 5%, ¼w	
C1, C2, C3, C4	= 0.22µF, 10%, 200V	
C5	= 0.1µF, 5%, 250V	
C6	= 1.0µF, 5%, 250V	
Q1	= 2N6657, NPN, 350V, 0.5A, 20W	
K1, K2*	= 2A Reed Relay, 12V, 2 FormC Dip	

*Note: Required for Ground Start applications, not required for Loop Start applications.

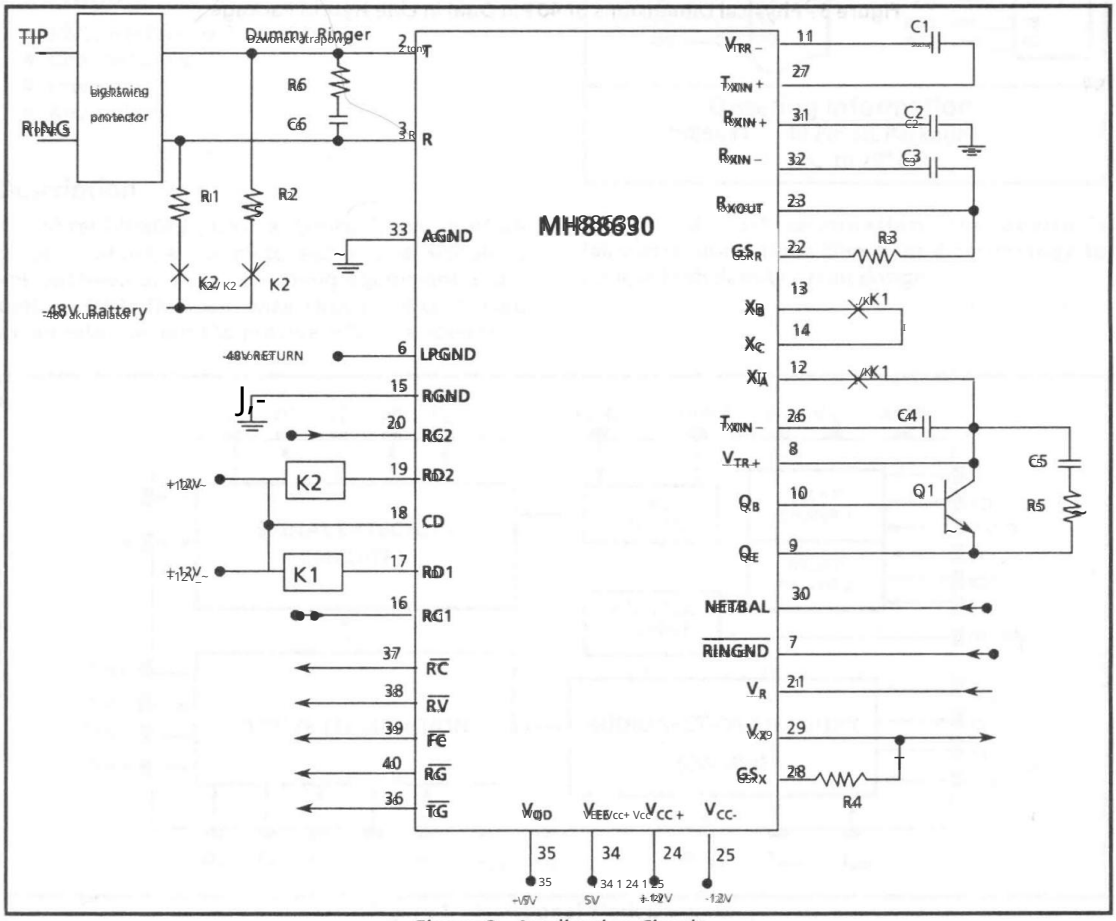

Figure 2 - Application Circuit

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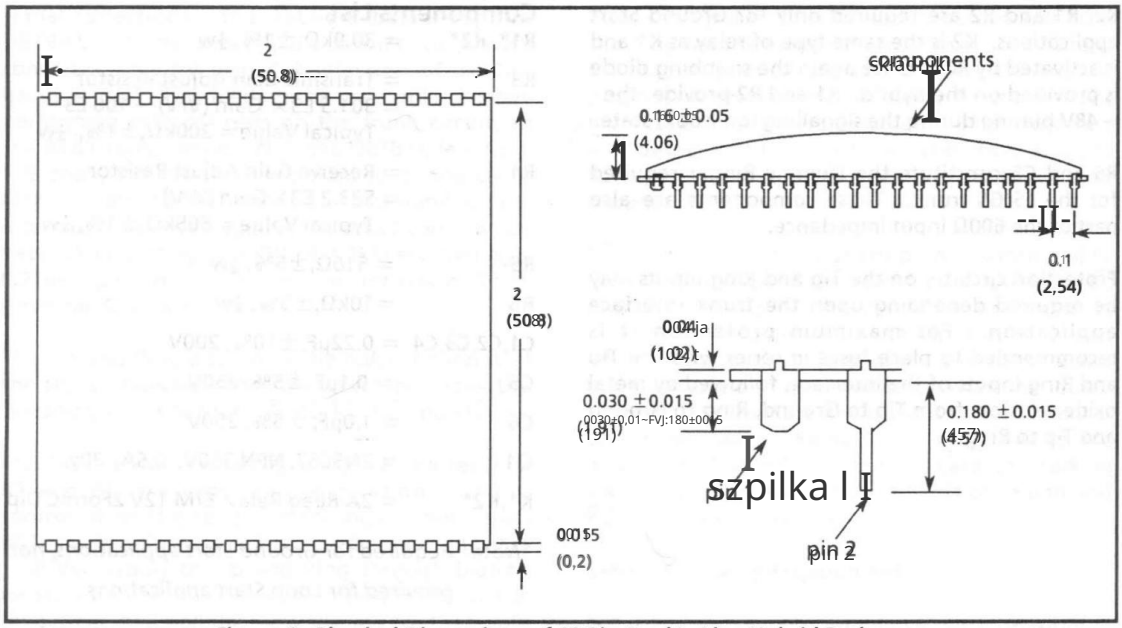

Figure 3 – Physical Dimensions of 40 Pin Dual In Line Hybrid Package

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Features

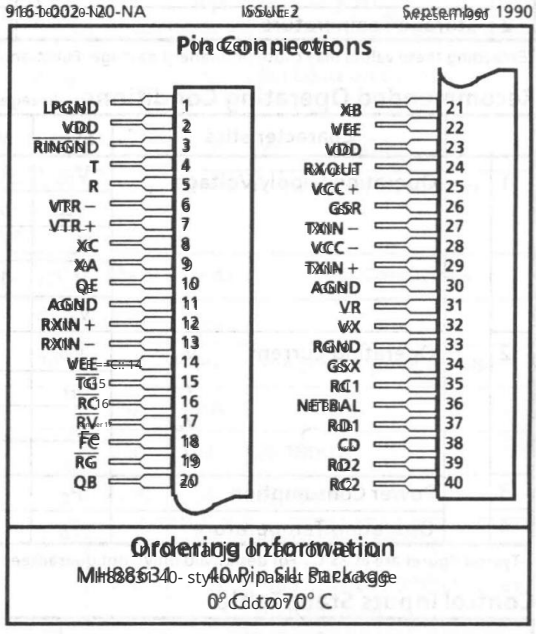
- Transformerless 2W-to-4W conversion
- Wyjścia wykrywania stanu linii:
  - forward current
  - reverse current
  - ring ground
  - tip ground
  - ringing voltage
- Programmable audio transmit and receive gain
- Loop start or ground start termination
- Selectable 600Ω or AT&T compromise balance network

Applications

- PBX interface to Central Office
- Channel bank
- Intercom
- Key system

Description

The MHS8631 Central Office Trunk Interface circuit provides complete audio and signalling link between an audio switching equipment and a central office. The loop seize circuitry is controlled by an external input to provide either a loop start



Ordering Information
MHS8631 40 Pin SIL Package
0° C to 70° C

or zakończenie rozruchu uziemienia. Urządzenie jest wykonane przy użyciu technologii hybrydowej grubowarstwowej aby osiągnąć projekt o dużej gęstości.

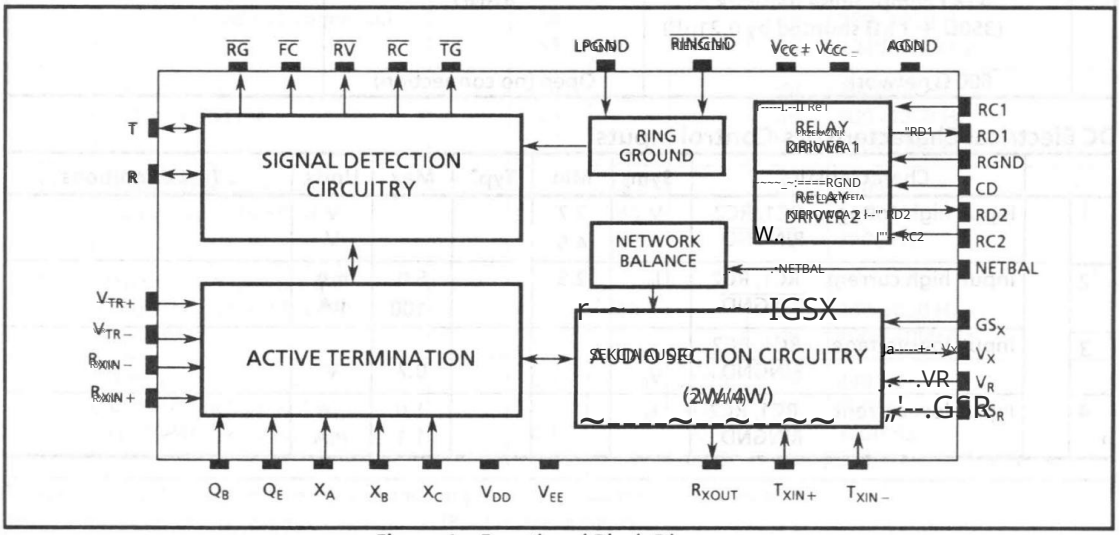


Figure 1. Functional Block Diagram

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Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD} - GNDD	-0.3	+6.0	V
		V_{EE} - GNDD	-6.0	+0.3	V
		V_{CC+} - GNDA		+18.0	V
		V_{CC-} - GNDA	-18.0		V
2	Storage Temperature	T_{STG}	-55	+125	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

All voltages are referenced to GNDD unless otherwise stated. GNDA is always at the same potential as GNDD.

	Characteristics	Sym	Min	Typ*	Max	Units	Comments
1	Operating Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
		V_{EE}	-5.25	-5.0	-4.75	V	
		V_{CC+}	11.4	12.0	12.6	V	
		V_{CC-}	-11.4	-12.0	-12.6	V	
		V_{BAT}		-48.0		V	
2	Operating Current V_{DD}	I_{DD}			6.0	mA	RINGND High
	V_{EE}	I_{EE}			-6.0	mA	
	V_{CC+}	I_{CC+}			8.0	mA	
	V_{CC-}	I_{CC-}			-8.0	mA	
3	Power Consumption	P_C			265	mW	
4	Operating Temperature	T_O	0		70	°C	

*Typical figures are at 25°C for design aid only: not guaranteed and not subject to production testing.

Control Inputs State Table

	Parameter	Active	Idle
1	RC1	Logic High	Logic Low
2	RC2	Logic High	Logic Low
3	$\overline{RINGND}$	Logic Low	Logic High
4	NETBAL	AT&T compromise network (350Ω + 1kΩ shunted by 0.21µF)	AGND
		600Ω network	Open (no connection)

DC Electrical Characteristics - Control Inputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Input high voltage RC1, RC2	V_{IH}	2.7			V	
	$\overline{RINGND}$		4.5			V	
2	Input high current RC1, RC2	I_{IH}	2.5		5.0	mA	
	$\overline{RINGND}$				100	µA	
3	Input low voltage RC1, RC2	V_{IL}			0.7	V	
	$\overline{RINGND}$						
4	Input low current RC1, RC2	I_{IL}			1.0	µA	
	$\overline{RINGND}$				1.1	mA	

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DC Electrical Characteristics - TIP/RING Line State Outputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Output High Voltage ($\overline{TG}$, $\overline{RC}$, $\overline{RV}$, FC, RG)			4.75		V	No Load on output
2	Output High Current ($\overline{TG}$, $\overline{RC}$, $\overline{RV}$, FC, RG)			0.17		mA	V_{OH} = 2.7V_{DC}
3	Output Low Voltage ($\overline{TG}$, $\overline{RC}$, $\overline{RV}$, FC, RG)			0.30		V	No Load on output
4	Output Low Sink Current ($\overline{TG}$, $\overline{RC}$, $\overline{RV}$, FC, RG)			0.40		mA	V_{OL} = 0.4V_{DC}

*Typical figures are at 25°C with nominal V_{CC} and V_{EE} and are for design aid only: not guaranteed and not subject to production

AC Electrical Characteristics - Audio Transmission

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Ringing Voltage	V_R	40	90	130	V_{RMS}	
2	Ringing Frequency			20		Hz	Ringing Type A, RS-464
3	Operating Loop Current	I_L	18		70	mA	
4	Off-Hook DC Resistance	R_T			300	Ω	@ 18mA
5	Operating Loop Resistance	R_L			2300	Ω	@ 18mA
6	On-Hook Leakage Current			3		μA	$\overline{RINGND}$ = 5.0V_{DC}
7	Ring Ground Sink Current	I_{RG}		100		mA	-48V with 200Ω in series on Ring lead
8	Tip and Ring AC Impedance			600		Ω	with 10kΩ + 1.0μF in parallel with Tip and Ring
9	Longitudinal Balance metallic to longitudinal			60 40		dB dB	200 - 1000 Hz 1000 - 4000 Hz
	longitudinal to metallic			58 53		dB dB	200 - 1020 Hz 1020 - 3020 Hz
10	Return Loss Trunk to Line			20 26 30		dB dB dB	200 - 500 Hz 500 - 1000 Hz 1000 - 3400 Hz
11	Transhybrid Loss (single frequency) into 600Ω	THL		18.5 34 30		dB dB dB	200 Hz 1000 Hz 3000 Hz
12	Transhybrid Loss (single frequency) into AT & T Compromise	THL		18 21		dB dB	200 - 1000 Hz 1000 - 4000 Hz
13	Frequency response (Output relative to 1 kHz, V_{TR}/V_X and V_R/V_{TR})		-0.15 -0.10 -0.10 -0.15		0.05 0.05 0.05 0.05	dB dB dB dB	200 Hz 300 Hz 3000 Hz 3400 Hz See Note 1

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 1 - Input 0dBm at V_{TR} or input 0.775 V_{RMS} at V_R with 600Ω termination.

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AC Electrical Characteristics — Audio Transmission

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
14	Idle channel noise			8		dBrnC0	C-Message
15	Power supply rejection ratio	PSRR		40		dB	
16	Analog signal overload level (adjustable gain)				6	dBm	1 kHz, 0dBm = 0.775V$_{RMS}$ into 600Ω

* Typical figures at 25°C are for design aid only and not guaranteed or subject to production testing.

Pin Description

Pin #	Name	Description
1	LPGND	Loop Ground is the system ground reference with respect to -48 volts.
2	V_{DD}	Positive Power Supply (+5V).
3	$\overline{RING}_{GND}$	Ring Ground (Input). For Ground Start trunks only, a logic low input will enable the ring circuit to ground the Ring lead through a low resistance (390Ω). This is a signal to the C.O. that the interface is seizing the line.
4	T	Tip (Input). Normally connects to the "TIP" lead of the C.O.
5	R	Ring (Input). Normally connects to the "RING" lead of the C.O.
6	V_{TR}-	Connects to the T_{XIN}- (pin 29) via an external capacitor (C1).
7	V_{TR}+	Connects to the T_{XOUT} (pin 27) via an external capacitor (C4).
8	X_C	External relay contact (K1) connection from X_A (pin 9), activated by loop seize control input ($\overline{RC}$).
9	X_A	External relay contact (K1) connection from V_{TR}+ (pin 7), activated by loop seize control input ($\overline{RC}$).
10	Q_E	Connects to the emitter of an external transistor (Q1).
11	AGND	Analog Ground.
12	R_{XIN}+	Differential Receive (Input). Connects to analog ground via an external capacitor (C2).
13	R_{XIN}-	Differential Receive (Input). Connects to R_{XOUT} (pin 24) via an external capacitor (C3).
14	V_{EE}	Negative Power Supply (−5V).
15	$\overline{TG}$	Tip Lead Ground Detect (Output). Active low.
16	$\overline{RC}$	Reverse Loop Current Detect (Output). Active low.
17	$\overline{RV}$	Ringing Voltage Detect (Output). Active low.
18	$\overline{FC}$	Forward Loop Current Detect (Output). Active low.
19	$\overline{RG}$	Ring Lead Ground Detect (Output). Active low.
20	Q_B	Connects to the base of an external transistor (Q1).
21	X_B	External relay contact (K1) connection from X_C (pin 8), activated by loop seize control input ($\overline{RC}$).
22	V_{EE}	Negative Power Supply (−5V).
23	V_{DD}	Positive Power Supply (+5V).
24	R_{XOUT}	Audio receive signal (output) to the R_{XIN}- (pin 13) via an external decoupling capacitor (C3).
25	V_{CC}+	Positive Analog Power Supply Voltage (+12V).
26	G_R	Gain Setting Resistor (Input). Normally used to set the receive gain with an external resistor connected to R_{XOUT} (pin 24).

* Component tolerances do not reflect to Figure 2 unless otherwise stated.

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Pin Description†

Pin #	Name	Description
27	$T_{XIN}-$	**Transmit (Input).** Differential audio signal from V_{TR+} (pin 7) via an external capacitor (C4).
28	$V_{CC}-$	**Negative Analog Power Supply Voltage (−12V).**
29	T_{XIN+}	**Transmit (Input).** Differential audio signal from V_{TR-} (pin 6), via an external decoupling capacitor (C1).
30	AGND	**Analog Ground.**
31	V_R	**Audio Receive (Input).** The low-level audio signal input to the interface.
32	V_X	**Audio Transmit (Output).** The low-level audio signal output from the interface.
33	RGND	**Relay Ground.**
34	GS_X	**Gain Setting Transmit (Input).** Normally used to set the transmit gain with an external resistor connected to V_X (pin 32).
35	RC1	**Relay Control 1 (Input).** A logic high will activate the relay (K1) to provide loop access to the Tip and Ring.
36	NETBAL	**Network Balance (Input).** When there is no connection (open), the network is balanced at 600Ω. When this pin is grounded, the network is balanced at AT&T compromise.
37	RD1	**Relay Driver 1 (Output).** Open collector sinks current when RC1 is high. Diode clamp protected.
38	CD	**Clamping Diode.** Normally connects to the positive supply voltage.
39	RD2	**Relay Driver 2 (Output).** Open collector sinks current when RC2 is high. Diode clamp protected.
40	RC2	**Relay Control 2 (Input).** A logic high will activate the relay (K2) to provide proper biasing to the microphone. This input can be used for Ground Start trunks only.

†Component designations refer to figure 2, unless otherwise stated.

Functional Description

The MH88631 trans-hybrid interface circuit provides complete audio and signalling link to the Central Office.

The trunk interface circuit performs transformerless 2-to-4-wire conversion, between the 2-wire telephone loop and the 4-wire transmit and receive pairs of a voice switching system. The 4-wire connection can be interfaced to a filter/codec such as the MT8960X for use in a digital switched system.

Incoming analog signals coming from the C.O., applied differentially across Tip and Ring, pass through bridge rectifiers and appear at V_{TR+} and V_{TR-}, where they are actively terminated. Refer to Fig. 2 - Application Circuit. External capacitors C1 and C4 couple the incoming signals into the balanced inputs of the receive audio circuitry via T_{XIN+} and T_{XIN-}. The receive gain is adjusted by feedback resistor R4. For best performance, R4 should be physically located as close as possible to the GS_X pin. The gain adjusted receive signal appears at the V_X output pin.

Relay K1 is the loop seize relay which applies active line termination and also provides biasing of the microphone. Activating and deactivating K1 provides dial pulsing. Q1 is the current mode output transistor referred to as the hybrid driver transistor.

Outgoing analog signals from the system are provided to the interface at the V_R input where they are amplified with the gain controlled by the selection of the T_X gain feedback resistor R3. For best performance, R3 should be physically located as close as possible to the GS_R pin. The output of the receive amplifier, R_{XOUT}, is coupled to R_{XIN-} via C3. The balanced input to the current mode modulator is completed with the connection of C2 from R_{XIN+} to ground. Transmission to the C.O. is accomplished by modulating the loop with the outgoing analog signals. To prevent these transmitted signals are not coupled to the receive circuitry, a hybrid loss is maximized. The impedance matching is performed by the balanced network, which also reduces power loss and

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signal reflections. The network balance input, NETBAL, of the interface's 2 wire to 4 wire converter circuitry provides selection of a 600Ω balance used when feeding channel banks or when performing external tests on the trunk circuit, or the AT&T compromise. With the NETBAL input pin left open the interface is balanced to match to 600Ω. If the NETBAL input pin is grounded the interface is balanced against the AT&T compromise network consisting of 350Ω plus 1kΩ shunted by a 0.21μF capacitor. This is intended for typical North American C.O. connections.

The Tip and Ring also enter the balanced input of the signal detection circuitry which provides the signalling status outputs $\overline{TG}$, $\overline{RC}$, $\overline{RV}$, $\overline{FC}$, and $\overline{RG}$.

For Ground Start signalling, relay K2 and resistors R1 and R2, are required. Activation of K2 is controlled by the relay control logic input signal RC2. In the idle state K2 is closed connecting the -48 V supply to Tip and Ring through biasing resistors R1 and R2. Upon detection of $\overline{TG}$ or $\overline{RG}$, the system then pulls RC1 low, closing K1, then pulls RC2 low which opens K2 to remove the -48 volt supply from Tip and Ring.

In the Ground Start signalling environment, initiating a call to the C.O. is performed by the following sequence of events. The system provides a logic low to the ring ground input of the interface. This activates the circuitry which grounds the ring lead through a current limiting resistance. The C.O. recognizes the ground condition and connects the tip lead to ground. The interface senses this condition and the tip lead ground detect output switches to a logic low. The system then applies the loop termination by closing K1 using RC1 and opens K2 using RC2. A call from the C.O. is performed similarly. The C.O. can signal to the interface by pulling either Tip or Ring to ground potential, or by applying ringing voltage to the ring lead.

Signal Detection Circuitry

The signal detection circuitry provides the signalling status outputs. The system controlling the interface monitors these active low logic outputs.

$\overline{RV}$ is the Ringing Voltage detect output. When the C.O. applies ringing voltage to the terminating trunk interface provides a 50ms debounced output at $\overline{RV}$ in the ringing cadence. The output will remain low for approximately 50ms after the C.O. removes the ringing voltage. Ringing voltage above 40 V_{RMS} at 20 Hz will be detected.

$\overline{TG}$ is the Tip lead Ground detect output and $\overline{RG}$ is the Ring lead Ground detect output. The $\overline{TG}$ and $\overline{RG}$ outputs provide a means of determining call origination or other handshaking functions. The high impedance detection circuitry of the interface will detect both Tip Ground and Ring Ground voltages above approximately −15.3V of true ground.

$\overline{RC}$ is the Reverse loop Current detect output and $\overline{FC}$ is the Forward loop Current detect output. The $\overline{RC}$ and $\overline{FC}$ outputs of the interface are used to determine the polarity of the Tip and Ring pair which the C.O. uses for signalling during the active (off-hook) state of the interface. When the loop is closed by the interface, the trunk is in the normal or unreversed state. Some C.O.'s may reverse the polarity of Tip and Ring, to indicate the talking state. The interface will detect this condition and $\overline{RC}$ will output a low level.

External Circuitry Requirements

The loop seize circuit is completed with the addition of external components Q1, C5, R5 and K1.

K1, a DPST relay, is activated by relay control signal RC1. When loop seizure is required, K1 is closed and the interface applies active termination across Tip and Ring. The relay should have a 0.5 amp contact capability and 12 V_{DC} operation with a typical 500Ω coil resistance. To prevent back EMF from damaging the relay drive transistor (caused by the collapsing field of the inductive coil of the relay), a snubbing diode is provided on the hybrid and, therefore not needed externally. C5 and R5 provide relay contact noise filtering and transient noise suppression necessary for clamping inductive spikes created when the loop is closed during line seizure or dial pulsing.

Q1 provides the current drive for the active termination controlled by the current flow of the current modulator circuitry. Suitable ratings for Q1 should be based on worst case conditions which include fault conditions. A 350 volt or higher rating for Q1 is necessary to meet high voltage requirements. The Tip and Ring input protection varistors limit any high voltage spikes to approximately 300 volts. Under worst case conditions Q1 must be able to handle close to 100mA of collector current and dissipate two watts continuously. During pulse dialing, current spikes are generated due to the inductance of the loop. A 0.5 amp continuous collector current rating is therefore recommended to provide a safe margin.

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K2, R1 and R2 are required only for Ground Start applications. K2 is the same type of relay as K1 and is activated by RC2. Once again the snubbing diode is provided on the hybrid. R1 and R2 provide the -48V biasing during the signalling (on hook) state.

K2, R1 i R2 są wymagane tylko do startu z ziemi. Zastosowanie K2 jest tym samym typem przekaźnika co K1 i jest aktywowany przez RC2. Ponownie dioda tłumiąca jest dostarczana w hybrydzie. R1 i R2 zapewniają -48V polaryzację w stanie sygnalizacji (odłożenia słuchawki).

R6 and C6 constitute the Dummy Ringer required for the LS/GS trunk. These components are also part of the 600Ω input impedance.

R6 i C6 stanowią wymagany dzwonek Dummy dla LS/GS trunk. Te komponenty są również część 600Ω impedancji wejściowej.

Protection circuitry on the Tip and Ring inputs may be required depending upon the trunk interface application. For maximum protection it is recommended to place fuses in series with the Tip and Ring inputs of the interface, followed by metal oxide varistors from Tip to Ground, Ring to Ground and Tip to Ring.

Obwody zabezpieczające na wejściach Tip i Ring mogą być wymagane w zależności od interfejsu trunk aplikacja. Dla maksymalnej ochrony zaleca się umieszczanie bezpieczników szeregowo z końcówką i wejściami pierścieniowymi, a następnie warystory tlenkowe od czubka do uziemienia, od pierścienia do uziemienia i od końcówki do pierścienia.

Components List

Lista składników

R1*,R2*	= 30.9kΩ, ±1%, ¼w	= 30,9kΩ, ±1%, ¼w
R3	= Transmit Gain Adjust Resistor	= Rezystor regulacji wzmocnienia transmisji
	= 30.15 E3 × Gain (V/V) − 10.0 E3	= 30,15E3 × Wzmocnienie (V/V) − 10,0E3
	Typical Value = 20kΩ, ±1%, ¼w	Wartość typowa = 20kΩ, ±1%, ¼w
R4	= Receive Gain Adjust Resistor	= Odbierz rezystor regulacji wzmocnienia
	= 523.2 E3 × Gain (V/V)	= 523,2 E3 × Wzmocnienie (V/V)
	Typical Value = 505kΩ, ±1%, ¼w	Wartość typowa = 505kΩ, ±1%, ¼w
R5	= 510Ω, ±5%, ¼w	= 510Ω, ±5%, ¼w
R6	= 10kΩ, ±5%, ¼w	= 10kΩ, ±5%, ¼w
C1,C2,C3,C4	= 0.22μF, ±10%, 200V	= 0,22μF, ±10%, 200V
C5	= 0.1μF, ±5%, 250V	= 0,1μF, ±5%, 250V
C6	= 1.0μF, ±5%, 250V	= 1,0μF, ±5%, 250V
Q1	= 2N5657, NPN, 350V, 0.5A, 20w	= 2N5657, NPN, 350V, 0,5A, 20w
K1,K2*	= 2A Reed Relay, F/M, 12V, 2Form C	= 2A przekaźnik kontaktronowy, F/M, 12V, 2Form C
	Dip	Dip

*Note: Required for Ground Start applications, not required for Loop Start applications.

*Uwaga: Wymagane w przypadku aplikacji Ground Start, nie wymagane dla aplikacji Loop Start.

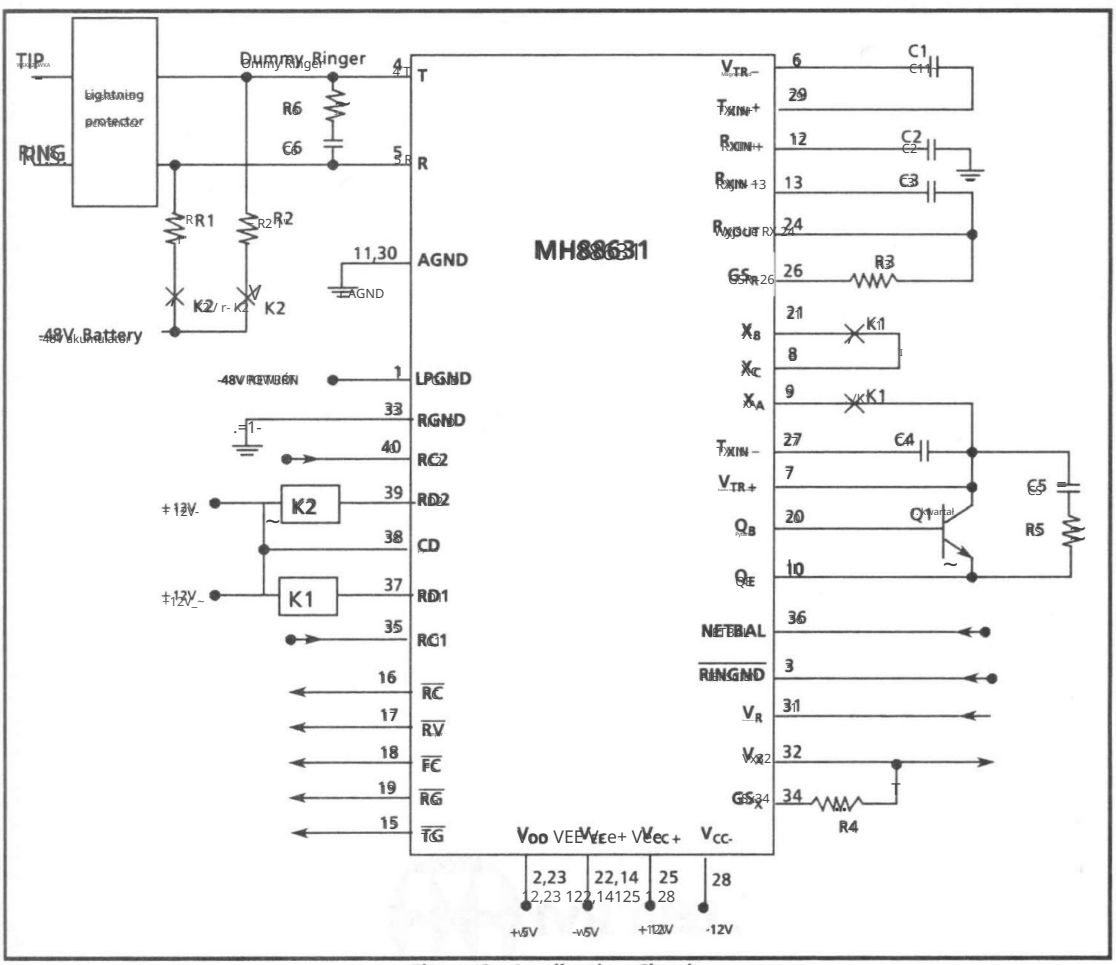

Figure 2 - Application Circuit

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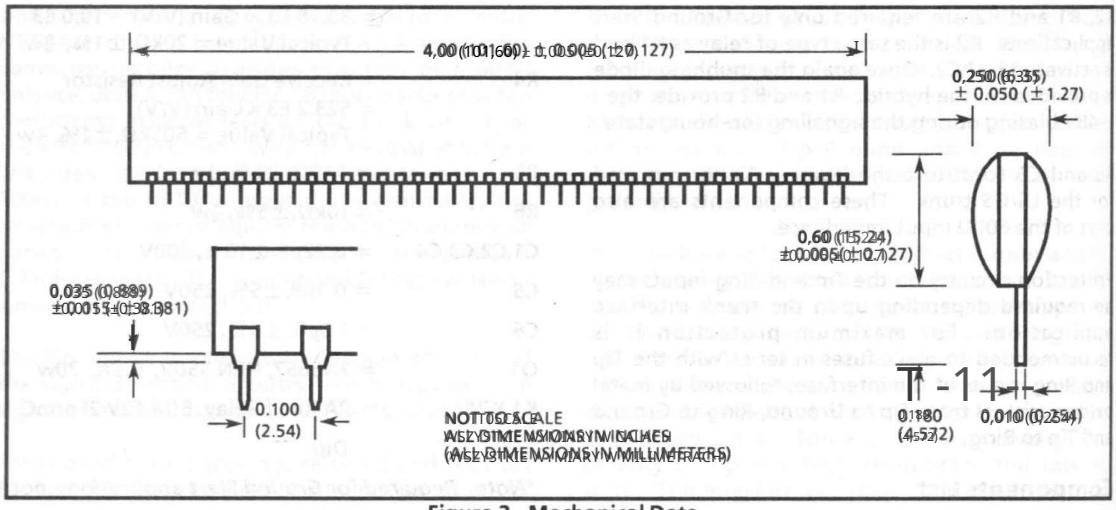

Figure 3 - Mechanical Data

Rysunek 3 - Dane mechaniczne

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MODEMS AND SUPPORT COMPONENTS

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9161 002 03801 NA Issue 3 November 1990

Features

- Bell 212A and CCITT V.22 compatible
- Usable for Bell 103 and V.22 Bis Applications
- Guard tone notch filters for V.22 Applications
- High and low bandfilters with compromise group delay equalizers and smoothing filters
- Answer/originate operating modes
- Detection of call progress tones
- Choice of clocking frequencies: 2.4576 MHz, 1.2288 MHz, 153.6 kHz
- Analog loopback test capability
- Two uncommitted operational amplifiers
- Pin compatible with AMI S35212A

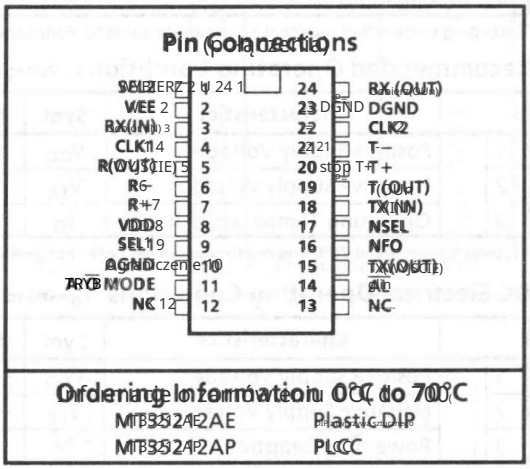
Applications

- Modem filter/equalizer for 1200 bps full duplex modem implementation
- Detection of tones in the call progress band by subscriber interfaces

Description

The MT35212A is an ISO2-CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 modems. The MT35212A includes both the transmit signal shaping filter and the receive signal separation filter, and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included. Provision is made for the receive smoothing filter to switch between the Call Progress mode and the normal data transmission mode.

Pin Connections



Ordering Information 0°C to 70°C

MT35212AE	Plastic DIP
MT35212AP	PLCC

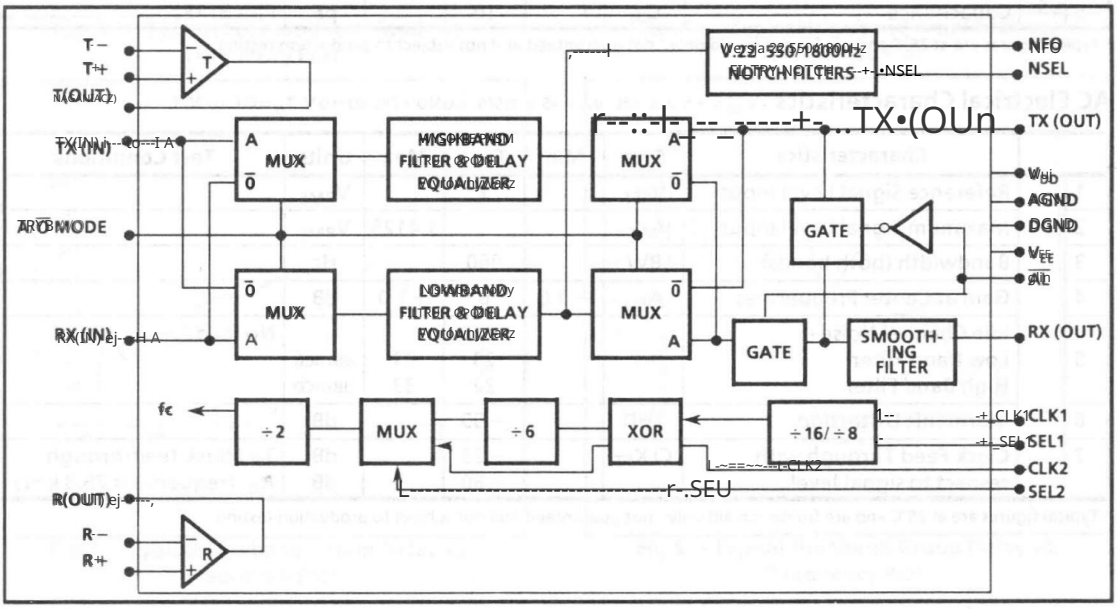


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne wartości dopuszczalne

	Parameter	Symbol	Min	Max	Units
1	Positive Supply Voltage 1 dodatnie napięcie zasilania	V_{DD}		6.75	V
2	Negative Supply Voltage 2 Ujemne napięcie zasilania	V_{EE}		-6.75	V
3	Storage Temperature Range 3 Zakres temperatur przechowywania	T_{STG}	-55	+125	°C
4	Analog Input 4 wejścia analogowe	V	V_{EE} -0.3	V_{DD} +0.3	V

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Funkcjonalne działanie w tych warunkach nie jest domniemane.

Recommended Operating Conditions - Voltages are with respect to ground unless otherwise stated.

Zalecane warunki pracy - napięcia podano względem uziemienia, chyba że podano inaczej.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Positive Supply Voltage Dodatnie napięcie zasilania	V_{DD}	4.75	5	5.25	V	$V_{DD}-V_{AGND}=$ $V_{DGND}-V_{AGND}=0$ V
2	Negative Supply Voltage Ujemne napięcie zasilania	V_{EE}	-4.75	-5	-5.25	V	$V_{DD}-V_{AGND}=$ $V_{DGND}-V_{AGND}=0$ V
3	Operating Temperature Range Zakres temperatur pracy	T_O	0	25	70	°C	

†Typical figures are at 25°C and are for design aid only - not guaranteed and not subject to production testing.
Typowe wartości liczbowe wynoszą 25°C i służą wyłącznie do celów projektowych - nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Operating Conditions - T_O = 0°C to 70°C.

Warunki pracy prądu stałego - T_O = 0°C do 70°C

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Positive Supply Voltage Dodatnie napięcie zasilania	V_{DD}	+4.75	5.0	5.25	V	
2	Negative Supply Voltage Ujemne napięcie zasilania	V_{EE}	-4.75	-5.0	-5.25	V	
3	Power Consumption Pobór mocy	P_C		75	150	mW	V_{DD} = 5.25V; V_{EE} = -5.25V

†Typical figures are at 25°C and are for design aid only - not guaranteed and not subject to production testing.
Typowe wartości liczbowe wynoszą 25°C i służą wyłącznie do celów projektowych - nie są gwarantowane i nie podlegają testom produkcyjnym.

DC Electrical Characteristics

Charakterystyka elektryczna prądu stałego - V_{DD} = +5V ±5%, V_{EE} = -5V ±5%, A_{GND} = D_{GND} = 0V, T_O = 0°C do 70°C, T_O = 0°C to 70°C.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	I	High Level Logic I Logika wysokiego poziomu	V_{IH}	4		V_{DD}	V	Pins 1, 9, 11, 14, 17. Kołki 1, 9, 11, 14, 17.
2	N P U T	High Level Logic 2 N Wysoki poziom Logic	V_{IH}	2.0		V_{DD}	V	Pins 4, 22. Kołki 4, 22.
3		Low Level Logic Niski poziom logiki	V_{IL}	V_{EE}		0.8	V	Pins 1, 4, 9, 11, 14, 17, 22. Kołki 1, 4, 9, 11, 14, 17, 22.
4		Resistance 4 T Odporny	R_{IN}		5		MΩ	Pins 3, 18. Szpilki 3, 18.
5		Capacitance 5 S Pojemność	C_{IN}		10		pF	Pins 3, 18. Szpilki 3, 18.

†Typical figures are at 25°C and are for design aid only - not guaranteed and not subject to production testing.
Typowe wartości liczbowe wynoszą 25°C i służą wyłącznie do celów projektowych - nie są gwarantowane i nie podlegają testom produkcyjnym.

AC Electrical Characteristics

Charakterystyka elektryczna prądu przemiennego - V_{DD} = +5V ±5%, V_{EE} = -5V ±5%, A_{GND} = D_{GND} = 0V, T_O = 0°C do 70°C.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Reference Signal Level Input Sygnał wejściowy poziomu odniesienia	V_{REEF}		1		V_{RMS}	
2	Maximum Signal Level Input Maksymalny poziom sygnału wejściowego	V_{MAX}			1.4125	V_{RMS}	
3	Bandwidth (both bands) Szerokość pasma (obie pasma)	BW	960			Hz	
4	Gain at Center Frequencies Wzmocnienie w częstotliwościach środkowych	A_{FRQ}	-1.0	0	+1.0	dB	
5	Idle Channel Noise - Low Band Filter Wzmocnienie kanału Filtr pasma niskiego High Band Filter Filtr pasma wysokiego			23 22	33 33	dBrnC0 dBrnC0	No load. Bez obciążenia.
6	Harmonic Distortion Zniekształcenie harmoniczne	THD		-55		dB	
7	Clock Feed Through with respect to signal level Przesłuchowość zegara w odniesieniu do poziomu sygnału	CLK		-23 -60		dB dB	Tx (clock feedthrough frequency is 76.8 kHz) Tx (przepust zegarowy częstotliwość zegara wynosi 76,8 kHz)

†Typical figures are at 25°C and are for design aid only - not guaranteed and not subject to production testing.
Typowe wartości wynoszą 25°C i służą wyłącznie do celów projektowych - nie są gwarantowane i nie podlegają testom produkcyjnym.

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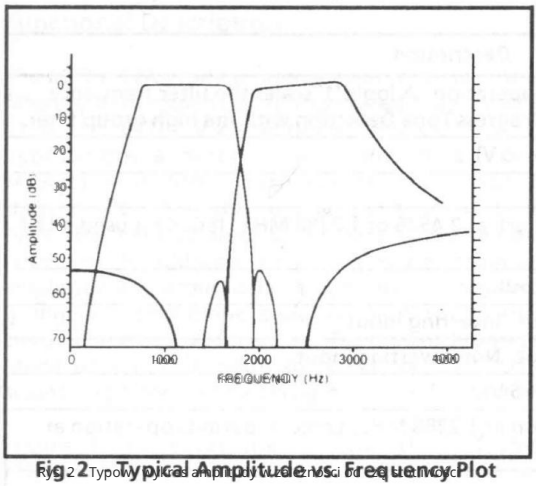

Fig 2 Typical Amplitude vs. Frequency Plot

FREQUENCY (Hz)		RELATIVE GAIN MIN.	MAX.
Lowband	400		-3.5
	800	-1	+1
	1200	-1	+1
	1600	-1.5	+1
	1800		-18
	2000		-48
	2400		-55
	2800		-50
Highband	800		-50
	1200		-53
	1600		-50
	2000	-2.5	+0.5
	2400	-1	+1
	2800	-0	+2.5
	3200		-10
	3500		-20

Table 1 Amplitude vs. Frequency Response

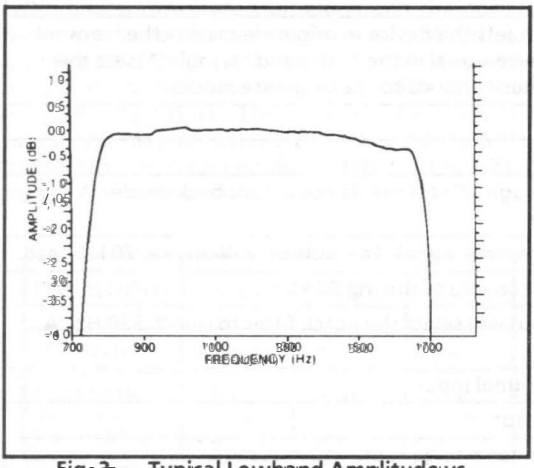

Fig 3 Typical Lowband Amplitude vs. Frequency Plot

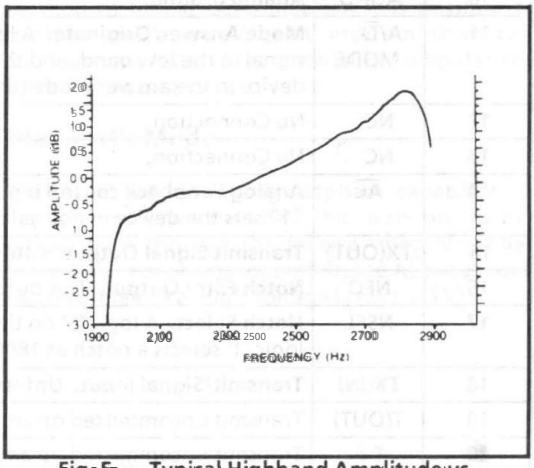

Fig 5 Typical Highband Amplitude vs. Frequency Plot

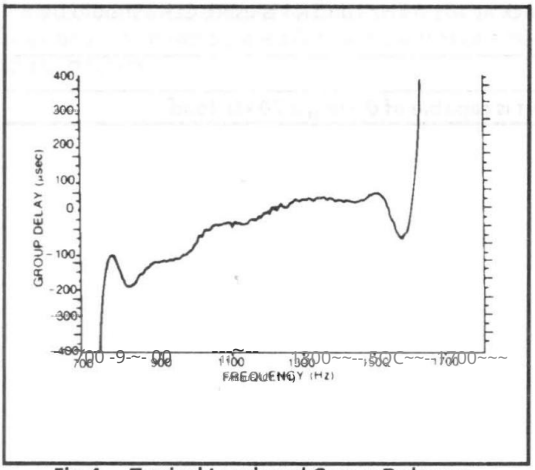

Fig 4 Typical Lowband Group Delay vs. Frequency Plot

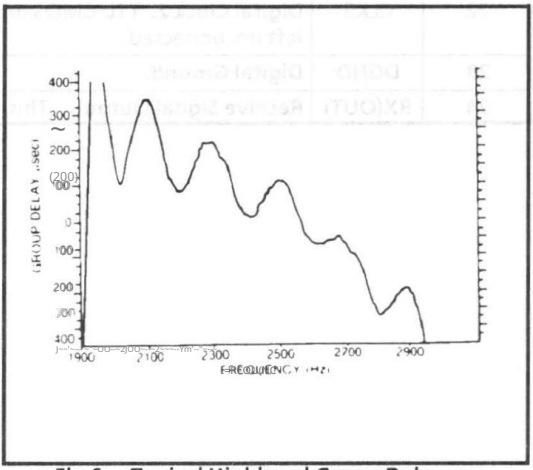

Fig 6 Typical Highband Group Delay vs. Frequency Plot

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Pin Description

Pin #	Name	Description
1	SEL2	**Select 2.** A logic '0' selects operation at 2.4576 MHz. A logic '1' selects operation at 2.2888 MHz.
2	V_{EE}	Negative supply voltage (typically − 5 V).
3	RX(IN)	**Receive signal input.**
4	CLK1	**Digital Clock 1.** TTL/CMOS input clock at 2.4576 or 2.2888 MHz. If CLK2 is used, CLK1 should be left unconnected.
5	R(OUT)	Receive uncommitted Op Amp output.
6	R−	Receive uncommitted Op Amp input, inverting input.
7	R+	Receive uncommitted Op Amp input, Non-inverting input.
8	V_{DD}	Positive supply voltage (typically +5 V).
9	SEL1	**Select 1.** Logic '0' permits operation at 2.2888 MHz; Logic '1' permits operation at 2.4576 MHz.
10	AGND	**Analog ground.**
11	$A/\overline{O}$ MODE	**Mode Answer/Originate.** A logic '0' sets the device in originate mode, the transmit signal is in the low band, and the receive signal in the high band. A logic '1' sets the device in the answer mode (the opposite bands to the originate mode).
12	NC	No Connection.
13	NC	No Connection.
14	$\overline{AL}$	**Analog Loopback control input.** A logic '0' sets the device in analog loopback mode. A logic '1' sets the device in normal mode.
15	TX(OUT)	**Transmit Signal Output.** Filtered transmit signal. This output will drive a 20 kΩ load.
16	NFO	**Notch Filter Output.** This output is capable of driving 20 kΩ.
17	NSEL	**Notch Select.** A logic '0' on this input will select the notch filter to reject 550 Hz. A logic '1' selects a notch at 1800 Hz.
18	TX(IN)	**Transmit Signal Input.** Unfiltered transmit signal input.
19	T(OUT)	Transmit uncommitted op amp output.
20	T+	Transmit uncommitted op amp non-inverting input.
21	T−	Transmit uncommitted op amp inverting input.
22	CLK2	**Digital Clock 2.** TTL/CMOS input clock at 153.6 kHz. If CLK1 is used, CLK2 should be left unconnected.
23	DGND	**Digital Ground.**
24	RX(OUT)	**Receive Signal Output.** This output is capable of driving a 20 kΩ load.

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Functional Description

The MT35212A modem filter implements both the filtering and equalizing functions required in Bell 212A and CCITT V.22 Modems. For CCITT V.22 applications a notch filter is switched in. The MT35212A provides both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included giving full compromise equalization through the transmit and receive filter pair. For the Call Progress Mode provision is made to select the R_X (OUT) smoothing filter. See Call Progress Mode for details

Figure 1 illustrates the functionality of the MT35212A modem filter. Selection between the call progress tone detection mode and the normal data transmission mode is made via Pin 1 (SEL2). For CCITT V.22 applications the notch filter can be programmed to provide rejection at 1800 Hz or 550 Hz via Pin 17 (NSEL). For maximum flexibility the MT35212A may be operated from a 2.4576 MHz, 1.2288 MHz or 3.6864 MHz clock. Refer to Table 2 for clock selection.

CLOCK INPUT	SEL1	CLK1	CLK2
153.6 kHz	Don't care	Open	Input
1.2288 MHz	logic '0'	Input	Open
2.4576 MHz	logic '1'	Input	Open

Table 2 - Input Clock Selection

Two uncommitted operational amplifiers are provided which can be used for gain control or anti-aliasing filters.

Call Progress Mode Operation

A logic '1' on Pin 1 (SEL2) selects this mode. This will insert a divide by six factor in the clock frequency (fc) causing the center frequencies of the filters to shift down to one-sixth of their original values. As a result, the 1200 Hz filter will be centered around 200 Hz and the 2400 Hz filter will be centered around 400 Hz. Refer to figure 2.

With the high group filter centered at 400 Hz, its passband will be approximately 300 Hz to 480 Hz. This allows the response dial tone of 350/440 Hz to pass as well as audible ringing at 440/480 Hz. Half of the busy or reorder tone of 480/620 Hz will also pass through the high group filter in this mode.

By using a suitable detector circuit combined with a method of timing determination it is possible to build a more intelligent modem that can communicate back to its terminal or computer the status of the phone call.

Diagnostic Mode

The MT35212A has Analog Loopback capability. A logic '0' on $\overline{AL}$ pin switches the transmit carrier output back through the receive smoothing filter for testing. For normal operation the $\overline{AL}$ pin should be connected to a High voltage level (i.e. 5V).

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NOTES:

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Features

- Single chip 300 bps full duplex asynchronous FSK modem
- Bell 103/113 and CCITT V.21 selectable
- Auto answer/originate operating modes
- Manual mode
- Phase continuous transmit carrier switching
- Digital and analog loopback modes
- CCITT V.25 tone generation
- UART clock output
- Passthru mode for protocol independence
- No external filtering required
- DTE interface: Functionally: RS-232C Compatible (CCITT V.24) Electrically: TTL level Compatible

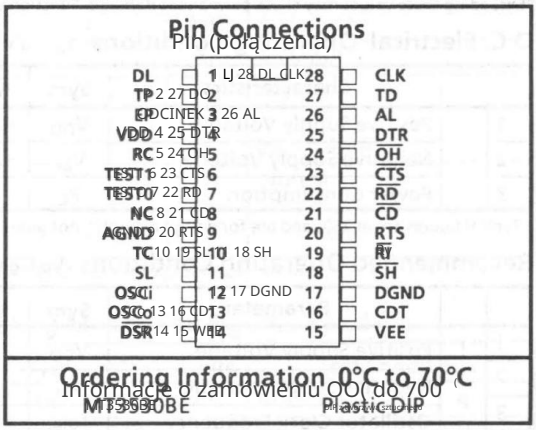
Applications

- Stand alone RS-232C interface modem
- Add on modem for personal computers and microprocessor systems

Description

The MT3530 is an ISO²-CMOS single chip full duplex FSK modem. It is intended for use in Bell 103/113 and CCITT V.21 type applications. The MT3530 features on chip transmit and receive filters; automatic originate mode selection; RS-232C control interface; digital and analog loopback test modes; and generation of both 1.8 kHz UART clock and V.25 answer tone. The device uses a 3.579545 MHz NTSC color TV crystal.

Pin Connections



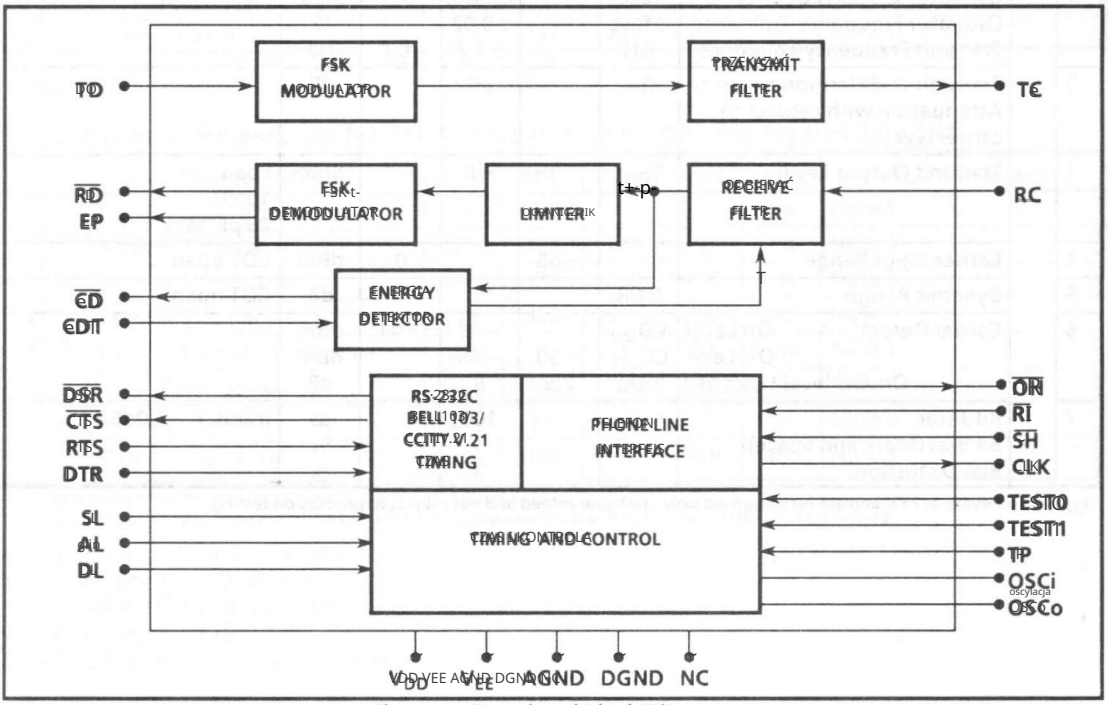


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{DD} to V_{EE}		+12.0	V
2	Storage Temperature Range	T_{STG}	-65	+150	°C
3	Input Voltage, All Pins	V_{IN}	V_{EE} - 0.3	V_{DD} + 0.3	V

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

D.C. Electrical Operating Conditions - T_O = 0°C to + 70°C.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive Supply Voltage	V_{DD}	+4.75	+5.0	+5.25	V	DGND = 0 Volt, AGND = 0 Volt
2	Negative Supply Voltage	V_{EE}	-4.75	-5.0	-5.25	V	DGND = 0 Volt, AGND = 0 Volt
3	Power Consumption	P_C		110	200	mW	V_{DD} = +5.0 V; V_{EE} = -5.0 V

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Recommended Operating Conditions - Voltages are referenced to ground unless otherwise noted.

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	Positive Supply Voltage	V_{DD}		+5		V	DGND = 0 Volt, AGND = 0 Volt
2		Negative Supply Voltage	V_{EE}		-5		V	DGND = 0 Volt, AGND = 0 Volt
3		Oscillator Clock Frequency	fosc		3.579545		MHz	
4		Oscillator Frequency Tolerance	Δfosc		±0.02		%	
5		Operating Temperature Range	T_O	0		70	°C	

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Analog Signal Parameters - 0°C ≤ T_O ≤ 70°C, V_{DD} = 5 Vdc, V_{EE} = -5 Vdc, fosc = 3.579545 MHz.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Oscillator Clock Frequency	fosc		3.579545		MHz	
	Oscillator Frequency Tolerance	Δfosc		±0.02		%	
	Transmit Frequency Tolerance	Δft		±1.2	±3	Hz	
2	Transmit 2nd Harmonic Distortion	T_{HD}		50		dB	
	Attenuation with respect to carrier level						
3	Transmit Output Level	T_{OUT}	-9	-8	-7	dBm	Programmed for 0 dBm; Load = 10 kΩ, 25 pF Max.
4	Carrier Input Range		-50		0	dBm	CDT open
5	Dynamic Range	DNR		50		dB	CDT open
6	Carrier Detect: On Level	CD_{ON}	-43	-43	-41	dBm	
	Off Level	CD_{OFF}	-50	-48		dBm	
	On/Off Level Hysteresis	CD_H	2.5	5		dB	
7	Bit Jitter			100		μs	Input = -30dBm
	Bit Bias (Mark and Space)			1		%	
	Bias Distortion			3		%	

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

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DC Electrical Characteristics

Charakterystyka elektryczna prądu stałego V_{DD} = 5 V ± 5% Vdc, V_{EE} = -5 V ± 5% Vdc, V_{DD} = 5 ± 5% Vdc, AGND = DGND = 0V, T_O = 0°C to 70°C.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	CMOS Inputs Wejścia CMOS — Voltage High Wysokie napięcie VIH	V_{IH}	3			V Uwaga 1	Note 1
		Voltage Low Niskie napięcie VIL	V_{IL}			3	V	
2		TTL Inputs 2 wejścia TTL — Voltage High Wysokie napięcie VIH	V_{IH}	2			V Uwaga 2	Note 2
		Voltage Low Niskie napięcie VIL	V_{IL}			0.8	V	
3		Input Resistance Rezystancja wejściowa	R_{IN}	8			MΩ	All Inputs
4		Input Capacitance Pojemność wejściowa	C_{IN}			15	pF	All Inputs
1	OUTPUTS	LSTTL Outputs Wyjścia LSTTL — Voltage High Napięcie Wysokie VOH 2.4 Napięcie	V_{OH}	2.4			V Uwaga 3	Note 3
		Voltage Low Niskie VOL	V_{OL}			0.4	V	I_{OL} = 0.4mA
2		TTL Output Wyjście TTL — Voltage High Wysokie napięcie VOH 2.4 Niskie	V_{OH}	2.4			V Uwaga 4	Note 4
		Voltage Low napięcie VOL	V_{OL}			0.4	V	I_{OL} = 1.6mA

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
[Typowe wartości liczbowe podano na poziomie 25°C i mają one wyłącznie charakter projektowy i nie są gwarantowane i nie podlegają testom produkcyjnym]

Modem Timing Parameters for CCITT V.21 Operating Mode. See Figures 2 and 4a.

Parametry modemu dla trybu pracy CCITT V.21 Operating Mode. Patrz rysunki 2 i 4a.

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ORIG	Answer Detect Odpowiedź wykryj	t_{AD}	3.2	4.0	5.4	ms Uwaga 5	Note 5
2		Receive Carrier Low Odbiór nośnej niska	t_{RCL}	172	205	236	ms Uwaga 5	Note 5
3		Transmit Carrier Nośnik transmisji	t_{TXC} 592	592	632	688	ms Uwaga 5	Note 5
4		Receive Carrier to $\overline{CD}$ Delay Opóźnienie nośnej odbioru a G względem CD	t_{RCD} 20	20	50	80	ms Uwaga 5	Note 5
5		$\overline{CD}$ to Off-Hook Delay Opóźnienie dzwonka CD do podniesienia słuchawki	t_{COH} 180	180	200	232	ms Uwaga 5	Note 5
1	ANS	Billing Delay Opóźnienie w rozliczeniu	t_{BD}	2.0	2.1	2.3	s Uwaga 5	Note 5
2		Answer Tone Odpowiedź	t_{AT}		3.4		s Uwaga 5	Note 5
3		Transmit Carrier Delay Opóźnienie nośnej transmisji	t_{TCD}		80		ms Uwaga 5	Note 5
4		Clear To Send Gotowy do wysłania	t_{CTS}	32	450	564	ms Uwaga 5	Note 5

‡ Timing is over recommended temperature & power supply voltages.
Przebiegi czasowe: Zalecane wartości temperatury i napięcia zasilania.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Typowe wartości liczbowe podano na poziomie 25°C i mają one wyłącznie charakter projektowy i nie są gwarantowane i nie podlegają testom produkcyjnym.

Modem Timing Parameters for Bell 103 Operating Mode. See Figures 3 and 4a.

Parametry modemu dla trybu pracy Bell 103 Operating Mode. Patrz rysunki 3 i 4a.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ORIG	Receive Dial Tone Odbiór sygnału wybierania	t_{DT}	70			ms Uwaga 5	Note 5
2		Answer Tone Detect Wykrywanie tonu odpowiedzi	t_{ATD}	100	120	200	ms Uwaga 5	Note 5
3		Receive Carrier Low Odbiór nośnej niskiej	t_{RCL}	172	200	236	ms Uwaga 5	Note 5
4		Transmit Carrier Nośnik nadawczy	t_{TXC} 592	592	632	688	ms Uwaga 5	Note 5
5		Receive Carrier to $\overline{CD}$ Delay Opóźnienie odbioru nośnika CD	t_{RCD}	10	20	32	ms Uwaga 5	Note 5
6		$\overline{CD}$ to Off-Hook Delay Opóźnienie dzwonka CD do podniesienia słuchawki	t_{COH} 180	180	200	232	ms Uwaga 5	Note 5
1	ANS	Billing Delay Opóźnienie w rozliczeniu	t_{BD}	2.0	2.1	2.2	s Uwaga 5	Note 5
2		Clear To Send Low Gotowy do wysłania niski	t_{CTS}	100	120	200	ms Uwaga 5	Note 5

‡ Timing is over recommended temperature & power supply voltages
Przebiegi przekazu zalecane wartości temperatury i napięcia zasilania
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Typowe wartości liczbowe podano na poziomie 25°C i mają one wyłącznie charakter projektowy i nie są gwarantowane i nie podlegają testom produkcyjnym.

Note 1. Include $\overline{SH}$, $\overline{RL}$, TEST0 , TEST1
Uwaga 1. Uwzględnij SH, RL, TEST0, TEST1
Note 2. Include $\overline{RTS}$, TD, $\overline{DTR}$, AL, DL, SL
Uwaga 2. Uwzględnij RTS, TD, DTR, AL, DL, SL
Note 3. Include $\overline{OH}$, $\overline{CLK}$, $\overline{CD}$, DSR
Uwaga 3. Uwzględnij OH, CLK, CD, DSR
Note 4. Include $\overline{RD}$, $\overline{CTS}$
Uwaga 4. Uwzględnij RD, CTS
Note 5 Test conducted using Passthru mode
Uwaga 5. Testy przeprowadzone w trybie Passthru

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Modem Timing Parameters for Bell 103 CCITT V.21. See Figures 2, 3, 4b & 5.

Parametry synchronizacji modemów dla Bell 103/CCITT V.21. Zobacz rysunki 2, 3, 4b & 5.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	ORIG	Data Terminal Low	t_{DTL}	15			ms	Note 5
2	ORIG	Request to Send On Delay	t_{RTS}	1			ms	Note 5
3	ORIG	Switch Hook Low	t_{SHL}	54			ms	
1	ANS	Ring Indicator to $\overline{OH}$ Delay	t_{RIO}		80		ms	Note 5
2	ANS	Data Terminal Low to $\overline{OH}$ Delay	t_{TOH}		10		ms	Note 5
3	ANS	Switch Hook to Off Hook Delay	t_{SOH}		40		ms	Note 5
4	ANS	Ring Indicator Low	t_{RIL}	107			ms	

† Timing is over recommended temperature & power supply voltages.

*Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

Note 5: Test conducted using Passthru Mode.

Pin Name	Pin No.	Input	Output	Voltage Level Low	Voltage Level High	Logic Family	I_{OL} mA
$\overline{SH}$	18	X		−3	+3	CMOS	
$\overline{RI}$	19	X		−3	+3	CMOS	
TEST0	7	X		−3	+3	CMOS	
TEST1	6	X		−3	+3	CMOS	
$\overline{OH}$	24		X	+0.4	+2.4	LSTTL	0.4
CLK	28		X	+0.4	+2.4	LSTTL	0.4
$\overline{CD}$	21		X	+0.4	+2.4	LSTTL	0.4
$\overline{RD}$	22		X	+0.4	+2.4	TTL	1.6
$\overline{CTS}$	23		X	+0.4	+2.4	TTL	1.6
$\overline{DSR}$	14		X	+0.4	+2.4	LSTTL	0.4
RTS	20	X		+0.8	+2.0	TTL	
TD	27	X		+0.8	+2.0	TTL	
DTR	25	X		+0.8	+2.0	TTL	
AL	26	X		+0.8	+2.0	TTL	
DL	1	X		+0.8	+2.0	TTL	
SL	11	X		+0.8	+2.0	TTL	

Table 1 - Signal Input and Output Compatibility

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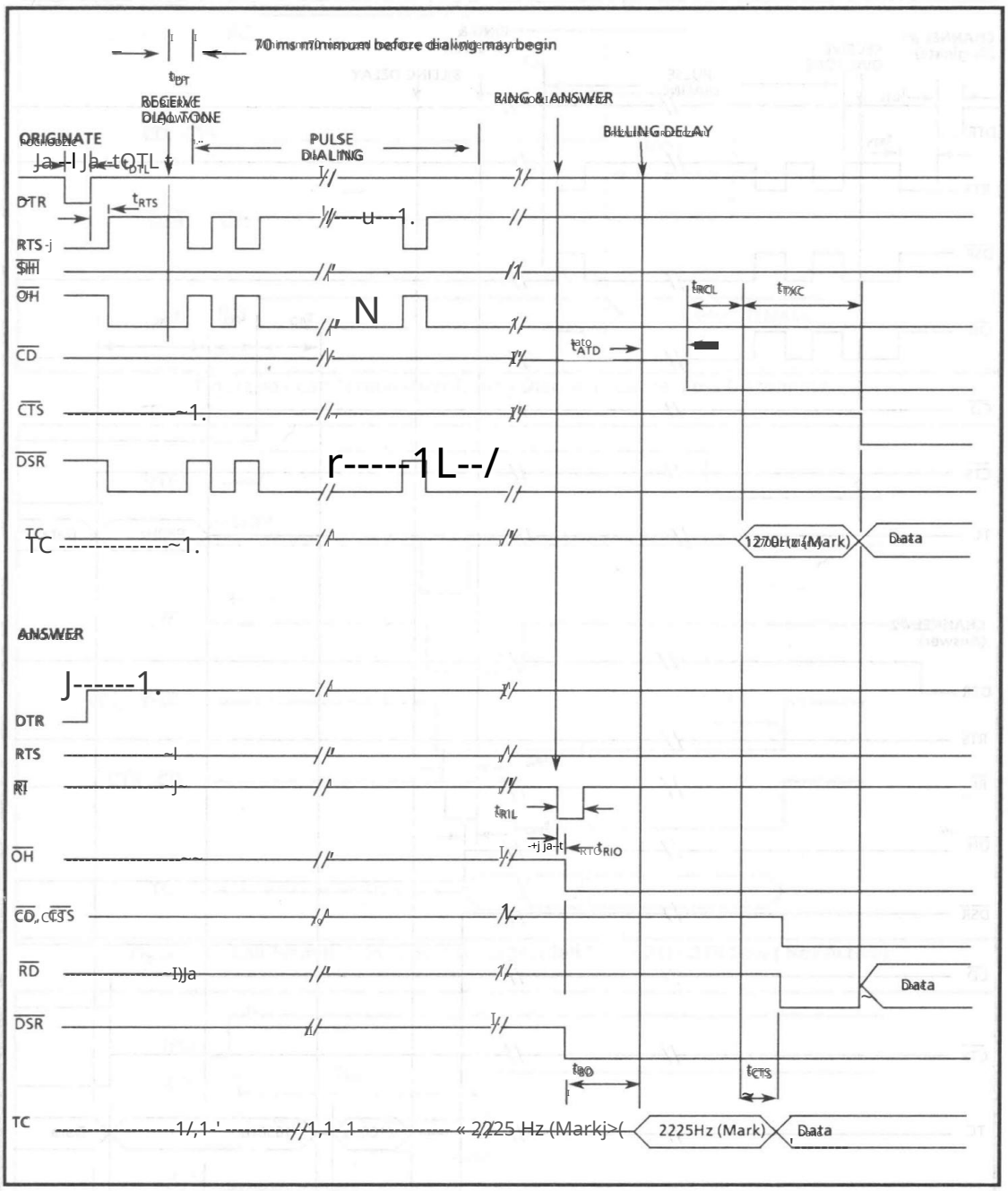

Figure 2 – MT3530 Modem Timing Chart for Bell 103 Operating Mode

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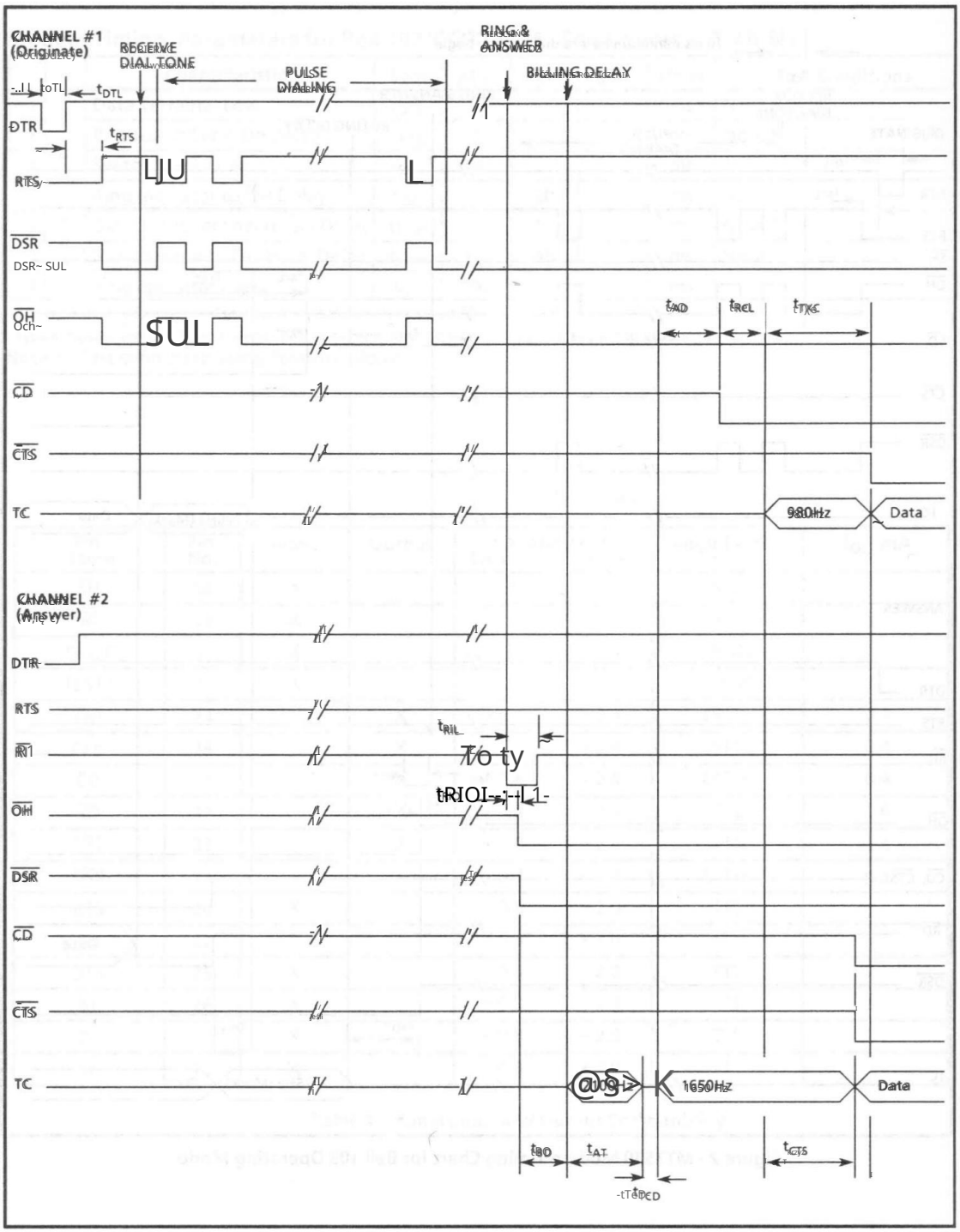

Figure 3. MT3530 Modem Timing Chart CCITT V.21 Operating Mode

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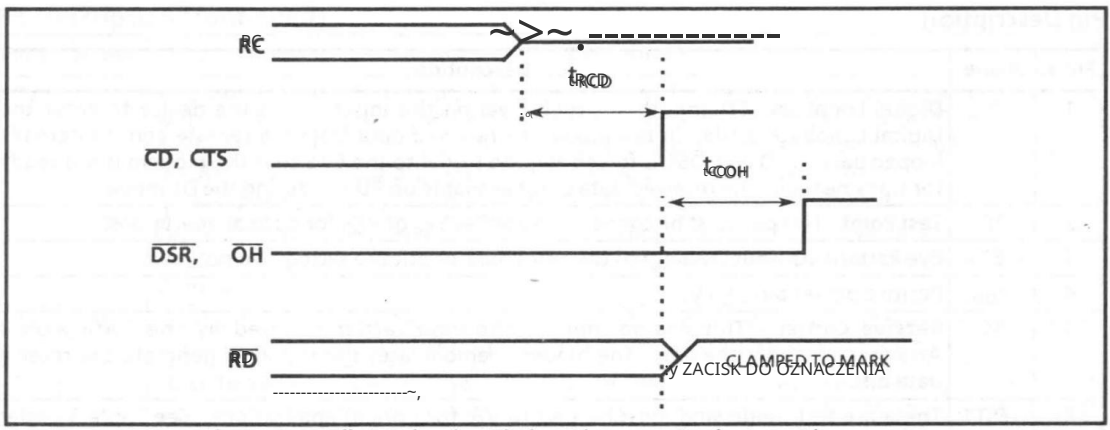

Figure 4a - Call Termination Timing Diagram - Carrier Loss Disconnect

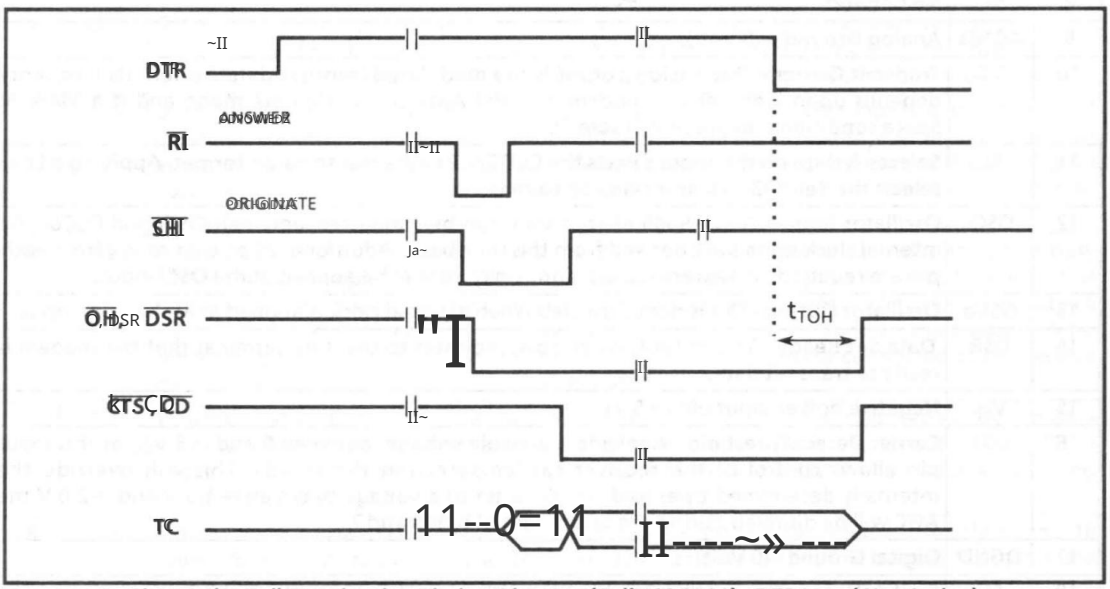

Figure 4b - Call Termination Timing Diagram (Bell 103/V.21) - DTR Low (Not Active)

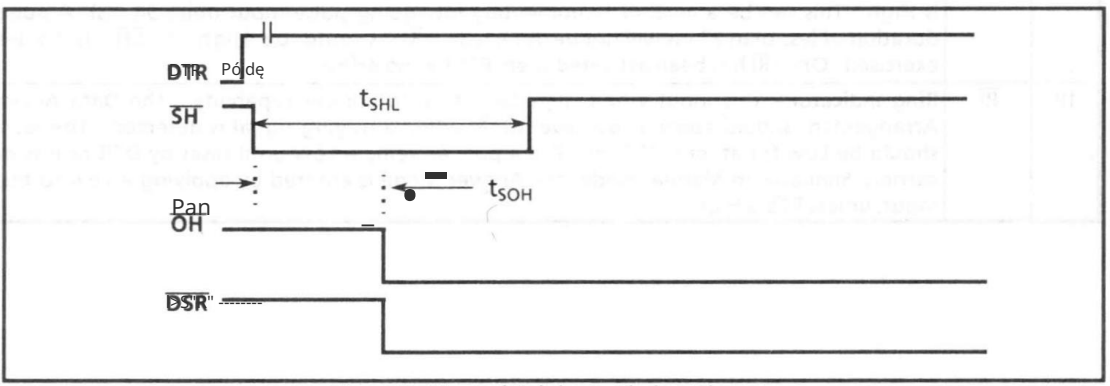

Figure 5 – Manual Originate Timing Diagram

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Pin Description

Opis pinów

Pin # / Nr	Name / Nazwa	Description / Opis
1	DL	**Digital Loopback** (TTL Input) – A High level on this input causes the device to enter the Digital Loopback mode. In this mode, the received data from the remote end is internally looped back to TD and $\overline{DSR}$ is forced High to signal to the DTE that the modem is not ready for transmission. The received data is not available on $\overline{RD}$ pin during the DL mode. Digital Loopback (wejście TTL) – Wysoki poziom na tym wejściu powoduje, że urządzenie przechodzi w tryb Digital Loopback. W tym trybie odebrane dane z zdalnego końca są wewnętrznie zapętlane z powrotem do TD, a DSR jest wymuszany do stanu wysokiego, aby zasygnalizować, że modem nie jest gotowy do transmisji. Odebrane dane są dostępne na pinie $\overline{RD}$ w trybie DL.
2	TP	**Test Point** – Test pin must be connected to either V_{EE} or V_{DD} for normal operations. Punkt testowy – pin testowy musi być podłączony do V_{EE} lub V_{DD}, aby zapewnić normalną pracę.
3	EP	**Eye Pattern** – Output (analog) of the demodulator prior to slicing. Do not load. Eye Pattern - Wyjście (analogowe) demodulatora przed krojeniem. Nie ładuj.
4	V_{DD}	**Positive power pin** (+5 V). Dodatni pin zasilania (+5 V).
5	RC	**Receive Carrier** – This analog input is the data carrier received by the Data Access Arrangement from the line. The modem demodulates this signal to generate the receive data bits. Odbierz wcześniej - To wejście analogowe jest nośnikiem danych odebranym przez Data Access Arrangement z linii. Modem demoduluje ten sygnał, aby wygenerować bity danych odbiorczych.
6 7	TEST1 TEST0	**Test** – These are test inputs and must be tied to V_{EE} for normal applications. See Table 3 under Passthru mode. Testy - są to wejścia testowe i muszą być powiązane z VEE dla normalnych aplikacji. Zobacz tabelę 3 w trybie Passthru.
8	NC	**No Connect** Brak podłączenia.
9	AGND	**Analog Ground** – (0 Volt). Masa analogowa – (0 Volt).
10	TC	**Transmit Carrier** – This analog output is the modulated transmit data carrier. Its frequency depends upon whether the modem is in the Answer or Originate mode and if a Mark or Space condition is being sent (Table 2). Transmit Carrier - To wyjście analogowe jest modulowaną nośną danych transmisyjnych. Jego częstotliwość zależy od tego, czy modem jest w trybie Answer lub Originate oraz czy wysyłany jest warunek Mark lub Space (Tabela 2).
11	SL	**Select** – A High on this input selects the CCITT V.21 data transmission format. Applying a Low selects the Bell 103 data transmission format. Select - A High na tym wejściu wybiera format transmisji danych CCITT V.21. Zastosowanie Low wybiera format transmisji danych Bell 103.
12	OSCi	**Oscillator Input** – A 3.579545 MHz crystal can be connected between OSCi and OSCo. All internal clock signals are derived from this time base. Additional 20 pF caps to V_{EE} from each pin are required. An external clock signal may instead be applied at the OSCi input. Wejście oscylatora - Kryształ 3,579545 MHz można podłączyć między OSCi i OSCo. Wszystkie wewnętrzne sygnały zegara są uzyskiwane z tej bazy czasowej. Wymagane są dodatkowe 20 pF kondensatorów do V_{EE} z każdego pinu. Zamiast tego można zastosować zewnętrzny sygnał zegara na wejściu OSCi.
13	OSCo	**Oscillator Output** – This is not connected when external clock is applied at at the OSCi input. Wyjście oscylatora – nie jest podłączone, gdy do wejścia OSCi zostanie przyłożony zegar zewnętrzny.
14	$\overline{DSR}$	**Data Set Ready** – This output, when Low, indicates to the data terminal that the modem is ready to transmit data. Zestaw danych gotowy - jeśli ten sygnał wyjściowy jest niski, informuje terminal danych, że modem jest gotowy do przesyłania danych.
15	V_{EE}	**Negative power input pin** (−5 V). Ujemny pin wejściowy zasilania (−5 V).
16	CDT	**Carrier Detect Threshold** – Applying a variable voltage between 0 and −5 V at this input pin allows control of the receiver carrier detection threshold. This will override the internally determined threshold. If CDT is set to a voltage between +1.5 V and +2.0 V the AGC will be disabled during the test modes of pins 6 and 7. Wcześniejszy próg wykrywania - Przyłożenie zmiennego napięcia między 0 i −5 V do tego pinu wejściowego umożliwia kontrolę wykrywania nośnej odbiornika. To spowoduje zastąpienie wewnętrznie ustalonego progu. Jeśli CDT jest ustawione na napięcie między +1,5 V i +2,0 V, AGC zostanie wyłączone podczas trybów testowych pinów 6 i 7.
17	DGND	**Digital Ground** - (0 Volt). 17 DGND Masa cyfrowa (0 Volt).
18	$\overline{SH}$	**Switch Hook** – This input is used to manually place the device in the Originate mode. The device will make the $\overline{OH}$ output Low and start the Originate sequence if $\overline{SH}$ is Low and DTR is High. This can be a level or a momentary low going pulse input (min. 54 ms). A pulse duration of less than 27 ms will not be detected. $\overline{RI}$ should be High if $\overline{SH}$ is to be exercised. Once $\overline{RI}$ has been activated then RTS has no effect. SH Switch-hook - To wejście służy do ręcznego umieszczania urządzenia w trybie Originate. Urządzenie ustawi wyjście $\overline{OH}$ na Low i rozpocznie sekwencję Originate, jeśli $\overline{SH}$ to będzie Low, a DTR będzie High. może to być poziom lub chwilowe zaniki wejście impulsowe (min. 54 ms). Impuls RI powinien być High, jeśli SH ma trwać krócej niż 27 ms, nie zostanie wykryty. Ćwiczony. Po ekg ważne $\overline{SH}$, RTS nie ma żadnego efektu.
19	$\overline{RI}$	**Ring Indicator** – This input when High permits auto answer capability. The Data Access Arrangement should apply a Low level to $\overline{RI}$ when a ringing signal is detected. The level should be Low for at least 107 ms. The input can remain Low until reset by DTR or loss of carrier. Similarly, in Manual mode, the Answer Mode is entered by applying a Low to this input, unless RTS is High. Ring Indicator - To wejście, gdy High, umożliwia automatyczną odpowiedź. Data Access Arrangement powinno zastosować poziom Low do RI, gdy zostanie wykryty sygnał dzwonienia. Poziom powinien być niski przez co najmniej 107 ms. Wejście może pozostać Low do momentu zresetowania przez DTR lub utraty nośnej. Podobnie, w trybie Manual, Answer Mode jest wprowadzany przez zastosowanie Low do tego wejścia, chyba że RTS jest High.

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Pin Description (continued)

Pin #	Name	Description
20	RTS	**Request To Send** - This controls data transmission from the modulator. A High on this input with the DTR input High (in the On condition) causes the device to enter the Originate mode. $\overline{OH}$ will go Low to seize the phone line. Auto dialing can be performed by toggling the RTS input High and Low to effect dial pulsing. This input must remain High for the duration of data transmission. (Auto and manual answer will not function if RTS is High.)
21	$\overline{CD}$	**Carrier Detect** - The output goes Low (On) to indicate that the receive data carrier has been received. It goes High (Off) if the received data carrier falls below the carrier detection threshold.
22	RD	**Received Data** - The device presents data bits demodulated from the received data carrier at this output. This output is forced High if DTR is Low or Carrier Detect is High (Off).
23	$\overline{CTS}$	**Clear To Send** - This output goes Low at the completion of the handshaking sequence and goes High when the modem disconnects. It is always High if the device is in the Digital Loopback mode. Data to be transmitted should not be applied at the TD input until this output goes Low (active).
24	$\overline{OH}$	**Off-Hook** - This output goes Low when either the RTS or $\overline{SH}$ input is active in the Originate mode and when a valid ring signal is detected on the $\overline{RI}$ input in the Answer mode. This output is High if DTR is Low or if the disconnect sequence has been completed.
25	DTR	**Data Terminal Ready** - A High on this input enables all the other inputs and outputs and must be present before the device will enter the data mode either manually or automatically. The device will enter an irreversible disconnect sequence if the input goes Low for more than 14 ms during a data call. A pulse duration of less than 6 ms will not be detected.
26	AL	**Analog Loopback** - This input allows the data terminal to make the telephone line busy (Off-Hook) and implement the Analog Loopback mode. A High at this input while DTR is High causes the device to make the $\overline{OH}$ output Low and to enter the Analog Loopback mode. The receive filter center frequency is switched to correspond to the transmit filter center frequency and the transmit data carrier output is internally connected to the receive data carrier input, as well as being available at TC.
27	TD	**Transmit Data** - Data bits to be transmitted are presented to this input serially by the data terminal. A High is considered a binary '1' or Mark, and a Low is a binary '0' or Space. The data terminal should hold this input in the Mark state when data is not being transmitted. During handshaking this input is ignored.
28	CLK	**Clock** - A 4.8 kHz TTL compatible square wave output is available to provide the 16 times clock signal required by a UART for 300 bps data rate. This output facilitates the integration of the modem function in the data terminal.

5

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Introduction

The MT3530 is a low speed full duplex modem designed for use in stand alone modem applications and applications in which the modem function is designed directly into the Data Terminal Equipment (DTE). The MT3530 contains on-chip FSK modulator and demodulator, transmit and receive filters and a supervisory control section. The modem can be used in many different modes. These include Answer/Originate modes, automatic/manual answer, automatic abort, automatic disconnect and Passthru.

Functional Description

Figure 1 illustrates the functionality of the MT3530 modem. The modulator section converts input serial digital data into a square wave at the frequency corresponding to the Mark/Space being sent. The transmit filter outputs a Frequency Shift Keying signal at the TC (Transmit Carrier) output. The frequency of the FSK signal corresponds to the fundamental frequency of the square wave at the input to the filter. The incoming analog signal from the telephone network is bandlimited (filtered) and limited (amplified/clipped) prior to the demodulator carrier input to remove adjacent channel interference and system noise. The output at the receive data pin is a digital logic "1" or "0". The supervisory control and timing section contains the necessary logic to provide initial inter-modem handshaking as well as operational protocol, such as automatic Answer, Originate only and automatic disconnect. Two diagnostic modes, analog and Digital Loopbacks, allow for system tests. In addition, a Passthru mode is available whereby the protocol handshake is disabled. The modem I.C. may be operated in Bell 103/113 or CCITT V.21 type applications. The select (SL) pin defines the operating mode. See Table 2.

Operation of MT3530 Modem Chip

A. Bell 103/113

Answer Mode

In the answer mode the MT3530 is idle waiting for an incoming call. As long as DTR is High, when a Low from the ring detector is presented to $\overline{RI}$ the MT3530 sets $\overline{OH}$ and $\overline{DSR}$ Low. This enables the hook-switch relay. This connects the modem to the phoneline in the Answer mode. The MT3530 waits 2.0 s (min), then sends carrier at 2225 Hz (Mark) to the originating modem. When the originating modem returns with 1270 Hz (Mark) the carrier detect circuit turns on within 120 ms and sets $\overline{CD}$ and $\overline{CTS}$ Low, indicating the handshaking sequence is completed. Data can now be sent and received.

Originate Mode

In the Originate mode a call is initiated, if DTR is High by applying High to the RTS input in auto mode or pulsing negative pulse Low to $\overline{SH}$ in manual mode. This will cause $\overline{OH}$ to go Low, pulling in the hook-switch relay to connect the telephone line, and putting the MT3530 in the Originate mode.

After a suitable time, or when dial tone is detected, RTS can be pulsed Low/High to provide dial pulses. (N.B. $\overline{OH}$ only follows RTS. The proper timing for dialing numbers must come from the terminal.) The RTS line (and the $\overline{OH}$) will go Low and High pulsing the line with desired digits. When the answering modem comes on line it will wait 2.0 s minimum ("billing delay") and then sends the 2225 Hz Answer Tone. 120 ms later the $\overline{CD}$ output goes Low indicating received carrier. 200 ms later it will respond with 592 ms (min) of 1270 Hz carrier. At the end of that time $\overline{CTS}$ (Clear to Send) will go Low indicating to the terminal that the communications link has been established.

SL (Select)	Mode	Transmit Frequency (Hz)*		Receive Frequency (Hz)*	
		Mark	Space	Mark	Space
0	Bell 103 Originate Bell 103 Answer	1270 2225	1070 2025	2225 1270	2025 1070
1	CCITT V.21 Channel 1 (Originate) CCITT V.21 Channel 2 (Answer) CCITT V.25 Answer Tone	980 1650 2100	1180 1850	1650 980	1850 1180

Table 2 - Bell 103/CCITT V.21 Operating Modes

Space = Binary 0, Mark = Binary 1, Crystal Frequency = 3.579545 MHz, *Frequency drift = ±3 Hz

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Tryb przerwania

W modelu MT3530 dostępna jest funkcja automatycznego przerywania, aby uniknąć wiązania systemu w przypadku wystąpienia trudności w ustanowieniu łącza. Jeśli nie wykryto żadnego nośnika w ciągu 14 sekund od włożenia urządzenia w tryb odpowiedzi lub inicjacji spowoduje przerwanie kalibracji linii Wysokie OH, rozłączenie poprzez ustawienie telefonicznej. DSR również przejdzie w stan wysoki. Ten czas przerwania można wydłużyć poprzez pulsowanie RTS Low Minimum 1 ms przed upływem 14 sekund. Spowoduje to zresetowanie licznika czasu przerwania. Jeśli limit czasu upłynął Aby zresetować DTR, konieczne będzie podanie impulsu wysokiego MT3530. W trybie Abort przechodzi do trybu Originate tryb.

Tryb wyłączenia

Jeżeli odbierana siła nośna spadnie poniżej −50 dBm podczas wymiany danych trwającej dłużej niż 190 ms MT3530 zakończy kalibrację i przejdzie w stan zawieszenia, rozłączając linię telefoniczną. (Zobacz rysunek 4a.)

Obsługa ręczna

Urządzenie MT3530 można obsługiwać zarówno ręcznie, jak i automatycznie. Aby przełączyć go w tryb odpowiedzi, zastosuj ujemny impuls (− 5V) na RI więcej niż 107 ms. Jeśli RI jest powiązane z wartością Low, urządzenie przejdzie do trybu odpowiedzi, gdy DTR jest ustawiony na Wysoki.

Podobnie, aby przełączyć go w tryb Originate, SH może być pociągnięty w stan Low przez ponad 54 ms. Poprzez wiązanie SH Niski, MT3530 przejdzie w tryb Originate zawsze, gdy DTR jest ustawiony na Wysoki.

Tryb Passthru

Za pomocą pinów „TEST0" i „TEST1" MT3530 można przełączyć w tryb Passthru. Zobacz Tabela 3 do konfiguracji. W tym trybie modem stoi bezczynny w trybie Originate i transmisji i funkcje odbioru stają się niezależne od siebie inny. W tym trybie czas i uzgadnianie Protokół może zostać zawieszony w zależności od statusu DTR.

Przy ustawieniu DTR na niski, transmisja i odbiór funkcje stają się niezależne od czasu i protokół uściśnięcia dłoni. Wszystkie zdarzenia na Switch-Wejście Hook, Ring Indicator i Request-To-Send piny są ignorowane.

W przypadku trybu DTR High, Answer lub Originate wybierane w taki sam sposób jak w trybie normalnym. Funkcje nadawania i odbioru są zależne w sprawie protokołu synchronizacji i uzgadniania. Carrier Detect działa jak w trybie normalnym. Auto

TEST0 PIN 7	TEST1 PIN 6	MT3530 STATUS	H = + 5 V (VDD) L = −5V (VEE)
L	L	Normal	
H	L	Passthru	

Tabela 3 – Wejścia sterujące w trybie passthru

Wyłączenie nastąpi, ale automatyczne przerwanie nie jest możliwe. Po zakończeniu kalibracji modem jest umieszczany w tryb początkowy.

B. Tryb CCITT V.21

MT3530 wykona te same operacje opisane powyżej w trybie CCITT V.21, jeśli SL pin jest przywiązany wysoko. Podstawowa zasada jest taka sama, ale częstotliwości i czasy są przełączane na zgodne ze specyfikacją V.21. Zobacz czas Dodatkowe informacje można znaleźć w wykresach (rysunki 3 i 4) oraz tabeli 2 szczegóły. W trybie V.21 dźwięk odpowiedzi V.25 O częstotliwości 2100 Hz zostanie wygenerowany po odebraniu połączenia.

Wymagania dotyczące zegara zewnętrznego

Aby uzyskać zewnętrzny zegar 3,579545 MHz, o poziomie TTL, współczynnik wypełnienia 50%, do pinu można zastosować falę prostokątną 12, OSCI, przez kondensator 0,1 µF.

Tryby diagnostyczne

W urządzeniu MT3530 dostępne są dwa tryby diagnostyczne. operator. Ustawiając pin AL w stan wysoki, podczas gdy DTR jest wysoki, urządzenie wchodzi w tryb pętli analogowej. Tryb OH przechodzi w stan niski, aby zająć linię telefoniczną.

Częstotliwość środkowa filtra odbiorczego przesuwa się do częstotliwość środkowa transmisji i sygnał TC są wewnętrznie podłączony do wejścia RC. Sygnał nadawczy również pozostaje dostępny na pinie TC. Tak więc, każdy cyfrowy dane wejściowe w TD są kodowane i wysyłane przez TC, a w tym samym czasie z powrotem przez wejście analogowe, zdekodowane, i na pinie RD.

Po ustawieniu pinu DL w stan wysoki układ MT3530 wchodzi Tryb cyfrowej pętli zwrotnej. W tym trybie wszelkie dane otrzymane z odległego końca linii telefonicznej jest retransmitowany z powrotem do źródła i wymuszany jest DSR Wysoki. Należy pamiętać, że dane cyfrowe nie są dostępne w wyjście RD w tym trybie. Zobacz tabelę 4.

Test Mode	Status Lines†						
	DTR	RTS	DSR	OH	CTS	CD	RD
AL	H	H	L	L	L	L	L
DL	H	H	H	L	H	H	H

Tabela 4 – Stan sterowania w trybach diagnostycznych
† (L = Niski, H = Wysoki)

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Application

Two typical MT3530 system configurations are illustrated. Figure 6 shows a stand-alone RS-232 interface modem to be used as a peripheral accessory to a communications terminal or computer.

Figure 7 shows an add-on modem for building into a computer and connecting to the internal parallel bus structure. The ACIA or UART does the parallel-to-serial and serial-to-parallel conversion required.

Both configurations are intended for direct connection to the telephone line. This requires meeting FCC Part 68 for network protection.

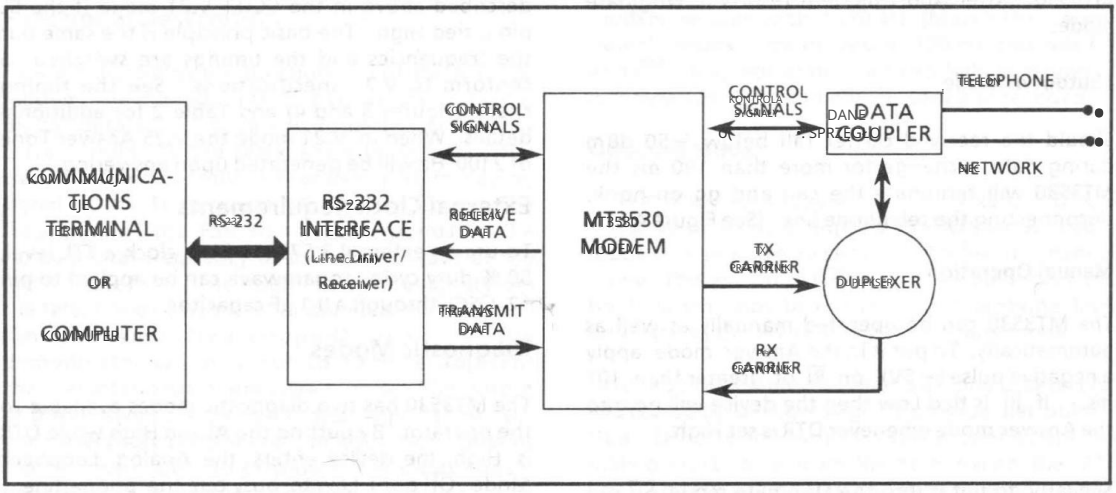

Figure 6 - Serial Interface System Configuration for MT3530

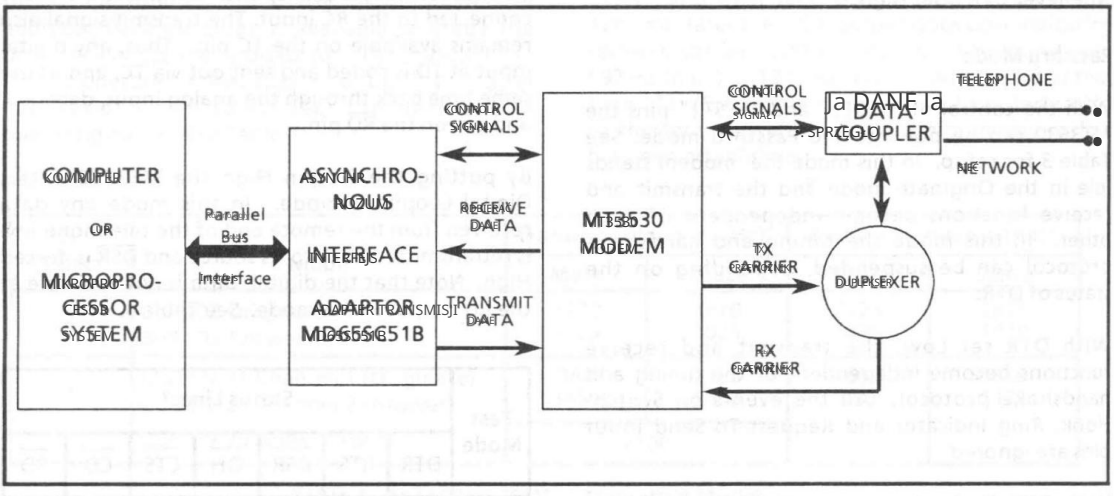

Figure 7 - Parallel Interface System Configuration for MT3530

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916 1002-01 NA ISSUE 4 November 1990

Features

- Performs ASK (amplitude shift keyed) modulation and demodulation
- 32 kHz carrier frequency
- Up to 2 kbit/s full duplex data transfer rate
- On chip oscillator
- On chip tone caller for alerting functions
- Adjustable tone caller frequencies
- Selectable self loop test mode
- 5V (2.5 mA) power supply
- ISO2-CMOS and switched capacitor technologies
- 18 Pin DIP

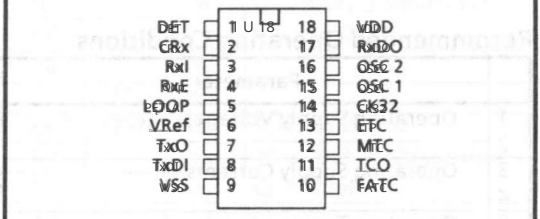
Applications

- Simultaneous data and voice communication in PABXs
- Modem/data set adapter
- "Smart" telephone sets

Description

The MT8840 is a "carrier over voice" voice modem which allows simultaneous transfer of voice and data over a single pair of wires. Data is transferred on an amplitude shift keyed (ASK) 32 kHz carrier. On-chip oscillator circuitry and tone caller functions are provided. The device is fabricated in Mitel's double poly ISO2-CMOS™ technology utilizing switched capacitor techniques.

Pin Connections



Ordering Information 0°C to +85°C

MT8840AE 18 Pin PDIP
MT8840AS 18 Pin SOIC

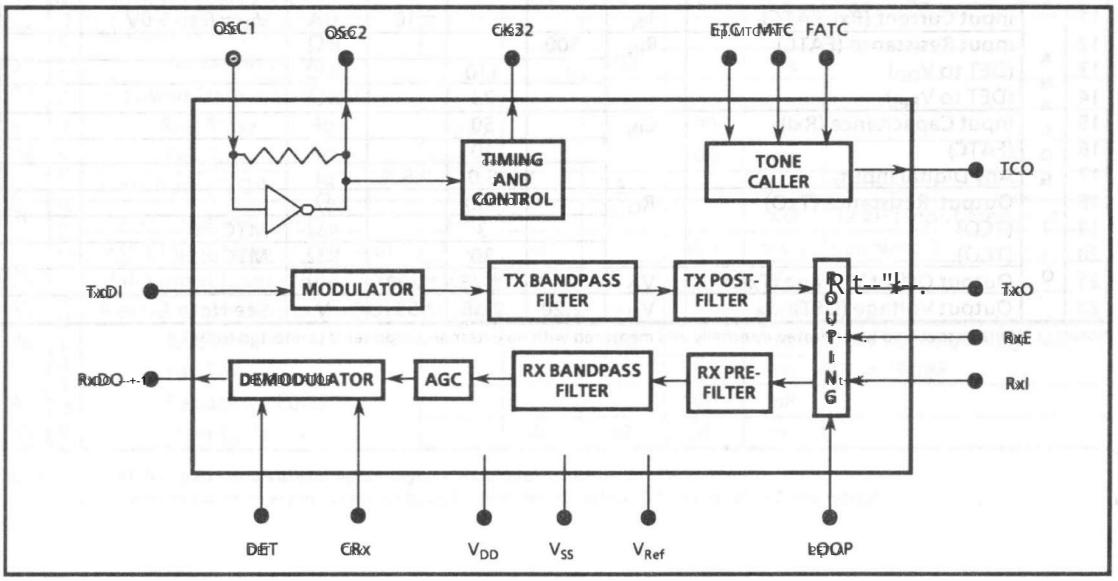


Figure 1 - Functional Block Diagram

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Absolute Maximum Ratings*

Bezwzględne wartości maksymalne

	Parameter	Symbol	Min	Max	Unit
1	Supply Voltage (Napięcie zasilania)	V_{DD}-V_{SS}	-0.3	+7.0	V
2	Voltage On Any Pin (Napięcie na dowolnym pinie)	V_{Max}	V_{SS}-0.3	V_{DD}+0.3	V
3	Current On Any Pin (Prąd na dowolnym pinie)	I_{Max}		20	mA
4	Storage Temperature (Temperatura przechowywania)	T_S	-65	+150	°C
5	Package Power Dissipation (Rozpraszanie mocy pakietu)	P_{Diss}		850	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Działanie funkcjonalne w tych warunkach nie jest zalecane.

Recommended Operating Conditions

Zalecane warunki pracy

	Parameter	Symbol	Min	Typ	Max	Unit
1	Operating Supply Voltages (Napięcie zasilania robocze)	V_{DD}	4.75	5	5.25	V
2		V_{Ref}		$0.4V_{DD}$		V
3	Operating Supply Currents (Prądy robocze zasilania)	I_{DD}		2.5	5.0	mA
4		I_{Ref}			200	µA
5	Operating Temperature (Temperatura robocza)	T_O	0		+85	°C
6	Load Capacitance (TxO) (Pojemność obciążenia (TxO))	C_L			50	pF
7	Load Resistance (TxO) (Rezystancja obciążenia (TxO))	R_L	10			KΩ

D.C. Characteristics

Charakterystyki prądu stałego V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_A = -40 to +85°C (All voltages are referenced to V_{SS} /GND)
(Wszystkie napięcia odniesione do V_{SS} /GND)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
1	DIGITAL	Input Current (Prąd wejściowy)	I_{IN}			±10.0	µA	V_{IN} = 0 to V_{DD}
2		Input Low Voltage (Napięcie wejściowe niskie)	V_{IL}	0		1.5	V	
3		Input High Voltage (Napięcie wejściowe wysokie)	V_{IH}	3.5		5.0	V	
4		Output Low Voltage (Napięcie wyjściowe niskie)	V_{OL}			0.4	V	V_{OL} @ 0.4mA = 0.4mA
5		Output High Voltage (Napięcie wyjściowe wysokie)	V_{OH}	4.6			V	V_{OH} @ 0.4mA = 0.4mA
6		Output Drive Current						
7		N-Channel Source (Except OSC2) (Kanał N (oprócz OSC2))	I_{OL}	0.4			mA	V_{OL} @ 0.4V = 0.4V
8		OSC2		0.1			mA	
9		P-Channel Source (Except OSC2) (Źródło kanału P (oprócz OSC2))	I_{OH}	0.4			mA	V_{OH} @ 4.6V = 4.6V
10		OSC2		0.1			mA	
11	ANALOG (FATC)	Input Current (Rx) (Prąd wejściowy (Rx) FATC)	I_{IN}			±10.0	µA	V_{IN} = 0 to 5.0V
12		Resistance (FATC) (Rezystancja wejściowa (FATC))	R_{IN}	500			KΩ	
13		(DET to V_{DD})			170		KΩ	
14		(DET to V_{Ref})			23		KΩ	
15		Input Capacitance (Rx)	C_{IN}		50		pF	
16		(FATC)			10		pF	
17		Any Digital Input (Dowolne wejście cyfrowe)			5.0	7.5	pF	
18		Output Resistance (TxO) (Rezystancja wyjściowa (TxO))	R_O		100		Ω	
19		(TCO)			3		KΩ	MTC=0
20		(TCO)			30		KΩ	MTC=1
21		Output Offset Voltage (TxO) (Napięcie przesunięcia wyjściowego (TxO))	V_{OS}		±25.0	±200	mV	
22		Dynamic Voltage (DET) (Napięcie dynamiczne (DET))	V_D	2.20	2.36	2.55	V	See Note 1

Notes: 1. Voltage spec is generated internally and measured with no external components connected to DET.
Uwagi: 1. Specyfikacja napięcia jest generowana wewnętrznie i mierzona bez zewnętrznych komponentów podłączonych do DET.

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A.C. Characteristics

A.C. Characteristics - V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T = 0 to 85°C (All voltages are referenced to V_{SS}/GND)

A.C. Characteristics - V_{DD}=5.0V ± 5%, V_{SS}=0V, T=0 do 85°C (Wszystkie napięcia odnoszą się do V_{SS}/GND)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
1	DIGITAL I/O	Crystal/Clock Frequency	f_C	3.5759	3.5795	3.5831	MHz	OSC 1, OSC 2
2		Clock Input (OSC 1)						
3		Rise Time	t_{CLHCI1}			100	ns	10% - 90% of (V_{DD} - V_{SS})
4		Fall Time	t_{CHLCI1}			100	ns	
5		Duty Cycle	DC_{CI1}	40	50	60	%	
6		Clock Output (OSC 2)						
7		Rise Time	t_{CLHCO2}		100		ns	C_L = 30pF, 3.58MHz ext.
8		Fall Time	t_{CHLCO2}		100		ns	C_L = 30pF, 3.58MHz zewn.
9		Duty Cycle	DC_{CO2}		50		%	clock to OSC1
10		Capacitive Load	C_{LCO2}			30	pF	
11		Clock Output (CK32)	f_{CK32}	32508	32541	32574	Hz	fc = 3.5795MHz
12		Rise Time	t_{CLHK32}		100		ns	10% - 90% of (V_{DD} - V_{SS})
13		Fall Time	t_{CHLK32}		100		ns	C_L = 100pF
14		Duty Cycle	DC_{CK32}		50		%	
15		Capacitive Load	C_{LK32}			100	pF	
16	TONE CALLER	Warbler Frequency (TCO)	f_{WT}	7.935	7.945	7.955	Hz	fc = 3.5795MHz ± 0.1%
17		Low Tone Frequency	f_{LT}	352	350	428	Hz	FATC = 0, fc = 3.5795MHz
18				1036	1148	1260	Hz	FATC = V, fc = 3.5795MHz
19		High Tone Frequency	f_{HT}	440	487	535	Hz	FATC = 0, fc = 3.5795MHz
20				1295	1434	1574	Hz	FATC = V, fc = 3.5795MHz
21		Harmonic Relationship	f_{HT}/f_{LT}		1.25			
22		Warbler Output (TCO)						
23		Rise Time	t_{CLHWO}		500		ns	100KΩ load to V_{Ref}
24		Fall Time	t_{CHLWO}		500		ns	C_L = 30pF, MTC = 0
25		Duty Cycle	DC_{WO}		50		%	
26		Output Level (TCO)	V_{TCC}		V_{DD}		V_{pp}	MTC = 0
27					0.625		V_{pp}	MTC = 1 (obciążenie 100kΩ do V_{Ref})
28	MODULATOR	Modulated Frequency	f_{MOD}		32541		Hz	
29		Output Level (TxO)	V_{TXO}	225	250	270	mV_{pp}	V_{DD} - V_{SS} = 5V
30		Output Level (TxO)						
31		variation vs. V_{DD}	V_{TXO}		100		%	
32		Transmit Data Input (TxDI)						
33		Rise Time	t_{LHTXDI}			100	ns	
34		Fall Time	t_{HLTXDI}			100	ns	
35		Data Rate (TxDI)	f_{Data}		2		kbit/s	See Note 1
36	DEMODULATOR	Input Impedance (RxI)	Z_{IN}		50		KΩ	32 kHz Input Frequency
37		Valid Input Level - Data (RxI)	V_{RXI}	40		400	mV_{pp}	See Note 2
38		Valid Input Level - Data + Voice	V_{RXI}			3.0	V_{pp}	
39		Receive Data Output (RxDO)	f_{Data}		2		kbit/s	
40		Rise Time	t_{LHRXDO}		100		ns	10% - 90% of (V_{DD} - V_{SS})
41		Fall Time	t_{HLRXDO}		100		ns	C_L = 100pF
42		Capacitive Load	C_{LRXDO}			100	pF	
43		Duty Cycle	DC_{RXDO}	40	50	60	%	

Notes: 1. All A.C. parameters are based on a typical data rate of 2 kbit/s.
2. Measured with no external resistor to DET input. Detection level internally set to 2.36V typical

Uwagi: 1. Wszystkie parametry AC podane są dla typowej szybkości transmisji danych, 2 kbit/s.
2. Zmierzono bez zewnętrznego rezystora na wejściu DET. Poziom detekcji wewnętrznie ustawiony na 2,36V typowo

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AC Characteristics (Continued)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
44	DEM OD	Inband Noise Rejection (S/N)		12			dB	Input Sig. (RxI) = 400mV$_{pp}$
45		Attenuation to Voice Signals		40			dB	f_{RxI} = 0 - 5KHz
46		Detector Filter Q	Q		38			
47		Detector Center Frequency			32		kHz	

Pin Description

Pin #	Name	Description
1	DET	Demodulator detector level adjust input (Analog). Internal resistive divider applies 2.36V at open circuit condition. Connect external resistor to lower detect level.
2	CRx	External AGC time constant adjust input (Analog). Connect external capacitor to V_{SS}.
3	RxI	Modulated receive signal input (Analog). Biased at V_{Ref}.
4	RxE	Receive enable input (Digital) with internal pull up. Active high.
5	LOOP	Self-test mode select input (Digital) with internal pull down. Active high.
6	V_{Ref}	Internal reference voltage output (Analog).
7	TxO	Modulated transmit carrier output (Analog).
8	TxDI	Transmit data input (Digital).
9	V_{SS}	Negative power supply.
10	FATC	Tone caller center frequency adjust input (Analog).
11	TCO	Tone caller output (Digital).
12	MTC	Mute tone caller input (Digital) with internal pull down. Active high.
13	ETC	Enable tone caller input (Digital) with internal pull down. Active high.
14	CK32	32 kHz data strobe output (Digital).
15	OSC1	Clock input. 3.579545 MHz crystal connected between
16	OSC2	Clock output to drive external devices. these pins completes internal oscillator.
17	RxDO	Receive data output (Digital). Synchronized to CK32.
18	V_{DD}	Positive power supply.

Functional Description

The MT8840 contains a modulator and demodulator circuitry for CCITT 32 kHz ASK signalling as well as a two-tone (tone caller) generator to replace the function of the mechanical telephone ringer.

A 32 kHz carrier is modulated by the digital bit stream applied to input TxDI. This results in an amplitude shift keyed (ASK) 32 kHz carrier. A logical high at TxDI enables the carrier and a logical low disables it. The digitally modulated wave form is shaped by the Tx POST FILTER and smoothed by the Tx POST FILTER. The signal then enters the routing block where it is transferred to the TxO output.

The modulated 32 kHz receive signal is applied to RxI. With a logical low applied to LOOP and a logical high applied to RxE, receive signals are routed to the RxPREFILTER. Switched capacitor filters are used throughout the MT8840 to prevent aliasing in the switched capacitor RxPREFILTER, BANDPASS FILTER. Voice signals are removed by the bandpass filter which is followed by an AGC circuit. This provides a dynamic range of 20dB for the receiver. An external 1µF capacitor connected from CRx to V_{SS} is required to control the AGC attack and decay time constants. Data is recovered from the received signal in the demodulator. The minimum voltage level to which the demodulator responds may be adjusted by connecting a resistor from DET to V_{DD} or V_{Ref}. Since DET is the input to a comparator, noise should be kept to a minimum at this point. The recovered receive data is synchronized to the leading edge of the 32 kHz clock (available at CK32) before appearing at RxDO.

When in loop back mode, the Rx PREFILTER input is internally disconnected from the RxI input pin and connected to TxO. The transmitter output is still available at TxO.

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A two tone warbling audio signal is available at TCO when the tone caller enable input (ETC) is high. TCO is internally clamped to V_{Ref} when the tone caller is disabled. The tone output can be attenuated by 20dB if a logical high is applied to the tone caller mute input (MTC).

Dwutonowy sygnał dźwięk kowy jest dostę pny pod adresem TCO, gdy sygnał wejściowy włączający ton (ETC) jest wysoki. TCO jest wewnę trznie zaciskany do V_{Ref}, gdy ton dzwonią cy jest wyłą czony. Wyjście tonu może być tłumione o 20 dB, jeśli zostanie do niego zastosowany logiczny wysoki poziom wejście wyciszenia tonu dzwoniącego (MTC).

Applications

Figures 2 through 4 show how the MT8840 may be utilized to transfer data and voice simultaneously over a single pair of wires in digital or analog PABXs and "smart" telephone sets. In all three figures a microprocessor sends/receives data to/from the MT8840 via a UART which converts the data format from parallel-to-serial or serial-to-parallel for the transmit and receive directions respectively. In the receive direction the MT8840 has on-board filters to reject voice-band signals leaving only the 32 kHz carrier. This carrier is then demodulated to recover the received data. In the transmit direction the data to be sent is modulated and passed on to a summing circuit which sums the modulated 32 kHz carrier and voiceband signals for transmission over the telephone line. In the PABX the Filter/Codec has filters which reject the 32 kHz carrier from the received composite voice and data signal allowing only voiceband signals to pass through which are then PCM encoded for digital switching. However, in both the analog PABX and smart telephone set, lowpass filters could be included to handlimit the received signal leaving only voice signals to be passed on to the switch array or handset earpiece.

Rysunki od 2 do 4 pokazują, jak może wyglądać MT8840 służy do jednoczesnego przesyłania danych i głosu przez jedną parę przewodów w cyfrowych lub analogowych centralach PABX „inteligentne" telefony. We wszystkich trzech rysunkach mikroprocesor wysyła/odbiera dane do/z MT8840 za pośrednictwem UART, który konwertuje format danych z równoległego na szeregowy lub szeregowo na równoległy przesyłać i odbierać wskazówki.

odpowiednio. W kierunku odbioru MT8840 posiada wbudowane filtry do odrzucania sygnałów pasma głosowego pozostawiając tylko nośną 32 kHz. Ta nośna jest następ nie demodulowana, aby odzyskać otrzymane dane. W kierunku transmisji dane do wysłania są modulowane i przekazany do procesu sumującego, który sumuje modulowane sygnały nośne i pasma głosowego o częstotliwości 32 kHz transmisja przez linię telefoniczną. W PABX filtr/kodek ma filtry, które odrzucają 32 kHz nośną z otrzymanego złożonego głosu i danych sygnał umożliwiający przechodzenie wyłącznie sygnałów pasma głosowego przez które następ nie są kodowane są sygnały PCM w celu uzyskania sygnału cyfrowego przełączanie. Jednak zarówno w analogowym PABX, jak i inteligentny telefon, filtry dolnoprzepustowe mogą być włączone do ograniczenia pasma odebrane wyjście sygnału tylko sygnały głosowe przekazywane do przełącznika zestaw słuchawkowy lub słuchawka.

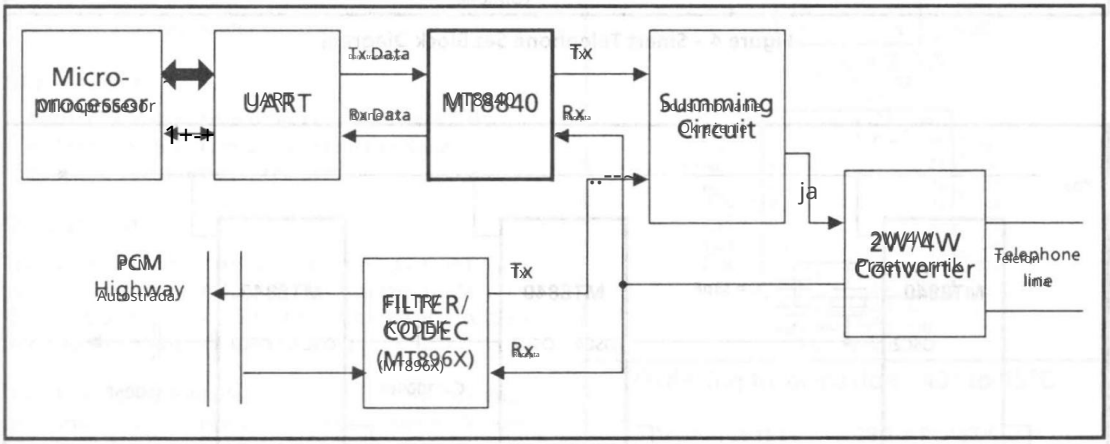

Figure 2 - Digital PABX Block Diagram

Rysunek 2 — Schemat blokowy cyfrowej centrali PABX

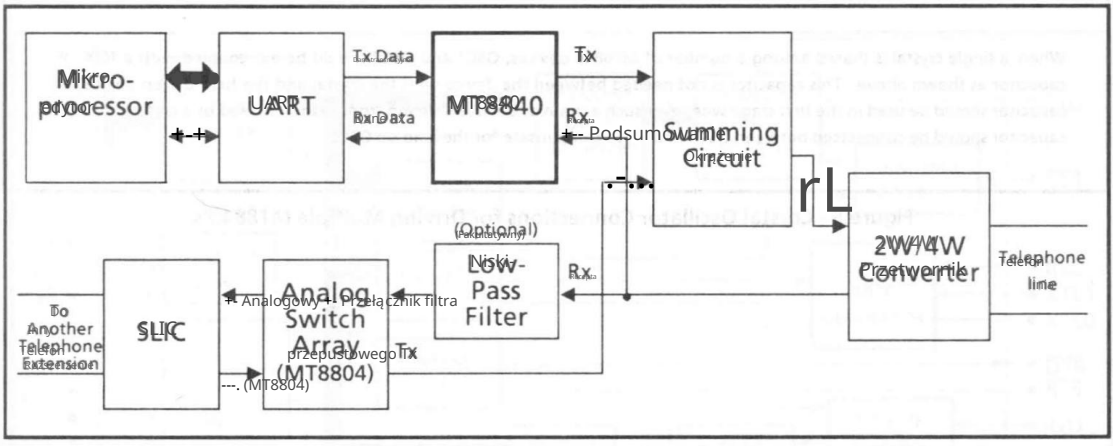

Figure 3 - Analog PABX Block Diagram

Rysunek 3 — Schemat blokowy analogowej centrali PABX

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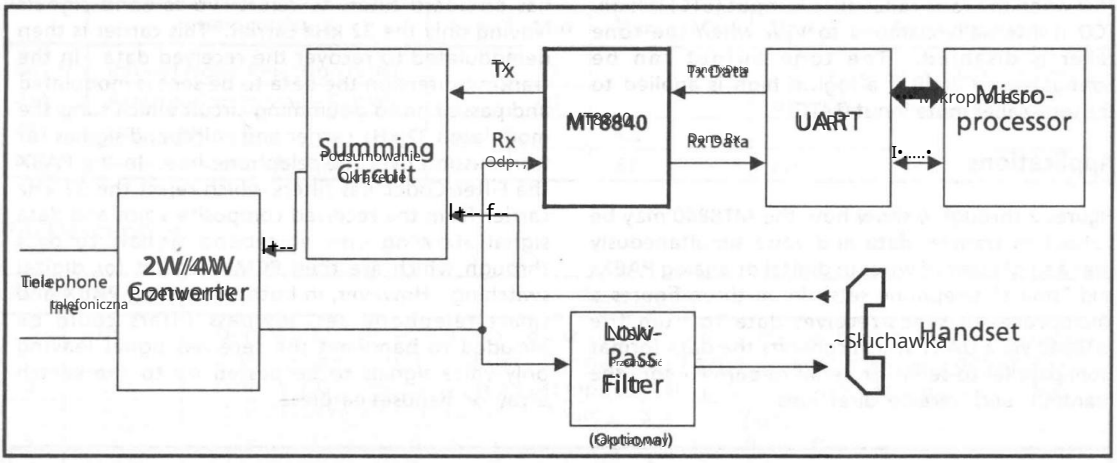
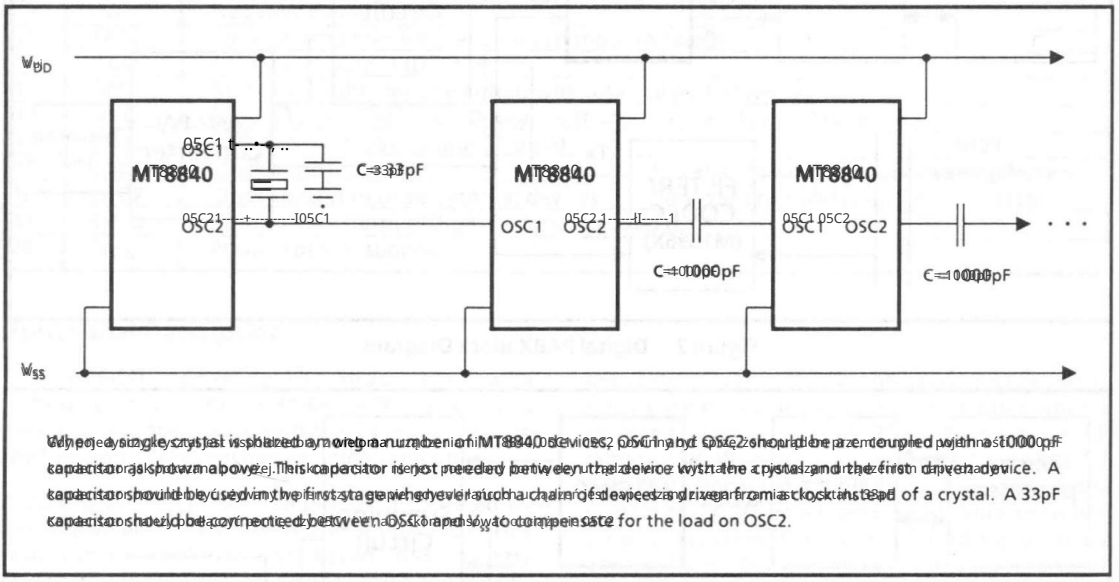


Figure 4 - Smart Telephone Set Block Diagram



When a single crystal is shared among several MT8840 devices, OSC1 and OSC2 should be connected with a 1000pF capacitor as shown above. This capacitor is not needed between the device with the crystal and the first device. A capacitor should be used in the first stage whenever a chain of devices is driven from a clock instead of a crystal. A 33pF capacitor should be connected between OSC1 and V_{SS} to compensate for the load on OSC2.

Figure 5 - Crystal Oscillator Connections for Driving Multiple MT8840's

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MITEL

ISO-CMOS MD65SC51B

Asynchronous Communications Interface Adaptor

916-1002-052NA ISSUE 5 November 1990

Features

- Replacement for existing NMOS part.
- 15 selectable baud rates from 50 bit/s to 19.2 kbit/s or 1/16th of external clock rate.
- Selectable word length & number of stop bits.
- Selectable echo mode.
- Full or half duplex operation.
- Data set/modem control functions.
- Parity generation and checking.
- Low power ISO-CMOS technology.
- TTL compatible.
- Single 3-6 volt power supply.

Applications

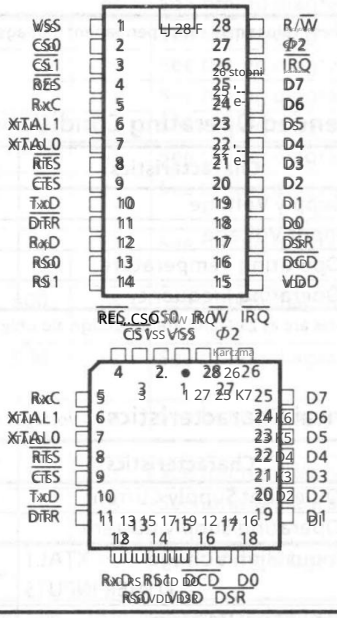
- Microprocessor to modem bidirectional link.
- Microprocessor (µP) serial data interface.
- Serial input/output interface.

Description

The MD65SC51B is an Asynchronous Communications Interface Adaptor fabricated in Mitel's ISO-CMOS technology. The device provides interfacing between a µP and a modem.

The MD65SC51B will also control all of the interrupt handling between the µP and the modem. A programmable baud rate generator is available to derive one of 15 selectable baud rates or 1/16th of an external clock rate.

Pin Connections



Ordering Information -40° to 85°C

MD65SC51BE	28 Pin Plastic DIP
MD65SC51BP	28 Pin PLCC

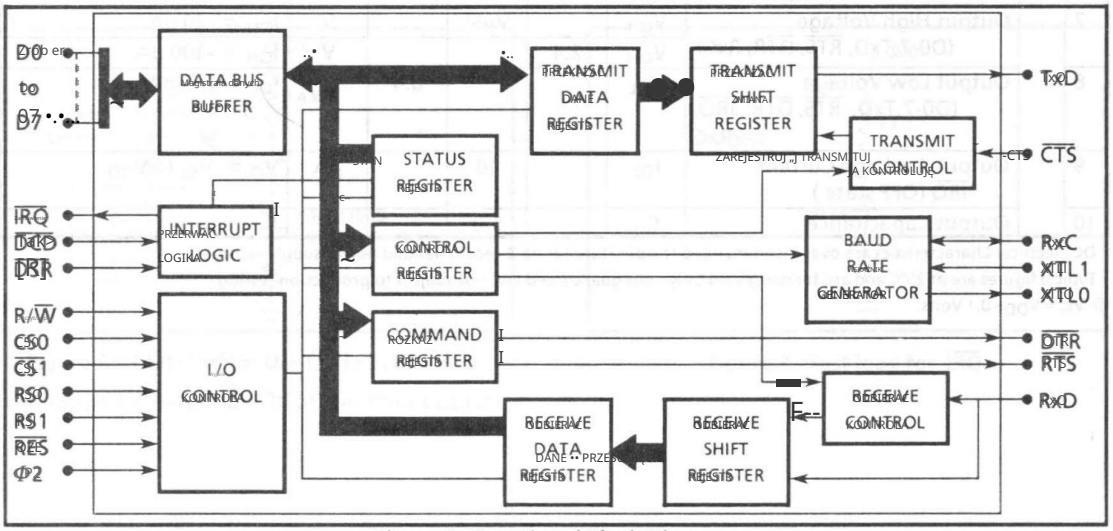


Figure 1. Functional Block Diagram

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Absolute Maximum Ratings*

Maksymalne wartości bezwzględne*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage (Napięcie zasilania)	V_{DD}	-0.3	7.0	V
2	Voltage on any I/O pin (Napięcie na dowolnym pinie I/O)	V_I	V_{SS} -0.3	V_{DD} +0.3	V
3	Current on any I/O pin (Prąd na dowolnym pinie I/O)	I_I		±10	mA
4	Storage Temperature (Temperatura przechowywania)	T_{SS}	-65	+150	°C
5	Power Dissipation (Rozpraszanie mocy) Plastic (Plastik)	P_D		0.6	W
	Ceramic (Ceramika)	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. (*Przekroczenie tych wartości może spowodować trwałe uszkodzenie. Działanie funkcjonalne w tych warunkach nie jest domyślne.)

Recommended Operating Conditions (Zalecane warunki pracy) Voltages are with respect to ground (V_{SS}) unless otherwise stated. (Napięcia są względem masy (V_{SS}), chyba że zaznaczono inaczej.)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage (Napięcie zasilania)	V_{DD}	3.0	5.0	6.0	V	
2	Input Voltage (Napięcie wejściowe)	V_I	0		V_{DD}	V	
3	Operating Temperature (Temperatura robocza)	T_A	-40	+25	+85	°C	
4	Operating Frequency (Częstotliwość robocza)	f	0		2.0	MHz	

‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing. (‡Typowe wartości są przy 25°C i służą tylko do celów projektowych; nie są gwarantowane i nie podlegają testowaniu produkcyjnemu.)

DC Electrical Characteristics† (Charakterystyka elektryczna prądu stałego† Napięcia podane są względem (V_{SS}), chyba że podano inaczej. Voltages are with respect to (V_{SS}) unless otherwise stated.)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current (Prąd zasilania spoczynkowego)	I_{DD1}		2		µA	Outputs Unloaded (Wyjścia rozładowane)
2		Operating Supply Current (Prąd zasilania operacyjnego)	I_{DD}		2		mA/MHz	Outputs Unloaded (Wyjścia rozładowane/MHz bez obciążenia)
3	INPUTS	Input High Voltage (Napięcie wejściowe wysokiego) XTAL1	V_{IH}	3.0		V_{DD}	V	
		OTHER INPUTS (Inne wejścia)	V_{IH}	2.0		V_{DD}	V	
4		Input Low Voltage (Niskie napięcie wejściowe)	V_{IL}	0		0.8	V	
5		Input Leakage Current (Prąd upływu wejściowego) RxC (D0-D7) (odczyt, zapis)	I_{IZ}			10	µA	V_{IN} = 0 to V_{DD} (V_{IN} = 0 do V_{DD})
		Other Inputs (Except XTAL1) (Inne wejścia (oprócz XTAL1))	I_{IZ}			2.5	µA	V_{IN} = 0 to V_{DD} (V_{IN} = 0 do V_{DD})
6		Input Capacitance (Pojemność wejściowa) (D0-7, CS)	C_{IN}		5.0		pF	
		Other Inputs (Except XTAL1) (Inne wejścia (oprócz XTAL1))	C_{IN}		10.0		pF	
7		Output High Voltage (Wyjście wysokiego napięcia) (D0-7,TxD, RTS, DTR, RxC)	V_{OH}		V_{H}①		V	I_{OH} = -20 µA
		(D0-7,TxD, RTS, DTR, RxC) VOH 2.4	V_{OH}	2.4			V	I_{OH} = -100 µA
8		Output Low Voltage (Wyjście niskiego napięcia) (D0-7,TxD, RTS, DTR, IRQ, RxC)	V_{OL}			0.4	V	I_{OL} = 1.6 mA
		(D0-7,TxD, RTS, DTR, IRQ, RxC) (odczyt)						
9		Output Leakage Current (Prąd upływu wyjściowego) IRQ (OFF state) (IRQ (stan WYŁĄCZONY))	I_{OZ}		10		µA	V_O = Vss do V_{DD} (V_O = V_{SS} do V_{DD})
10		Output Capacitance (Pojemność wyjściowa)	C_O		5.0		pF	

†DC Electrical Characteristics are over recommended temperature range and recommended power supply voltages. (†Charakterystyka elektryczna prądu stałego w zalecanym zakresie temperatur i zalecanych napięciach zasilania.)

‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing. (‡Typowe wartości są przy 25°C i służą tylko do celów projektowych; nie są gwarantowane i nie podlegają testowaniu produkcyjnemu.)

① V_H = V_{DD} -0.1 Volts. (V_H = V_{DD} -0,1 Volta.)

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AC Electrical Characteristics[1]

Characteristics Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ[2]	Max	Units	Notes
1		Φ_2 Cycle Period	t_{CYC}	500	310		ns	See timing diagram 1
2		Φ_2 High Pulse Width	t_C	200			ns	See timing diagram 1
3		Address Setup Time	t_{AS}	70			ns	See timing diagram 2, 3
4		Address Hold Time	t_{AH}	0			ns	See timing diagram 2, 3
5		Φ_2 to Valid Data Delay	t_{DDR}			150	ns	See timing diagram 2
6		Data Hold Time (Read)	t_{DHR}	10			ns	See timing diagram 2
7		Data Setup Time (Write)	t_{DSW}	60			ns	See timing diagram 3
8		Data Hold Time (Write)	t_{DHW}	10			ns	See timing diagram 3
9		Read/Write Setup Time	t_{RWS}	70			ns	See timing diagram 2, 3
10		Read/Write Hold Time	t_{RWH}	0			ns	See timing diagram 2, 3
11	COMMUNICATION INTERFACE	External TxD Clock Cycle Period	t_{ECP}	0.4			µs	See timing diagram 4
12		External TxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 4
13		External TxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 4
14		External Clock to Valid Data Transmitted	t_{TXDD}			500	ns	See timing diagram 4
15		$\overline{RTS}$ and DTR Propagation Delay from Φ_2	t_{DLY}			500	ns	See timing diagram 5
16		$\overline{IRQ}$ Propagation Delay from Φ_2 (CLEAR)	t_{IRQD}			500	ns	See timing diagram 5
17		External RxD Clock Cycle Period	t_{ECP}	0.4			µs	See timing diagram 6
18		External RxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 6
19		External RxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 6

† Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in Figures 2 and 3.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note: Rise and Fall times (t_R & t_F) are 10 to 30 ns.

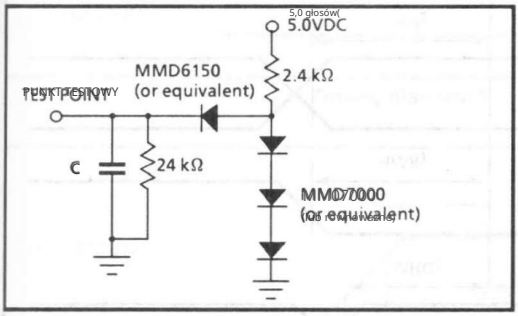

Figure 2. Test load for D_0–D_7, TxD, $\overline{DTR}$, $\overline{RTS}$

C = 130 pF for D_0–D_7, TxD, $\overline{DTR}$, $\overline{RTS}$; C = 30 pF for other outputs

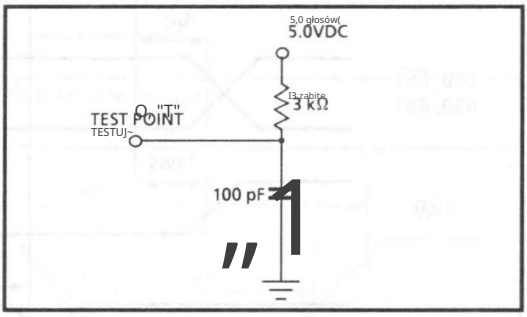

Figure 3. Test load for $\overline{IRQ}$

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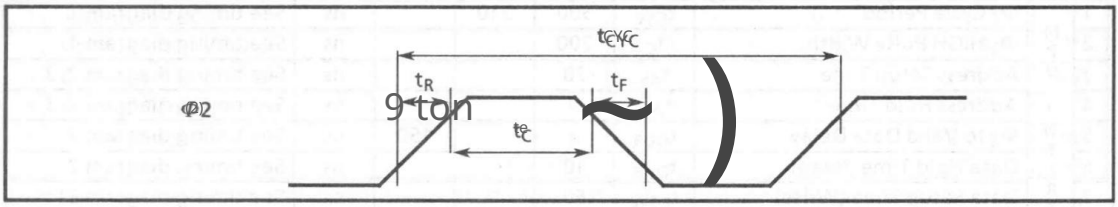
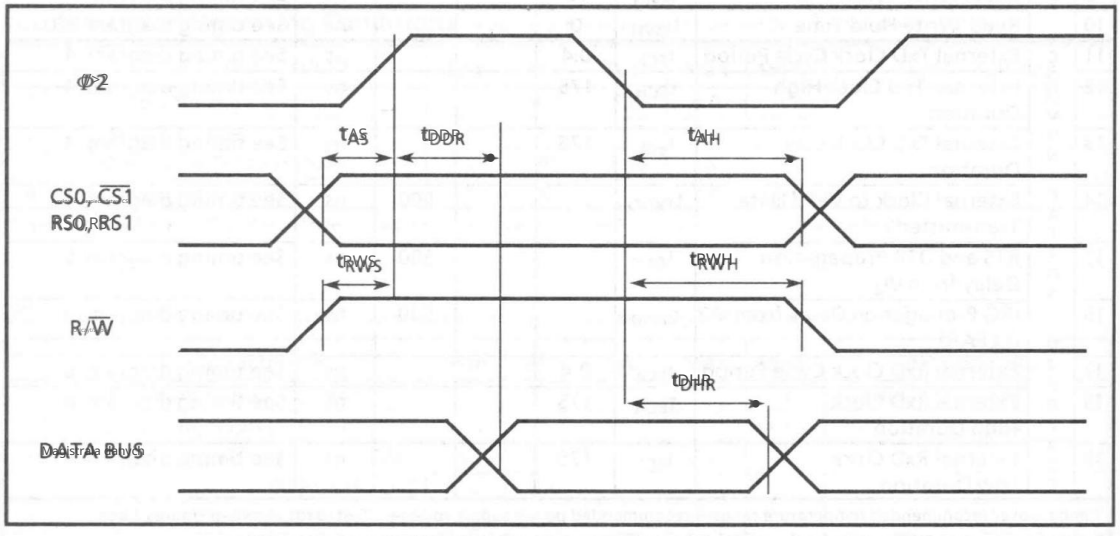
Timing Diagrams

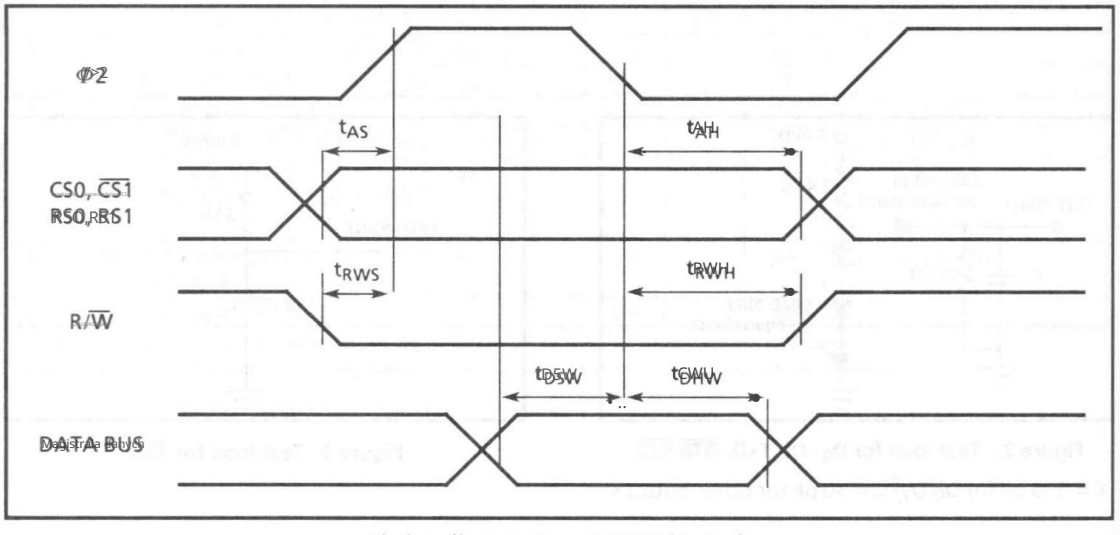
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs.



Timing diagram 1 - Φ2 clock



Timing diagram 2 - MPU Read Cycle



Timing diagram 3 - MPU Write Cycle

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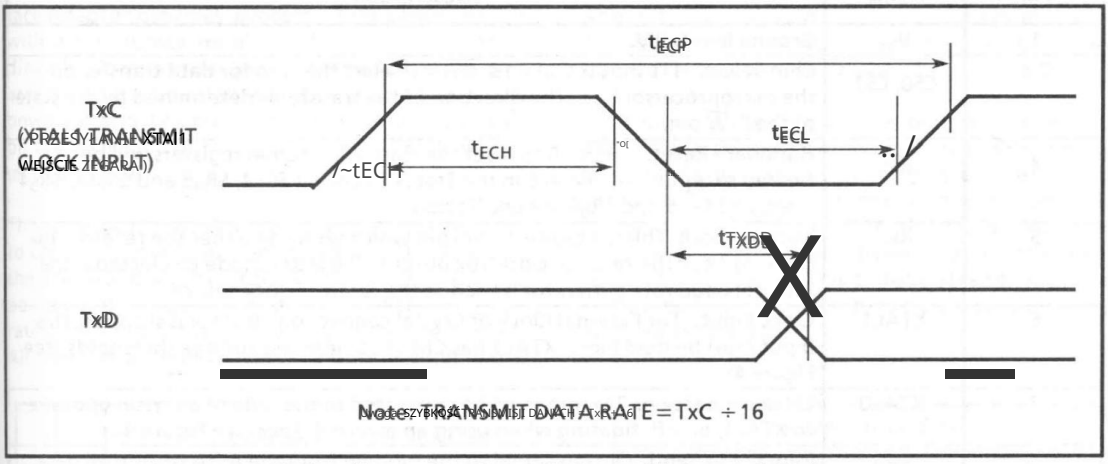
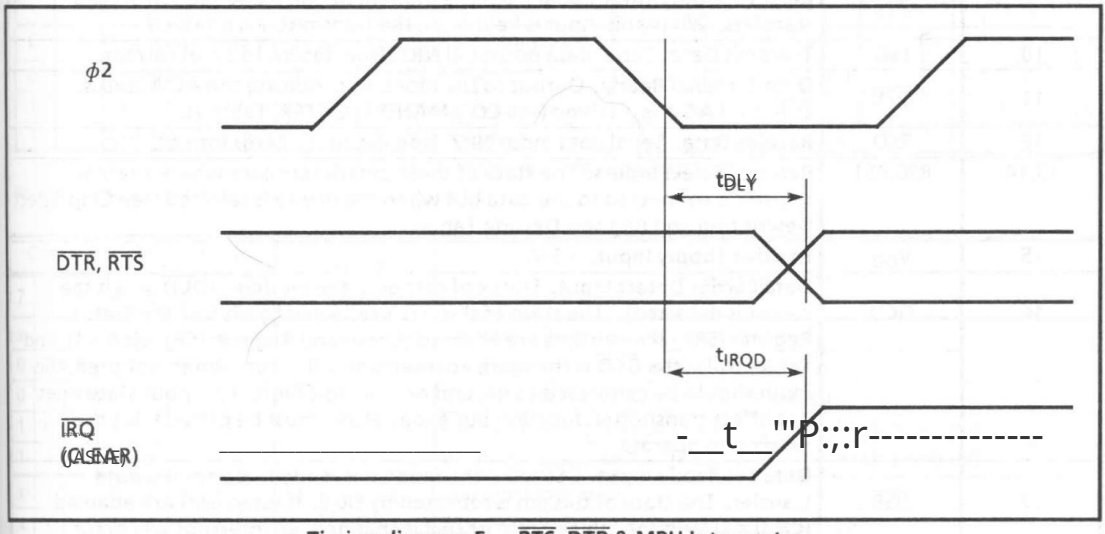
Timing Diagrams

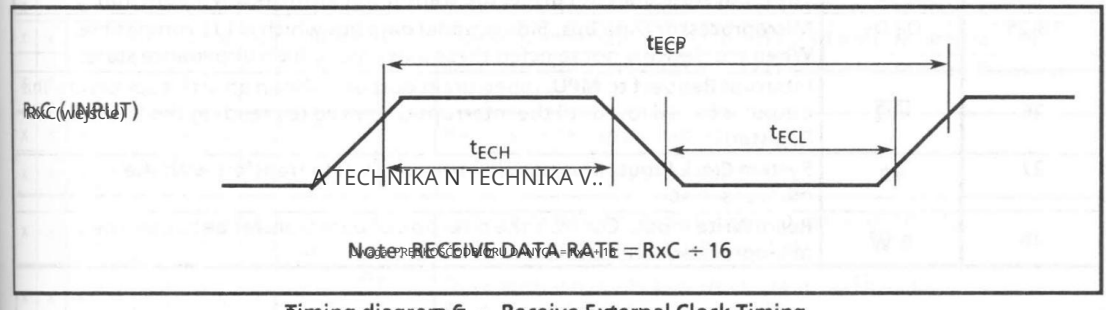
The points from which these timing values are measured are V_{IL} & V_{IH} for inputs and V_{OH} & V_{OL} for outputs.



Timing diagram 4 Transmit Data with External Clock



Timing diagram 5 RTS, DTR, Programmable MPU Interrupt



Timing diagram 6 Receive External Clock Timing

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Pin Description

Pin	Name	Description
1	V_{SS}	**Ground Input.** 0 V.
2,3	$CS0, \overline{CS1}$	**Chip Select.** The inputs CS0 = 1 and $\overline{CS1}$ = 0 select the chip for data transfer on the microprocessor bus. The direction of the transfer is determined by the state of the R/$\overline{W}$ pin.
4	$\overline{RES}$	**Hardware Reset.** $\overline{RES}$ = 0 to reset the chip. All internal registers will be cleared except bits 4, 5 and 6 in the Status Register (SR_b4, SR_b5 and SR_b6). SR_b4 is set, and SR_b5 and SR_b6 are unaffected.
5	RxC	**Receiver Clock.** This is a bidirectional pin which serves as either the receiver 16x clock input or the receiver clock 16x output. The latter mode is selected if the internal baud rate generator is used as the receiver clock source.
6	XTAL1	**Clock Input.** For External Clock or Crystal connection. If clock is stopped, this input must be held high. XTAL1 has CMOS compatible voltage thresholds (see Figure 4).
7	XTAL0	**Clock connection.** This pin must be connected to one side of a crystal opposite to XTAL1, or left floating when using an external clock (see Figure 4).
8	$\overline{RTS}$	**Request to Send.** Output signal to the modem from the ACIA to control data transfers (see COMMAND REGISTER, Table 2).
9	$\overline{CTS}$	**Clear to Send.** Input signal from the modem to the ACIA to control data transfers. When this input is held high, the transmitter is disabled.
10	TxD	**Transmit Data.** Serial data output in NRZ (Non Return to Zero) format.
11	$\overline{DTR}$	**Data Terminal Ready.** Output to the modem to indicate the ACIA status. $\overline{DTR}$ = 0 if ACIA is enabled (see COMMAND REGISTER, Table 2).
12	RxD	**Receive Data.** Serial data input NRZ (Non Return to Zero) format.
13,14	RS0,RS1	**Register Select Inputs.** The state of these pins determines which internal register is connected to the data bus when the device is selected (see Chip Select Description and Register Decode Table).
15	V_{DD}	**Positive Supply Input.** +5 V.
16	$\overline{DCD}$	**Data Carrier Detect Input.** Status of carrier at the modem. [$\overline{DCD}$ = 0 if the carrier is detected.] The state of this pin is reflected by bit 5 of the Status Register (SR). If interrupts are enabled (Command Register (CR) bit 0 = 1), and the logical state $\overline{DCD}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect transmitter function but a logical low must be present for the receiver to operate.
17	$\overline{DSR}$	**Data Set Ready Input.** $\overline{DSR}$ = 0 if the modem is ready to perform a data transfer. The state of this pin is reflected by SR_b6. If interrupts are enabled (CR_b0 = 1), and the logical state of $\overline{DSR}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect transmitter or the receiver function.
18-25	D_0-D_7	**Microprocessor Data Bus.** Bidirectional data bus which is TTL compatible. When the device is not selected these pins enter a high impedance state.
26	$\overline{IRQ}$	**Interrupt Request to MPU.** (open drain output). When an interrupt occurs, this output is driven low. Will remain low until interrupt is serviced (by reading the Status Register).
27	ϕ_2	**System Clock Input.** This signal synchronizes data transfers with the microprocessor.
28	R/$\overline{W}$	**Read/Write Input.** Controls the direction of data transfer between the microprocessor and the ACIA.

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Functional Description

Opis funkcjonalny

MD65SC51B Asynchronous Communications Interface Adaptor provides processor (µP) based systems with a full duplex serial interface. The µP port is directly compatible with 6800/6500 style bus architectures. Coupled with the Status Register, a powerful and flexible interrupt facility is included on the MD65SC51B to allow fast response from the µP to the ACIA.

Asynchroniczny adapter łączy komunikacja MD65SC51B zapewnia systemy oparte na procesorach (µP) z interfejsem szeregowym full duplex. Port µP jest bezpośrednio kompatybilny styl magistrali architektury. W połączeniu z Rejestrem statusu, wydajna i elastyczna funkcja przerwania funkcji w jest włączony MD65SC51B, umożliwiająca szybką reakcję µP do ACIA.

The serial port provides signals which may be used to control a communication channel compatible to the EIA Standard RS-232C specification. An on-board baud rate generator allows 16 different baud rates for data transmission and reception timing. All frequencies are derived from an external clock or crystal. The receive frequency may be received separately from the transmit frequency, allowing reception and transmission at independent speeds. Alternatively, the ACIA will produce a signal that is 16 times the baud rate for use by a remote ACIA (See Pin Description - RxC).

Port szeregowy dostarcza sygnały, które mogą być wykorzystane kontrolować kanał komunikacyjny zgodny z Specyfikacja standardu EIA-RS-232C . Wbudowany generator prędkości transmisji umożliwia 16 różnych prędkości transmisji stawka za transmisję danych i AP . godziny odbioru . All częstotliwości pochodzą z zegara zewnętrznego częstotliwość lub kryształ. Częstotliwość odbierania może być oddzielna odbiór i transmisja z niezależnymi prędkościami. Alternatywnie, ACIA wygeneruje sygnał, który jest 16-krotna szybkość transmisji, do wykorzystania przez zdalny ACIA (Zobacz opis pinu - RxC).

The format of the data word is programmable. The word length ranges from five to nine bits (including parity). Parity can be odd, even or deselected altogether. The parity bit may also be forced high or low. Either 1, 1.5 or 2 stop bits may be added to the end of the serial data stream. For maintenance applications, the received data stream may be looped back onto the transmit data stream using echo mode operation.

Format słowa danych jest programowalny. długość słowa waha się od pięciu do dziewięciu bitów (włączając parzystość). Parzystość może być nieparzysta, parzysta lub niezaznaczone całkowicie. Bit parzystości może być wymuszony na wysoki lub niski. Można dodać 1, 1,5 lub 2 bity stopu konce strumienia danych szeregowych. W celu konserwacyjnych aplikacje, odebrany strumień danych może być zapętlone z powrotem do strumienia danych transmisyjnych przy użyciu praca w trybie echa .

RS1	RS0	Internal Register Selected Wewnętrzny rejestr wybrany		Reset Operation Effect Resetuj efekt operacji															
				Hardware Reset Resetowanie sprzętowe								Programmed Reset Zaprogramowany reset							
		Write Pisać	Read Czytać	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	Transmit Data Register Rejestr danych transmisji	Receive Data Register Odbierz rejestr danych	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	1	Programmed Reset Zaprogramowany reset	Status Register Status Rejestracji	0	-	-	-	1	0	0	0	-	-	-	-	-	0	-	-
1	0	Command Register Rejestr poleceń	Command Register Rejestr poleceń	0	0	0	0	0	0	0	0	-	-	-	0	0	0	0	0
1	1	Control Register Kontroler Rejestrów	Control Register Kontroler Rejestrów	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Table 1 - Register Address Decoding
Tabela 1 - Dekodowanie adresu rejestru

Note: "-" denotes no change from state previous to reset
Notatka: „-” oznacza brak zmiany z poprzedniego stanu do resetowania

Command Register Bit Rejestr poleceń Bit									Control Function Kontrola Funkcja	Resulting Function Funkcja wynikowa
7	6	5	4	3	2	1	0			
x	x	x	0	x	x	x	x	x	Parity Mode Control Tryb parzystości Kontrola	No Parity Bit transmitted or received. Brak przesłanego bitu parzystości lub otrzymanego.
0	0	0	1	x	x	x	x	x		Odd Parity Bit transmitted or received. Nieparzysty bit parzystości przesłany lub odebrany.
0	1	1	1	x	x	x	x	x		Even Parity Bit transmitted or received. Przesłanie lub parzystość.
1	0	0	1	x	x	x	x	x		Parity Bit set to MARK (Receive parity check disabled). Bit parzystości ustawiony na MARK (sprawdzanie parzystości odbioru wyłączone).
1	1	1	1	x	x	x	x	x		Parity Bit set to SPACE (Receive parity check disabled). Bit parzystości ustawiony na SPACJĘ (sprawdzanie parzystości odbioru wyłączone).
x	x	x	0	0	x	x	x	x	Echo Mode Enable Tryb echa Włączać	Normal Operation. Operacja normalna.
x	x	1	0	0	0	x	x	x		Echo Mode Enabled (bits 2 and 3 must be 0). Tryb echa włączony (bity 2 i 3 muszą być ustawione na 0).
x	x	x	0	0	0	x	x	x	Transmit Interrupt Control Przerwanie transmisji Kontrola	Transmit interrupt disabled. RTS set High (Transmitter off). Przerwanie transmisji wyłączone. rnset High (Nadajnik wyłączony).
x	x	x	0	1	0	x	x	x		Transmit interrupt enabled. RTS set Low (Transmitter on). Włączono przerwanie transmisji. rnset Low (Nadajnik włączony).
x	x	x	1	0	0	x	x	x		Transmit interrupt disabled. RTS set Low (Transmitter on). Przerwanie transmisji wyłączone. rnset Low (Nadajnik włączony).
x	x	x	1	1	0	x	x	x		Transmit interrupt disabled. RTS set Low (Transmit Break on TxD). Przerwanie transmisji wyłączony. rnset Low (przerwa transmisji włączona) TxD).
x	x	x	x	x	x	x	0	x	Receiver Interrupt Enable Odbiornik Przerywać Włączać	Receiver interrupts enabled. Przerwania odbiornika włączone.
x	x	x	x	x	x	x	1	x		Receiver interrupts disabled. Przerwania odbiornika wyłączone.
x	x	x	x	x	x	x	0	x	Data Terminal Ready Terminal danych Gotowy	Data terminal not ready to transfer data. (DTR = 1). Terminal danych nie jest gotowy do przesyłania danych (DTR = 1). Receiver and all interrupts disabled. Odbiornik i wszystkie inne przerwania wyłączone.
x	x	x	x	x	x	x	1	x		Data terminal ready to transfer data. (DTR = 0). Terminal danych gotowy do przesyłania danych (DTR = 0). Receiver and all interrupts enabled. Odbiornik i wszystkie inne przerwania włączone.

Table 2 — Command Register Description
Tabela 2 — Opis rejestru poleceń

Note: "x" is a don't care or all symbol. Przykład: „x” to nie obchodzi lub reprezentuje wszystkie symbole. Patrz tabela 3 dla dalszych wyjaśnień.

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Serial Interface Description

Transmitted and Received Data

Data is transmitted from the ACIA on the TxD pin, and received on the RxD pin. The inactive state of either data channel (RxD or TxD) is a mark condition (logical high). This type of data code is termed Non-Return to Zero (NRZ). Data transmitted or received by the MD65SC51B is always preceded by a "start bit".

The start bit is a space condition (logical low) which signifies the start of active data on the channel. The receiving ACIA also uses the start bit to optimize its sampling for the middle of the data bits that follow. Between received words, the ACIA samples the channel at 16x Baud rate. When a low is detected, the ACIA waits half a bit period before sampling again. This delay allows subsequent bits (sampled at the same frequency as the baud rate) to be sampled as far from the bit boundaries as possible. Noise or "glitch" immunity is also added by this mechanism. Low going pulses of less than 1/2 a bit period wide will not be mistaken for the start bit (the ACIA resumes the 16x sampling rate).

Data bits following the start bit are in ascending order with the least significant bit (LSB) first, and the most significant bit (MSB) last. The MSB depends on the number of bits per word selected; the ACIA can be programmed for 5 bit, 6 bit, 7 bit or 8 bit data word transmission/reception. Each bit has a period equal to the reciprocal of the selected baud rate, which in turn is dependent on the clock source frequency (see Table 4).

Parity sensing and generation can be chosen for odd parity, even parity or no parity. When parity is selected, the parity bit follows the MSB of the data word. For even parity, the condition of the parity bit will be such that there are an even number of

Control Register Bit								Control Function	Resulting Function
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	Stop Bit Control	1 stop bit.
1	x	x	x	x	x	x	x		2 stop bits except in the following cases: a/ 1 bit stop if word length set for 8 bits & parity enabled ② b/ 1.5 stop bits if word length set for 5 bits & parity disabled
x	0	0	x	x	x	x	x	Word Length Setting	8 bits.
x	0	1	x	x	x	x	x		7 bits.
x	1	0	x	x	x	x	x		6 bits.
x	1	1	x	x	x	x	x		5 bits.
x	x	x	0	x	x	x	x	Receive Clock Source	External clock source. (RxC is Input)
x	x	x	1	x	x	x	x		Internal baud rate generator. (RxC is Output)
x	x	x	x	0	0	0	0	Baud Rate Control	115.2 kbaud ① or (Frequency) ÷ 16
x	x	x	x	0	0	0	1		50 baud ① or (Frequency) ÷ 36,864
x	x	x	x	0	0	1	0		75 baud ① or (Frequency) ÷ 25,576
x	x	x	x	0	0	1	1		109.92 baud ① or (Frequency) ÷ 16,769
x	x	x	x	0	1	0	0		134.58 baud ① or (Frequency) ÷ 13,704
x	x	x	x	0	1	0	1		150 baud ① or (Frequency) ÷ 12,288
x	x	x	x	0	1	1	0		300 baud ① or (Frequency) ÷ 6,144
x	x	x	x	0	1	1	1		600 baud ① or (Frequency) ÷ 3,072
x	x	x	x	1	0	0	0		1200 baud ① or (Frequency) ÷ 1,536
x	x	x	x	1	0	0	1		1800 baud ① or (Frequency) ÷ 1,024
x	x	x	x	1	0	1	0		2400 baud ① or (Frequency) ÷ 768
x	x	x	x	1	0	1	1		3600 baud ① or (Frequency) ÷ 512
x	x	x	x	1	1	0	0		4800 baud ① or (Frequency) ÷ 384
x	x	x	x	1	1	0	1		7200 baud ① or (Frequency) ÷ 256
x	x	x	x	1	1	1	0		9600 baud ① or (Frequency) ÷ 192
x	x	x	x	1	1	1	1		19.2 kbaud ① or (Frequency) ÷ 96

Table 4. Control Register Description

Notes: ① The preset baud rates given assume a crystal frequency of 1.8432 MHz
② To enable and disable parity, see Table 2.

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marks when considering the data word and the parity bit. With odd parity the condition of the parity bit will be such that there is an odd number of marks when considering the data word and the parity bit (both cases exclude the start and stop bits).

Transmit and Receive Clocks

The signals used by the ACIA for transmit/receive timing are found on three pins: XTAL0, XTAL1, and RxC. XTAL1 and XTAL0 are the input and output, respectively, of a crystal oscillator circuit. The crystal can be connected to these pins as seen in Figure 4. This oscillator circuit drives the internal baud rate generator, which divides the squarewave output of the oscillator by the divisor selected (see Table 4). If a crystal is not used, an external clock may drive the oscillator input while the oscillator output is left floating. If the clock is stopped (device still powered), the oscillator input should be held to a logical high.

The clock for the receiver may be taken from one of two sources: the output of the internal baud rate generator, or from an external clock input on the RxC pin. In the latter case the baud rate is 1/16th of the external clock. If the source of receiver timing is the internal baud rate generator, RxC becomes an output and produces a clock 16 times (16x) the baud rate (for driving remote ACIAs).

Control Signals

The signals are compatible with the RS-232C modem control circuits. The signals are the Request To Send (RTS), Data Terminal Ready

Characteristics	Spec.
Temperature stability @ 45 to + 85°C	±0.01%
Frequency* (MHz)	1.8432
Frequency tolerance* (±%)	0.02
Resonance mode*	parallel
Equivalent resistance* (ohms)	400 max.
Drive level* (mW)	2
Shunt capacitance* (pF)	7 max.
Load capacitance* (pF)	16.5 typ.
Oscillation mode*	Funda-mental

Table 6 Crystal Specification

*characteristics at 25°C ± 2°C

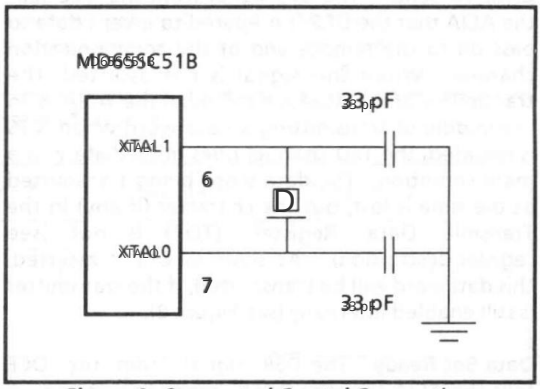

Figure 4 Suggested Crystal Connection

Status Register bit	Control Signal	Status Flag Set by	Status Flag Cleared by
0	PARITY ERROR③	Parity error detected.	Cleared Automatically after a read of the receive data Register and next error free reception of data.
1	FRAMING ERROR③	Framing error detected.	
2	OVERRUN③	Overrun has occurred.	
3	RECEIVE REGISTER FULL	Receive Register full.	Read Receive Data Register
4	TRANSMIT REGISTER EMPTY	Register empty.	Write Transmit Data Register.
5	$\overline{DCD}$	Carrier not detected (a high on $\overline{DCD}$).	Carrier detected (a low on $\overline{DCD}$).④
6	$\overline{DSR}$	Data set not ready (a high on $\overline{DSR}$).④	Data set ready (a low on $\overline{DSR}$).④
7	INTERRUPT	Interrupt has occurred. The $\overline{IRQ}$ signal to the microprocessor also goes low.	Read Status Register. This also clears the $\overline{IRQ}$ signal to the microprocessor.

Table 5 Status Register Description

Notes
③ No interrupt is generated from these conditions.
④ These bits are not resetable and reflect the state of the input.

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($\overline{DTR}$) outputs and the Clear To Send ($\overline{CTS}$), Data Set Ready ($\overline{DSR}$) and Data Carrier Detect ($\overline{DCD}$) inputs. Note that the ACIA is viewed as the Data Termination Equipment (DTE) as opposed to the Data Communication Equipment (DCE) when referencing the RS-232C specification.

Request To Send — $\overline{RTS}$ is used to indicate to the DCE that it should assume the data channel transmit mode. The state of this output is controlled by bits 2 and 3 of the Command Register (COMR$_b$2 and COMR$_b$3, see Table 2). When it is high (not asserted, or in other words, "negated") the ACIA's transmitter is disabled.

Data Terminal Ready — The $\overline{DTR}$ signal indicates to the DCE that the ACIA is ready for communication. This output is asserted when COMR$_b$0 is set.

Clear To Send — The $\overline{CTS}$ signal from the DCE tells the ACIA that the DCE is prepared to accept data to pass on to the remote end of the communication channel. When this signal is not asserted, the transmitter of the ACIA is disabled. If the ACIA is in the middle of transmitting a data word when $\overline{CTS}$ is negated the TxD channel goes immediately to a mark condition. The data word being transmitted at the time is lost, but the character (if any) in the Transmit Data Register (TDR) is not (see register description). As soon as $\overline{CTS}$ is asserted, this dataword will be transmitted, if the transmitter is still enabled internally (see Figure 8).

Data Set Ready — The $\overline{DSR}$ signal from the DCE tells the ACIA that the DCE is ready to operate. A transition on this pin causes an interrupt (if interrupts are enabled) and the state of the pin is reflected in the state of SR$_b$6. Transitions that follow will not affect the status bit until after the µP has serviced the first interrupt (read the SR). At that point, the SR will again reflect the current level of the $\overline{DSR}$ input, and an interrupt will occur again if it has changed. Transmitter and receiver operation is not affected by the level of this pin.

Data Carrier Detect — The $\overline{DCD}$ signal from the DCE tells the ACIA that the received signal is within specified limits. When $\overline{DCD}$ is not true the receiver of the ACIA will be disabled and the data being shifted in at that moment is lost. A transition on this pin, like the $\overline{DSR}$ input, causes an interrupt. Subsequent transitions will not affect the status bit until the first interrupt is serviced. If the pin has changed since the first occurred and before it was serviced, another interrupt will occur. An even number of level changes on $\overline{DSR}$ and $\overline{DCD}$, before the first interrupt has been serviced, will not cause another interrupt. This is because the status bits will be at the same logic level that caused the original interrupt.

Register Description

The MD65SC51B contains seven registers, five that are visible to the µP. These registers are the Transmit Shift Register (TSR, not available to µP), the Receive Shift Register (RSR, not available to µP), the Transmit Data Register (TDR), the Receive Data Register (RDR), the Status Register (SR), the Command Register (COMR), and the Control Register (CR). One of the five latter registers is visible to the µP when the chip selects (CS0, $\overline{CS1}$) are asserted and the E clock is true (high); the register chosen by the state of the register selects (RS0, RS1). The direction of µP bus transfer is determined by the state of the R/$\overline{W}$ signal (a high indicates a read of the contents of the register, a low a write to a register). When the SR is written to (the data written doesn't matter) a software reset will occur. For a comparison between the effect of a hardware reset and a software reset, see Table 1.

Transmit Data Register

The Transmit Data Register (TDR), in conjunction with the Transmit Shift Register, is used to place data on the transmit channel (TxD). If no word is being transmitted, a data word written to the TDR is immediately transferred into the TSR to be shifted out. A start bit precedes the data on the TxD channel; parity is added to the end of the word as needed (after the valid MSB is shifted out); and 1, 1.5, or 2 stop bits follow to end the transmitted information. If the ACIA is programmed to send a data word that is less than 8 bits in length (5, 6 or 7 bits), the extra bits in the data word are ignored.

While the TSR is occupied shifting out active data on to TxD (including the bit periods for the transmission of parity bits and stop bits), information written to TDR will be latched and held. When the last stop bit of the previous word is finished, the ACIA will transfer the data word in the TDR into the TSR and transmit it. If the TDR is written to more than once while information is being transmitted on TxD, the data word in TDR will be overwritten and retain the data associated with the last write.

If transmit interrupts are enabled, when the TDR is empty, an interrupt will occur and SR$_b$4 will be set (SR$_b$4 will be set even if interrupts are disabled). This coincides with the beginning of the start bit for the data just transferred to the TSR. The interrupt must be serviced (by reading SR) but SR$_b$4 may only be cleared by a write to the TDR. If the interrupt is serviced but TDR is not written to,

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another interrupt will occur at the next word boundary (word boundaries are referenced to the start of the last transmitted word, and occur every full word period after the end of that word. This timing is reset by a new transmission because, if TxD is idle the new word is transmitted immediately - see Figures 5 & 7.

Receive Data Register

Data on the receive channel (RxD) is stripped of the overhead bits (start, parity and stop) by the ACIA and shifted into the Receive Shift Register (RSR). When a full data word has been received (depending on the programmed length), the contents of the RSR are transferred into the Receive Data Register (RDR). If receive interrupts are

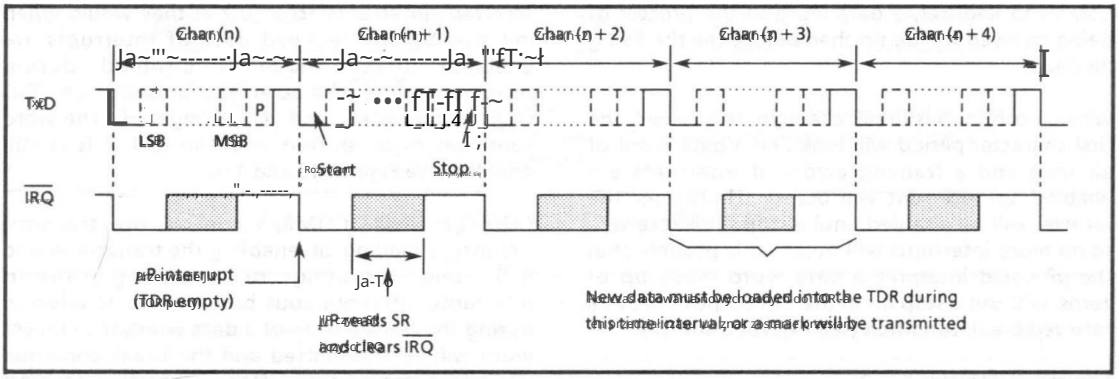

Figure 5. Continuous Data Transmit

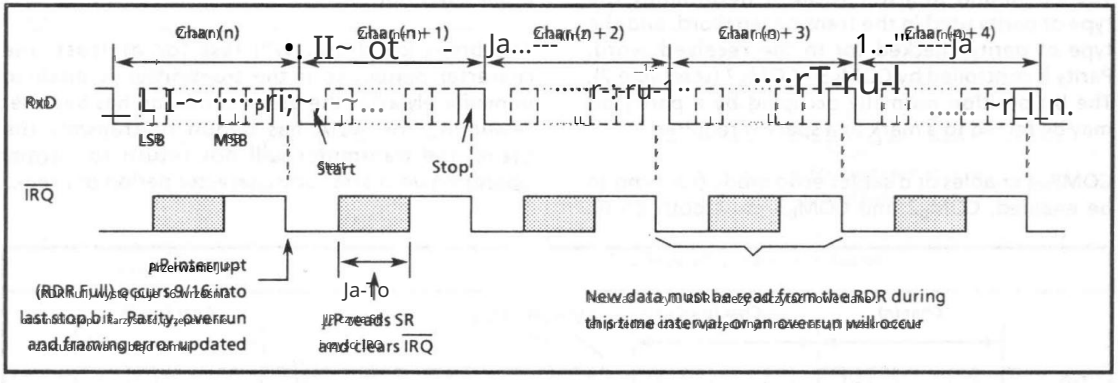

Figure 6. Continuous Data Receive

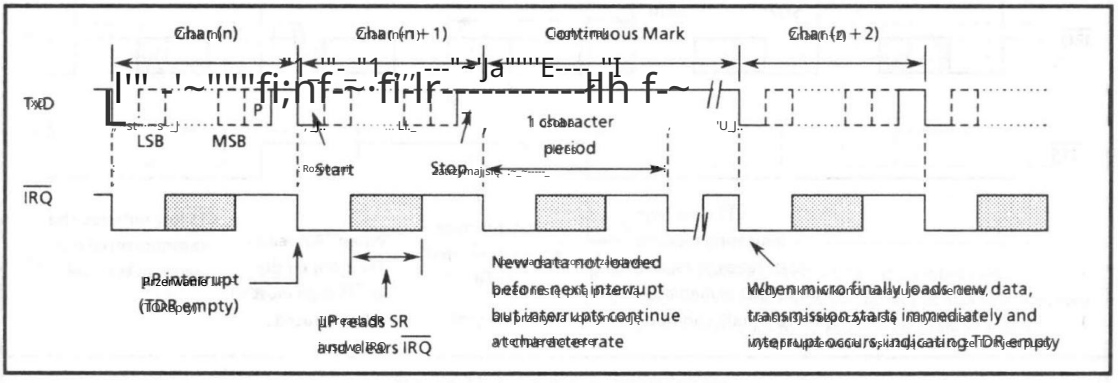

Figure 7. TDR not Loaded by Processor

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enabled, this transfer will cause an interrupt to occur and SR_b3 to be set (SR_b3 is set even when interrupts are disabled). The interrupt actually occurs about 9/16 through the last stop bit. As with the TDR, the interrupt is removed by reading SR and SR_b3 is cleared by reading the RDR.

If $\overline{DCD}$ is not asserted the RSR is immediately disabled and any word being received at the time is lost. If the receive circuitry is disabled through the Command Register, a data word in the process of being received will be finished before the the RSR is disabled.

When a continuous break character is received, the first character period will look like a data word of all zeros and a framing error. If interrupts are enabled, an interrupt will occur. Thereafter the receiver will be disabled until a stop bit is received, so no more interrupts will occur. It is possible that the μP could interpret a data word made up of zeros, without a stop bit in the correct position, as a received break condition (see Figures 6 and 12).

Command Register

The Command Register (COMR) determines the type of parity used in the transmitted word, and the type of parity checked for in the received word. Parity is controlled by COM_b5 - COM_b7 (see Table 2). The bit position normally occupied by a parity bit may be forced to a mark or a space if required.

$COMR_b4$ enables or disables echo mode (for echo to be enabled, COM_b2 and COM_b3 must both be 0).

When in echo mode the ACIA's receive circuitry is still operational but data written to the TDR will not be transmitted until echo mode is disabled and the transmitter re-enabled. $\overline{RTS}$ is asserted in echo mode, even though it is not programmed to be active by $COMR_b3$ and $COMR_b2$.

When data is received on RxD (the receiver must be enabled internally and $\overline{DCD}$ true) it is transmitted 1/2 bit period after it has been received. Interrupts occur just as they would when initiated by a received word (if interrupts are enabled). If echo mode is disabled during reception of a character transmission on TxD stops immediately and $\overline{RTS}$ is negated. The word continues to be shifted into the RSR if it is still enabled (see Figures 10 and 11).

$COMR_b2$ and $COMR_b3$ control the transmit circuitry, disabling or enabling the transmitter and $\overline{RTS}$, and disabling or enabling transmit interrupts. If continuous break mode is selected during the transmission of a data word, the current word will be transmitted and the break condition will begin immediately after. Transmit interrupts are automatically disabled during the transmit break condition.

The break condition will last for at least one character period. If the transmitter is enabled immediately after the break condition has been set (assuming the ACIA has begun to transmit the break) the transmitter will not return to normal operation until after one character period of break.

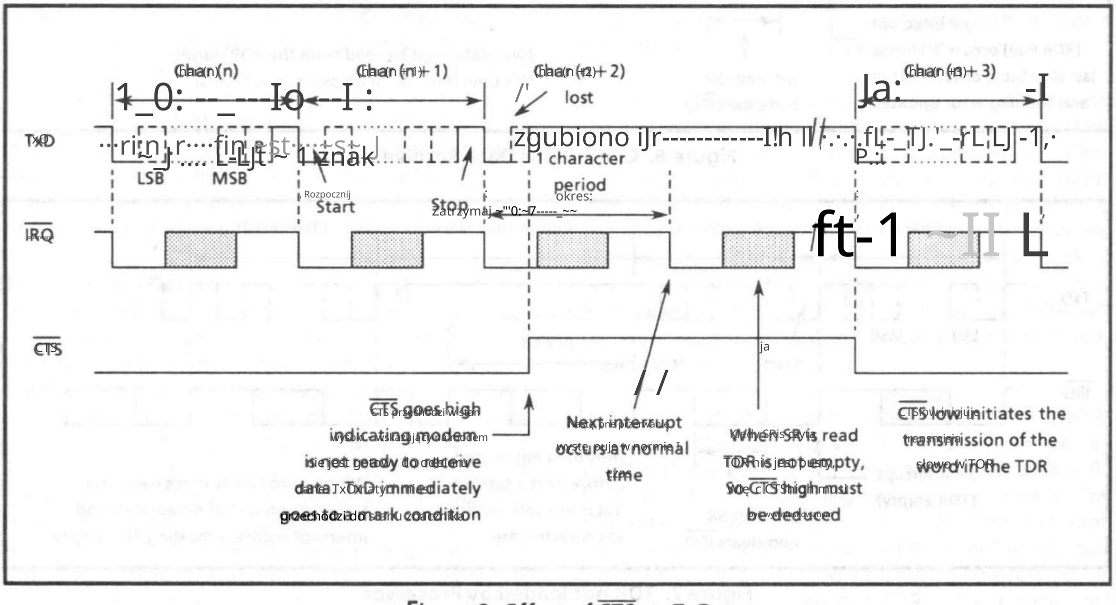

Figure 8. Effect of $\overline{CTS}$ on TxD

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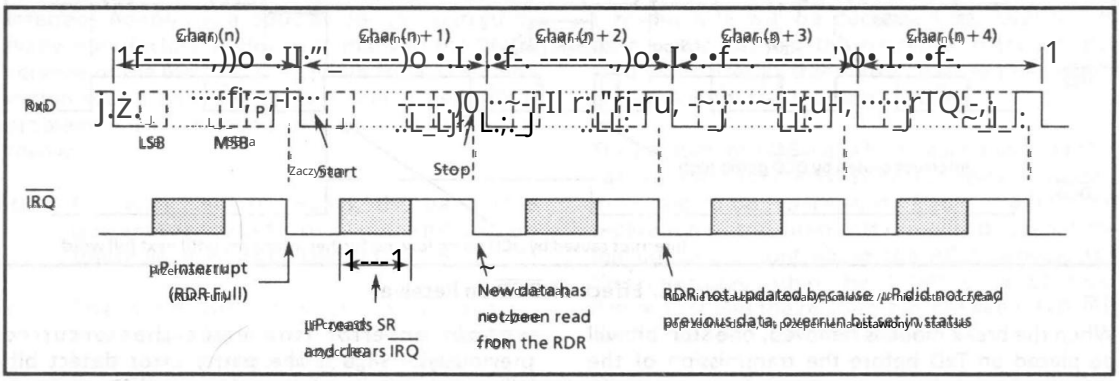

Figure 9. Effect of Overrun on Receiver

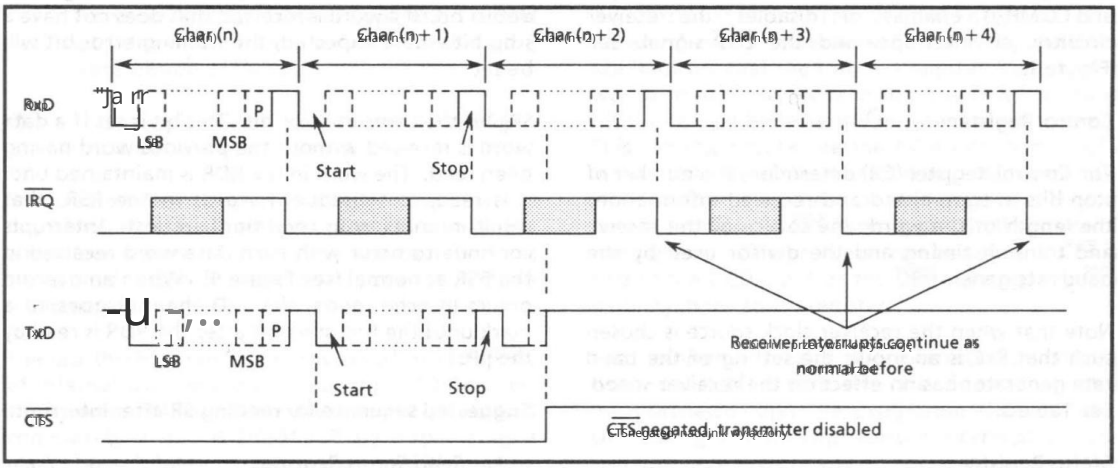

Figure 10. Effect of CTS on Echo Mode operation

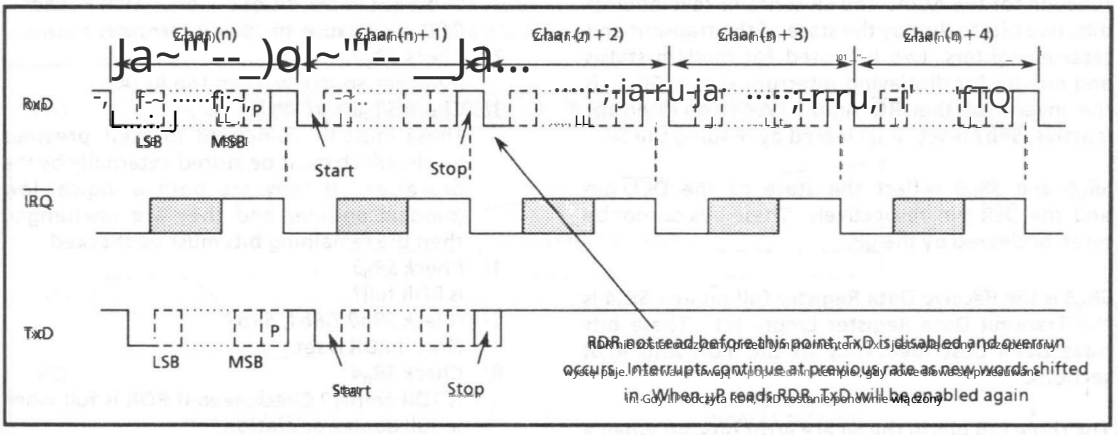

Figure 11. Overrun in Echo Mode

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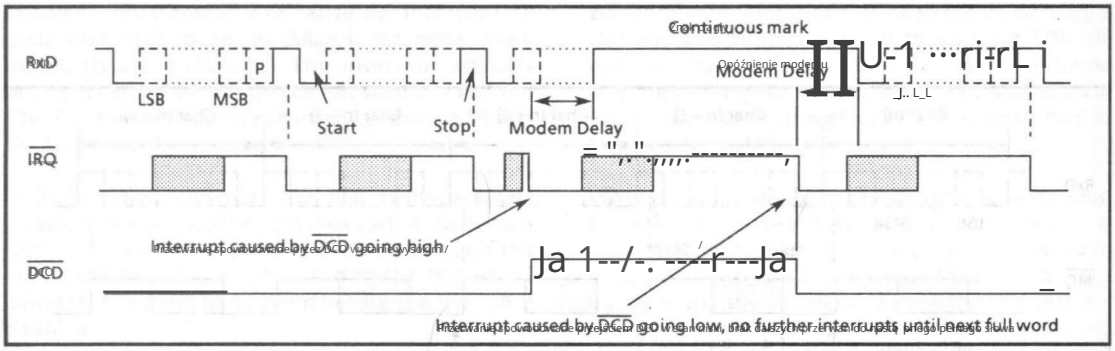

Figure 12. Effect of $\overline{DCD}$ on Receiver

When the break mode is removed, one stop bit will be placed on TxD before the transmission of the next word.

COMR$_1$ enables or disables receiver interrupts and COMR$_0$ enables or disables the receiver circuitry, all interrupts and the $\overline{DTR}$ signal. See Figure 3.

Control Register

The Control Register (CR) determines the number of stop bits in transmitted and received information; the length of the word: the source of the receive and transmit timing and the divisor used by the baud rate generator.

Note that when the receiver clock source is chosen such that RxC is an input, the selection of the baud rate generator has no effect on the receiver speed. See Table 3.

Status Register

The Status Register (SR) performs a "housekeeping" function for the ACIA. The SR contains several error bits, two bits to display the state of the transmit and receive registers, two bits used for modem status and one bit for displaying interrupt status. SR$_b$7 is the inverse of the $\overline{IRQ}$ signal. When an interrupt is active, SR$_b$7 is set high. It is cleared by reading the SR.

SR$_b$5 and SR$_b$6 reflect the state of the $\overline{DCD}$ pin and the $\overline{DSR}$ pin respectively. These bits cannot be reset or cleared by the µP.

SR$_b$3 is the Receive Data Register Full bit and SR$_b$4 is the Transmit Data Register Empty bit. These bits have been described fully in the TDR and RDR sections.

The three SR bits in the SR are error bits, set when a specific error condition occurs. These bits may only be cleared after the RDR is read and a word is received without an error (the error that occurred previously). SR$_b$0 is set if parity is enabled and the level of the parity bit received by the ACIA was incorrect. SR$_b$1 is the framing error bit. If a word is received that does not have a stop bit where expected the framing error bit will be set.

SR$_b$2 is the overrun error bit. This bit is set if a data word is received without the previous word having been read. The word currently in the RDR is maintained until it is read, so subsequent words in the RSR, that result in an overrun condition, are lost. Interrupts continue to occur with each data word received in the RSR as normal (see Fig. 9). When an overrun occurs in echo mode, the TxD channel goes to a mark until the first start bit after the RDR is read by the µP.

Suggested sequence for reading SR after interrupt:

1/ *Read Status Register.*
This operation automatically clears SR$_b$7 and negates the IRQ signal. Subsequent transitions on DSR and DCD will cause another interrupt.

2/ *Check SR$_b$7*
If not set, your code was not the ACIA.

3/ *Check SR$_b$6 and SR$_b$5*
These must be compared to their previous levels, which must be stored externally by the processor. If they are both a logical low (modem on-line) and they are unchanged then the remaining bits must be checked.

4/ *Check SR$_b$3*
Is RDR full?

5/ *Check SR$_b$0, SR$_b$1, SR$_b$2*
Or, if RDR is set.

6/ *Check SR$_b$4*
Is TDR empty? Check even if RDR is full when in full duplex operation.

7/ If none of the above occurred, $\overline{IRQ}$ must have been negated.

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MD65SC51B ACIA Improvements

The MD65SC51B Asynchronous Communications Interface Adapter is a popular design, sourced by many manufacturers. However, many of the CMOS versions of the 6551 ACIA originate from a common design source and may present some intermittent problems. The problems may be summarized as follows:

a) In "noisy" environments, the baud rate may be set to zero, thereby inhibiting transmission and/or reception.

b) The start bit of a character would occasionally be shorter than it should have been for a particular baud rate setting.

c) Information being transmitted could be overwritten by information meant for the Transmit Register. Correct operation would latch the new information while finishing the transmission of the old.

d) The parity bit would occasionally be set when it should have been cleared.

The first problem may occur when noise sets the programmable baud rate generator logic array into a disallowed state. The solution was to detect this state and, upon detection, reset the state immediately.

The last three problems are the result of sensitivity of internal asynchronous signals to CMOS process variations. These problems can be solved in the MD65SC51B by appending a mark state 1/16th of a bit period in width, to the last stop bit of each transmitted character. This extra mark time may affect device operation in instances where the total bandwidth of the ACIA transmit channel is used. In such a case, if the ACIA is set up to transmit characters that are, for example, 10 bits in length (including start, stop and parity bits), the maximum throughput of the ACIA on the transmit side will be decreased by 0.625%. In normal applications this decrease in throughput would be offset by transmitter inactive time, where the ACIA is not transmitting anything.

The addition of 1/16th of a bit to each character also causes two formerly simultaneous transmit interrupts to be separated by 1/16th of a bit. This separation of the interrupts can only be seen if the microprocessor is controlling the ACIA services the first interrupt within the 1/16th of a bit time. Figure 13 shows the relationship between TxD, $\overline{IRQ}$ and the added 1/16th mark state.

The transmit interrupts are caused by the end of the stop bit of the last transmitted character and the falling edge of the start bit of the next character being transmitted. The second interrupt is a potential problem because the status register does not indicate that the transmit register is empty if it was written to when servicing the first interrupt (this is logical because the register is not empty). This condition looks like the ACIA just had its $\overline{CTS}$ input negated while transmitting one character with another in the transmit register. This is only a problem if $\overline{CTS}$ is being used for flow control applications. The problem can be solved if $\overline{CTS}$ is tied to the $\overline{DCD}$ input or the $\overline{DSR}$ input, giving $\overline{CTS}$ visibility in the status register.

The occurrence of the two interrupt condition is obviously affected by the speed of the microprocessor and the programmed baud rate. Decreasing the microprocessor interrupt service routine execution speed or increasing the programmed baud rate of the ACIA decreases the chances of servicing the first interrupt within 1/16th of a bit.

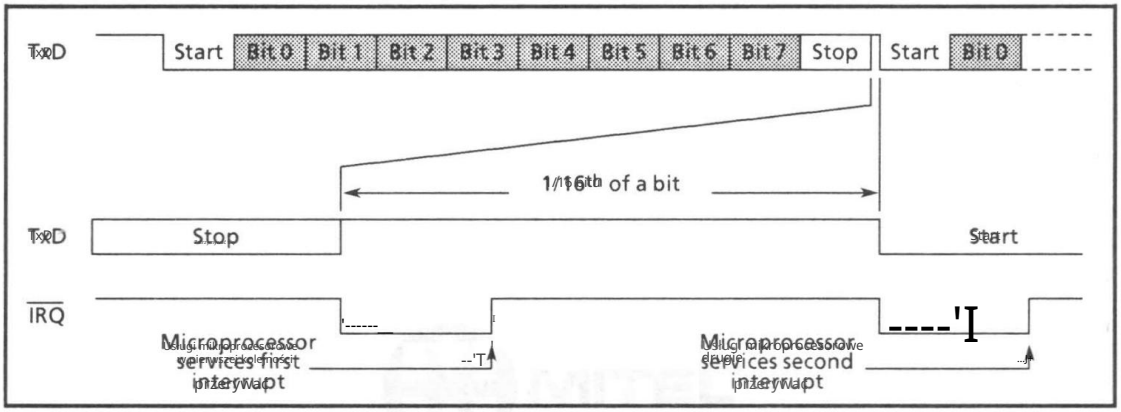

Figure 13. Relationship between TxD and $\overline{IRQ}$

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NOTES:

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CUSTOM HYBRIDS

HYBRYDY NA ZAMÓWIENIE

6

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9161-002-121-NA ISSUE 1 September 1989

Features

- Total customized SLIC solution
- Compact package outline
- Low tooling costs
- Flexible design approach
- Few external components necessary

Applications

SLIC interface for:

- PABX's
- Key Systems
- Intercoms
- Central Office
- Channel Bank

Description

Mitel Semiconductor's thick film hybrid facility is dedicated to the manufacture of hybrids for the telecommunications industry. A major portion of the facility is for the manufacture of ASIMs (Applications Specific Integrated Modules).

ASIMs combine Mitel's applications expertise and design with manufacturing technologies to offer unique customer specific solutions.

Design experience in communications, combined with Mitel's VLSI and advanced interconnect technologies, result in integrated modules tailored for individual customer applications.

ASIMs offer significant systems cost reductions together with all the inherent advantages of modular design approach.

This data sheet is intended as a guide to Mitel's capabilities in SLIC design and manufacture. A menu of customer requirements is outlined within the following pages.

By the options detailed, please fill in all of the relevant information and requirements for your slic function. Upon receipt of the details, Mitel will be able to assess the feasibility and propose technical solutions tailored to your needs.

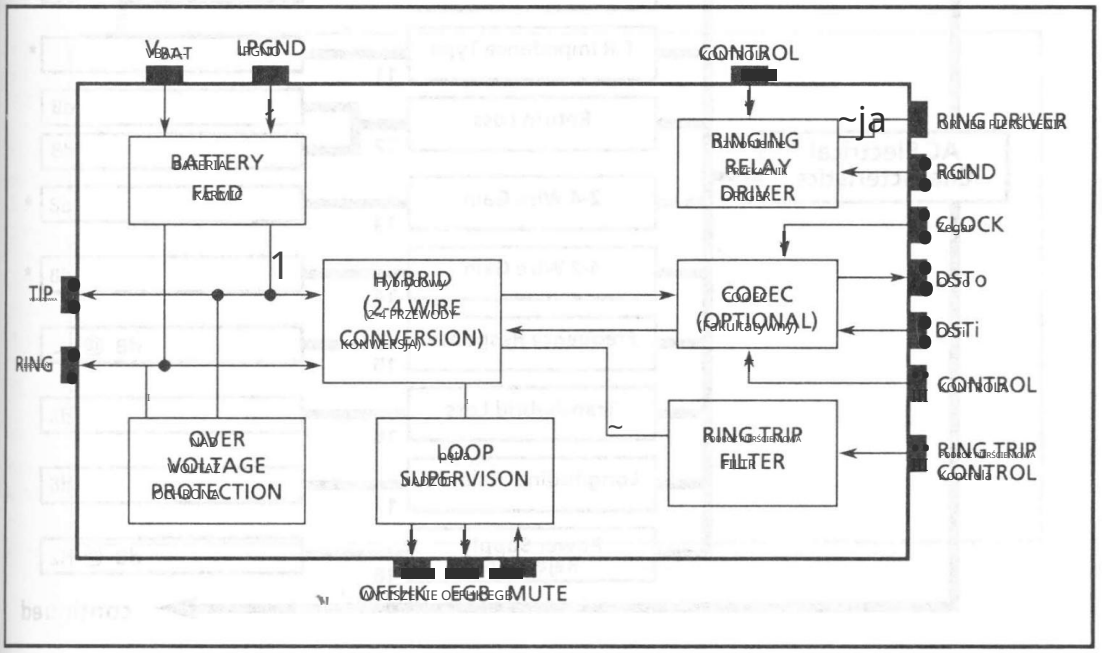

Figure 1. Functional Block Diagram

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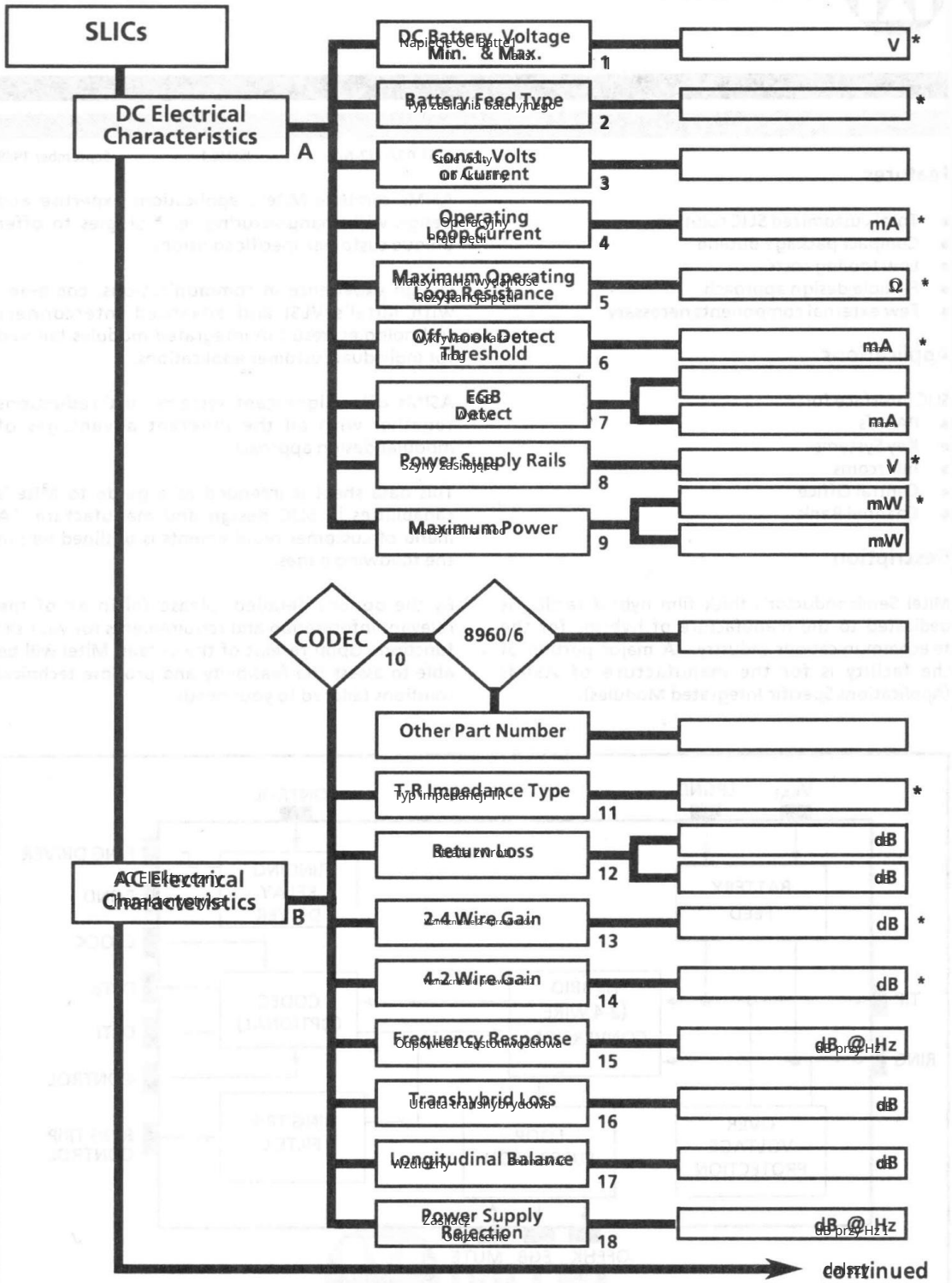

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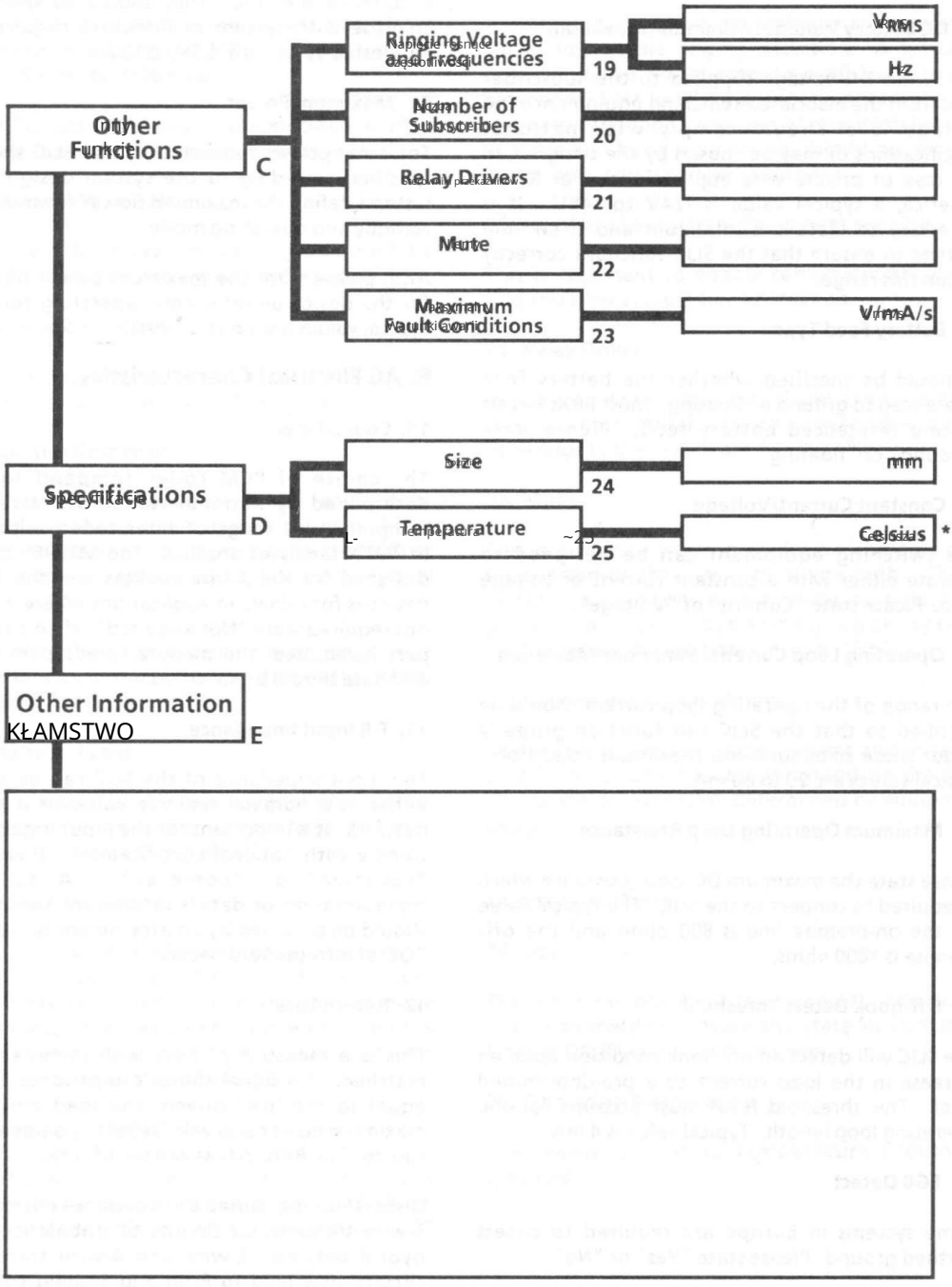

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Functional Description
Opis funkcjonalny

A. DC Electrical Characteristics
A. Charakterystyki elektryczne prądu stałego

1. DC Battery Voltage: Minimum/Maximum
1. Napięcie baterii DC: minimalne/maksymalne

This is the DC voltage supplied to the subscriber loop from the associated switching equipment. The voltage level should comply with national specifications or may be chosen by the designer, in the case of private wire applications. For North America a typical value is -24V to -48V. It is necessary to state the minimum and maximum voltage to ensure that the SLIC functions correctly within this range.
To jest napięcie DC dostarczane do pętli abonenckiej z powiązanego sprzętu przełączającego. Poziom napięcia powinien być zgodny z krajowymi specyfikacjami lub może zostać wybrany przez projektanta w przypadku zastosowań z prywatnymi przewodami. W Ameryce Północnej typowa wartość wynosi od -24V do -48V. Należy podać minimalne i maksymalne napięcie, aby mieć pewność, że urządzenie SLIC będzie działać poprawnie w tym zakresie.

2. Battery Feed Type
2. Typ zasilania baterii

It should be specified whether the battery feed is referenced to ground or floating. Most PBXs have a ground referenced battery feed. Please state "ground" or "floating".
Należy określić, czy zasilanie baterii jest odniesione do ziemi, czy pływające. Większość PBX ma zasilanie baterii odniesione do ziemi. Proszę podać „uziemienie” lub „pływające”.

3. Constant Current/Voltage
3. Stały prąd/napięcie

The switching equipment can be designed to operate either with a constant current or voltage feed. Please state "Current" or "Voltage".
Sprzęt przełączający może być zaprojektowany do pracy z zasilaniem stałym prądem lub napięciem. Proszę podać „Prąd” lub „Napięcie”.

4. Operating Loop Current: Minimum/Maximum
4. Prąd pętli roboczej: minimalny/maksymalny

The range of the operating loop current should be specified so that the SLIC can function properly under these minimum and maximum conditions. Typical values are 20 to 60 mA.
Zakres prądu pętli roboczej powinien być tak określony, aby SLIC mógł prawidłowo działać w tych minimalnych i maksymalnych warunkach. Typowe wartości to 20 do 60 mA.

5. Maximum Operating Loop Resistance
5. Maksymalna rezystancja pętli roboczej

Please state the maximum DC loop resistance which is required to connect to the SLIC. The typical value for the on-premise line is 800 ohms and the off-premise is 1800 ohms.
Proszę podać maksymalną rezystancję pętli DC, która jest wymagana do podłączenia do SLIC. Typowa wartość dla linii lokalnej wynosi 800 omów, a poza lokalną 1800 omów.

6. Off-hook Detect Threshold
6. Próg wykrywania połączenia telefonicznego

The SLIC will detect an off-hook condition upon an increase in the loop current to a pre-determined level. This threshold level must account for the operating loop length. Typical value is 4 mA.
SLIC wykryje stan odłączenia słuchawki po zwiększeniu prądu pętli do wcześniej określonego poziomu. Ten poziom progowy musi uwzględniać długość pętli roboczej. Typowa wartość to 4 mA.

7. EGB Detect
7. Wykrywanie EGB

Some systems in Europe are required to detect earth ground. Please state "Yes" or "No".
Niektóre systemy w Europie są wymagane do wykrywania uziemienia. Proszę podać „Tak” lub „Nie”.

The EGB (Earth Ground Button) detect threshold determines the difference in current flowing in the Tip lead and Ring Lead indicating an activation of the Earth Ground Button. A typical value is 20 mA.
EGB (przycisk uziemienia) wykrywa próg, który określa różnicę prądów płynących w przewodzie końcówki i przewodzie pierścieniowym, wskazując aktywację przycisku uziemienia. Typowa wartość to 20 mA.

8. Power Supply Rails
8. Szyny zasilające

These are required to supply voltage to the internal circuitry of the SLIC. They should be specified to coincide with system architecture requirements. Suggested values are ±5V, ±12V.
Są one wymagane do dostarczania napięcia do wewnętrznych obwodów SLIC. Powinny być określone tak, aby odpowiadały architekturze systemu. Sugerowane wartości to 5 V i 12 V.

9. Maximum Power
9. Maksymalna moc

The total power consumed by the SLIC should be specified according to the system design. Some systems define the maximum power consumption in standby and operating mode.
Całkowita moc pobierana przez SLIC powinna być określona zgodnie z projektem systemu. Niektóre systemy definiują maksymalne zużycie energii w trybie gotowości i pracy.

Also, please state the maximum power dissipation for the device under normal operating conditions. Typical values are up to 2 watts.
Proszę również podać maksymalną moc rozpraszaną dla urządzenia w normalnych warunkach pracy. Typowe wartości wynoszą do 2 watów.

B. AC Electrical Characteristics
B. Charakterystyki elektryczne prądu przemiennego

10. Codec/Filter
10. Kodek/filtr

The choice of PCM codec companding law is determined by national standards. Mitel has a comprehensive range of filter codecs within their MT89XX family of product. The MT8965 has been designed for the A-law markets and the MT8960 device is for μ-law. In applications where a codec is not required state "Not Required". If an alternative part is required, the manufacturer's part number and data should be specified.
Wybór kompresji kodeka PCM określony jest przez normy krajowe. Mitel ma kompleksową gamę kodeków filtrów w swojej rodzinie produktów MT89XX. MT8965 został zaprojektowany dla rynków A-law, a urządzenie MT8960 jest przeznaczone dla μ-law. W zastosowaniach, w których kodek nie jest wymagany, należy określić „Nie wymagane”. Jeśli wymagana jest alternatywna część, należy podać numer części i dane producenta.

11. T-R Input Impedance
11. Impedancja wejściowa T-R

The input impedance of the SLIC can be specified either as a nominal resistive value or a complex network. It is important for the input impedance to comply with national specifications. Please state "resistive" or "complex". A schematic representation or details or relevant specifications should be provided by an attachment or within the "Other Information" section.
Impedancja wejściowa SLIC może być określona jako nominalna wartość rezystancyjna lub złożona sieć. Ważne jest, aby impedancja wejściowa była zgodna z krajowymi specyfikacjami. Proszę podać „rezystancyjne” lub „złożone”. Schemat ideowy lub szczegóły lub odpowiednie specyfikacje należy dostarczyć w załączniku lub w sekcji „Inne informacje”.

12. Return Loss
12. Strata powrotna

This is a measure of how well impedances are matched. If a signal source's impedance is exactly equal to the driven impedance, the load will absorb maximum power and will "reflect" no power to the source. The Return Loss will be infinite.
Jest to miara dopasowania impedancji. Jeśli impedancja źródła sygnału jest dokładnie równa impedancji obciążenia, obciążenie będzie pochłaniać maksymalną moc i nie będzie odbijać mocy do źródła. Strata powrotna będzie nieskończona.

Discontinuities caused by impedance mismatches in 2-wire transmission circuits or unbalances in the hybrid between 2-wire and 4-wire transmission circuits, may lead to Echo and Singing conditions. Return Loss may be more accurately defined in terms of Echo Return Loss (ERL) and Singing Return Loss (SRL) as follows:
Nieciągłości spowodowane niedopasowaniem impedancji w dwuprzewodowych obwodach transmisyjnych lub asymetrią w hybrydzie pomiędzy dwuprzewodowymi a czteroprzewodowymi obwodami transmisyjnymi, mogą prowadzić do powstawania warunków echa i śpiewania. Dokładniej można zdefiniować stratę powrotną w kategoriach straty powrotnej echa (ERL) i straty powrotnej śpiewu (SRL) w następujący sposób:

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Echo Return Loss (ERL) is a weighted average of the return loss over the frequency range 500 Hz and 2500 Hz.

Singing Return Loss (SRL) is the lower value of the average return losses in the 200 Hz to 500 Hz band, and the 2500 Hz to 3200 Hz band.

ERL and SRL loss requirements are specified in dB as measured in a specified reference impedance.

13. 2-Wire-to-4-Wire Gain

This is the T-R system gain and should be specified as part of the loss plan for the system.

14. 4-Wire-to-2-Wire Gain

This is the system gain from T-R and should be considered in conjunction with the above.

15. Frequency Response

The operational bandwidth template required for the interface is to accommodate 300 Hz to 3400 Hz generally to the level measured at 1000 Hz. Typical values are ±0.1 dB relative to the loss measured at 1000 Hz. A typical value is ±0.1 dB.

The template should also detail any tone rejection. All tone rejections should be specified in the "other information" section.

16. Transhybrid Loss

This is a measure of the return signal power from the input pair to the output pair of the same 4-wire interface. A typical value is 20 dB.

17. Longitudinal Balance

This is a measure of the degree of balance between the two sides of a 2-wire circuit. Improper longitudinal balance results in power common mode rejection and produces a net voltage between the two sides, generating metallic noise audible to the user. A typical value is 53 dB at 3000 Hz.

18. Power Supply Rejection

This is the ability of the interface to prevent any ripple noise signal present on the power supply rails from entering the transmission path. Typical value is 30 dB.

C. Other Functions

19. Ringing Voltages and Frequencies

It is necessary to specify in minimum and maximum values for reliable ringing detection. A typical 2-type ringing in North America is 40 Vrms to 150 Vrms at 15.3 Hz to 68.0 Hz superimposed on -56.5 V battery voltage. Any special requirements, such as pulse and burst suppression, should be detailed in the "other information" section.

20. Number of Subscriber Equipment per Line

This is important to enable correct design of the ringing waveform filter and off-hook detection.

21. Relay Drivers

In line card design, the relay driver can be used to turn on the external relay to connect the ringing generator to the line. State "Yes" or "No".

22. Mute

This is a feature which provides an analog signal suppression of the 2-wire to 4-wire path. This is useful in applications such as music on hold, tone generation, etc., depending upon system configuration. Please state "Yes" or "No".

23. Maximum Fault Condition

This is the maximum voltage, current and duration of a fault condition that can be withstood by the SLIC. The conditions would be determined by equipment design.

D. Specifications

24. Size

The maximum physical size allowed for the device should be specified. Please also state SIL (Single-In-Line) or DIL (Dual-in-Line) package.

25. Operating Temperature

The normal operating temperature should be specified.

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E. Inne informacje

Tutaj należy podać wszelkie inne szczegóły, które pomogą pracownikom firmy Mitel w przygotowaniu propozycji projektu SLIC. Zazwyczaj pomocna jest znajomość projektu systemu i jego zastosowania.

***Uwaga**

Aby pomóc w ocenie wymagań interfejsu, opcje oznaczone gwiazdką (*) MUSZĄ zostać zaznaczone. Pozostałe opcje są wymienione w celu zilustrowania możliwości Mitel Custom SLIC. Wiele funkcji ma wartości domyślne, które będą nieodłączną cechą projektu.

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Custom CO Trunk Interface

9161-002-128-NA Issue 1 September 1989

Features

- Total customized trunk interface solution
- Compact package outline
- Low cooling costs
- Flexible design approach
- Few external components necessary

Applications

Interface for:

- PABXs
- Key Systems
- Intercoms
- Central Office
- Channel Bank

Description

Mitel Semiconductor's thick film hybrid facility is dedicated to the manufacture of hybrids for the telecommunications industry. A major portion of the facility is for the manufacture of ASIMs (Application Specific Integrated Modules).

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Design experience in communications combined with Mitel's advanced connect technologies result in integrated modules tailored for individual customer applications.

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This data sheet is intended as a guide to Mitel's capabilities in trunk interface design and manufacture. A menu of customer requirements is outlined within the following pages.

By the options detailed, please fill in all of the relevant information and requirements for your line interface function. Upon receipt of the details, Mitel will be able to assess the feasibility and propose technical solutions tailored to your needs.

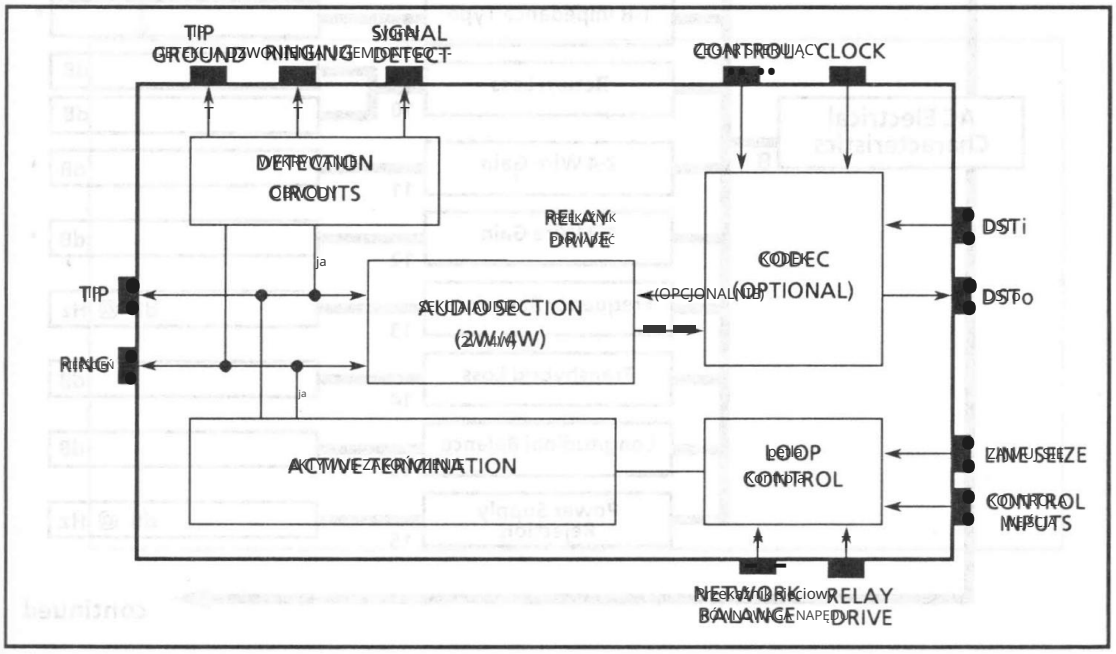

Figure 1 - Functional Block Diagram

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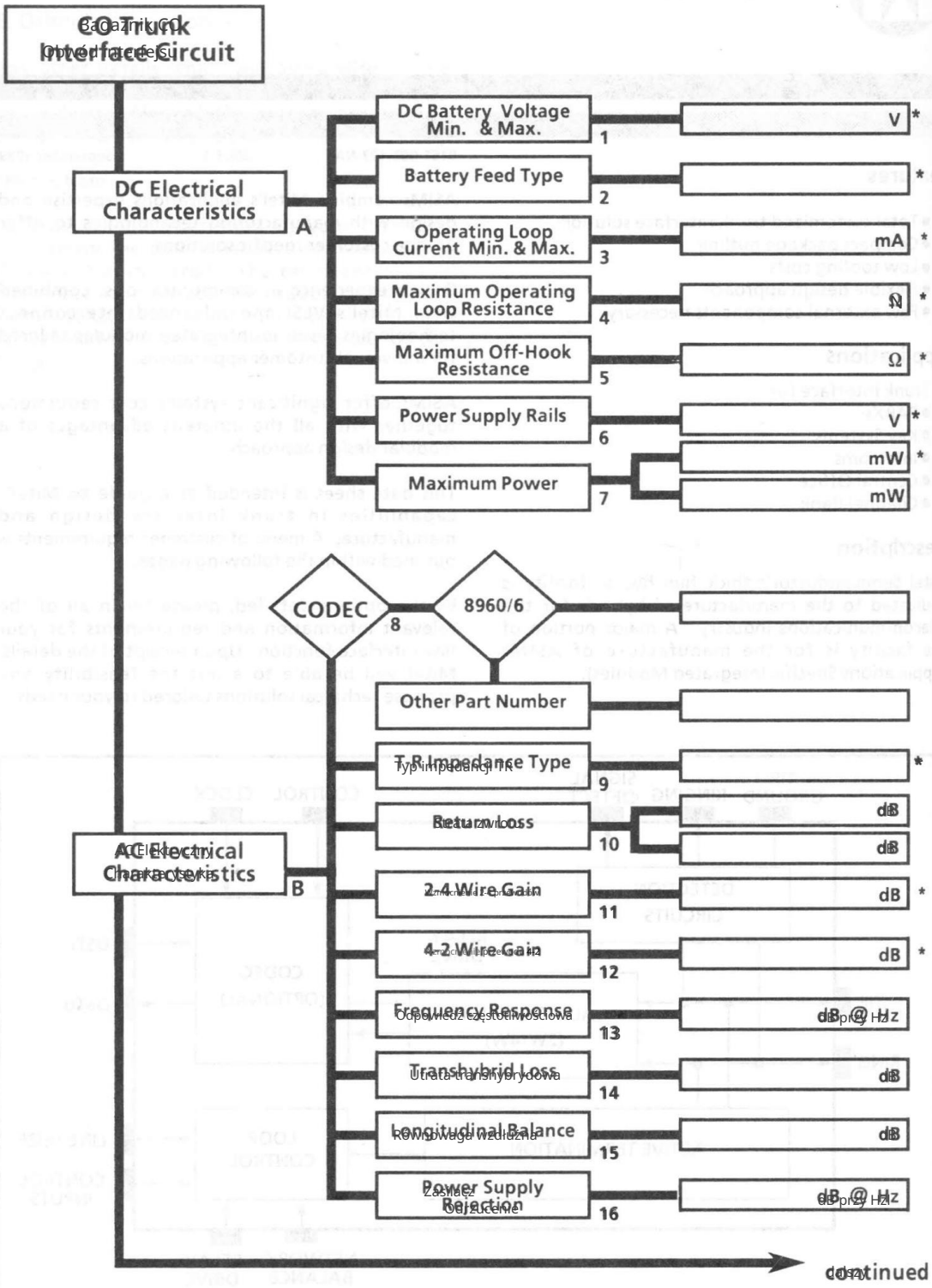

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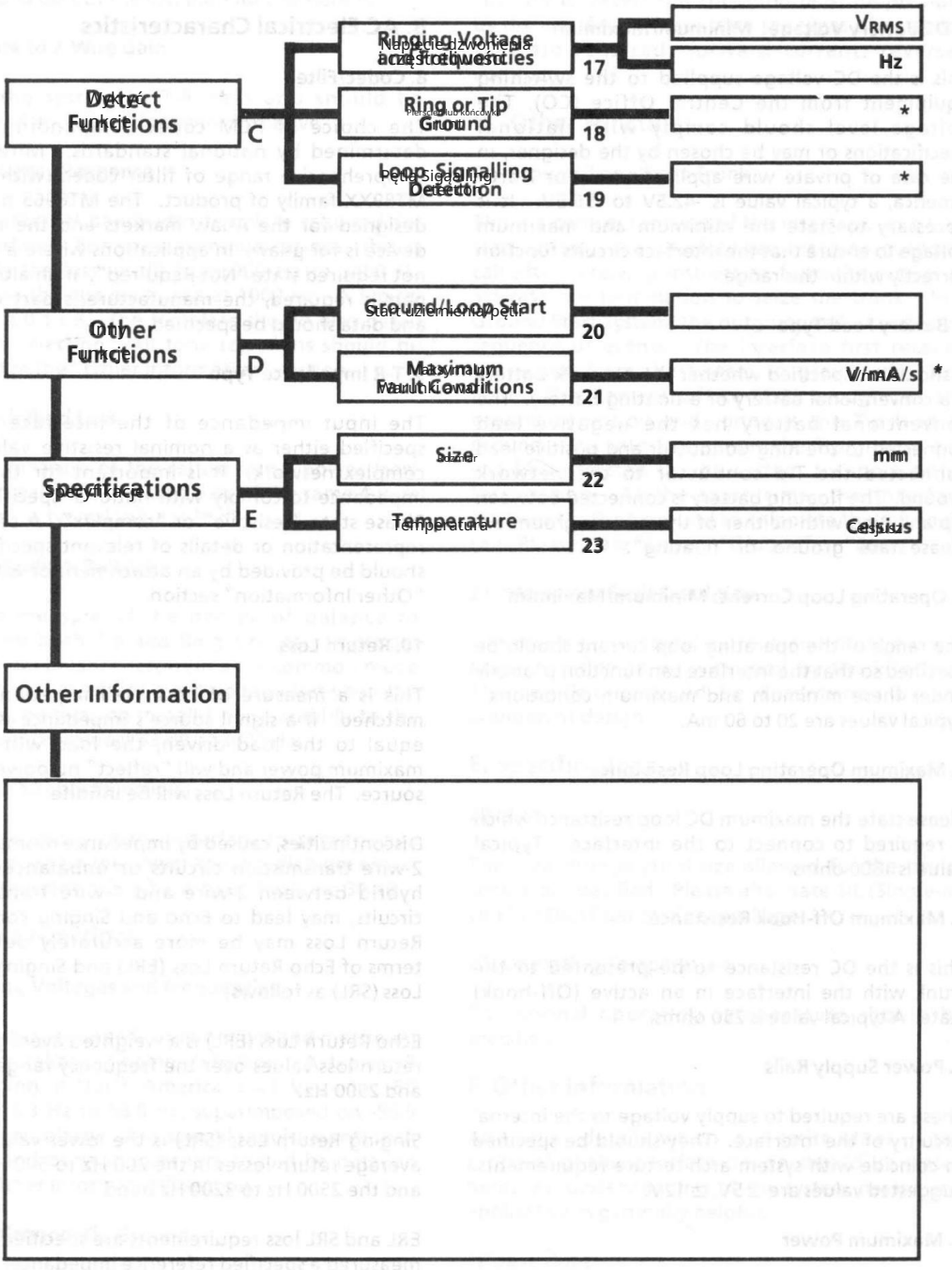

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OPIS FUNKCJONALNY

A. Charakterystyka elektryczna DC

1. Napięcie baterii DC: minimalne/maksymalne

Jest to napięcie DC dostarczane do urządzeń przełączających z Centrali (CO). Poziom napięcia powinien być zgodny ze specyfikacjami krajowymi lub może zostać wybrany przez projektanta. W przypadku zastosowań z prywatnymi przewodami. W Ameryce Północnej typowa wartość wynosi od -42,5 V do -56,5 V. Konieczne jest określenie minimalnego i maksymalnego napięcia, aby zapewnić prawidłowe funkcjonowanie obwodów interfejsu w tym zakresie.

2. Typ zasilania bateryjnego

Należy określić, czy akumulator sieciowy jest akumulatorem konwencjonalnym czy akumulatorem pływającym. W akumulatorze konwencjonalnym przewód ujemny jest podłączony do przewodu pierścieniowego, a przewód dodatni jest podłączony do przewodu końcówki do uziemienia sieci. Akumulator pływający jest podłączony między końcówką a pierścieniem, przy czym żaden z tych przewodów nie jest uziemiony. Proszę podać „na ziemi" lub „pływający".

3. Prąd pętli roboczej: minimalny/maksymalny

Należy określić zakres roboczego prądu pętli, aby interfejs mógł prawidłowo funkcjonować w tych minimalnych i maksymalnych warunkach. Typowe wartości wynoszą od 20 do 60 mA.

4. Maksymalna rezystancja pętli roboczej

Proszę podać maksymalną rezystancję DC loop, która jest wymagana do połączenia z interfejsem. Typowe wartości wynoszą 1800 omów.

5. Maksymalny opór przy podniesionej słuchawce

Jest to rezystancja DC, która ma być przedstawiona magistrali, gdy interfejs jest w stanie aktywnym (odłączonym). Typowa wartość to 250 omów.

6. Szyny zasilające

Są one wymagane do dostarczania napięcia do wewnętrznych obwodów interfejsu. Powinny być określone tak, aby odpowiadały wymaganiom architektury systemu. Zalecane wartości to ±5V, ±12V.

7. Maksymalna moc

Całkowita moc pobierana przez interfejs powinna być określona zgodnie z projektem systemu. Niektóre systemy definiują maksymalne zużycie energii w trybie gotowości i pracy.

Proszę również podać maksymalną moc rozpraszania dla urządzenia w normalnych warunkach. Typowe wartości to do 2 watów.

B. Charakterystyka elektryczna prądu zmiennego

8. Kodek/Filtr

Wybór prawa kompresji kodeka PCM jest określany przez normy krajowe. Mitel ma kompleksowy zakres kodeków filtrujących w swojej rodzinie produktów MT89XX. MT8965 został zaprojektowany dla rynków A-law, a urządzenie MT8960 jest przeznaczone dla μ-law. W zastosowaniach, w których kodek nie jest wymagany, należy wpisać „Niewymagane". Jeśli wymagana jest alternatywna część, należy określić numer części i dane producenta.

9. Typ impedancji T-R

Impedancja wejściowa interfejsu może być określona jako nominalna wartość rezystancyjna lub sieć złożona. Ważne jest, aby impedancja wejściowa była zgodna ze specyfikacjami krajowymi. Proszę podać „resistive" lub „complex". Schematyczne przedstawienie lub szczegóły odpowiednich specyfikacji powinny być dostarczone w załączniku lub w sekcji „Other Information".

10. Strata zwrotna

Jest to miara tego, jak dobrze impedancje są dopasowane. Jeśli impedancja źródła sygnału jest dokładnie równa impedancji obciążenia, obciążenie pochłonie maksymalną moc i nie „odbije" żadnej mocy do źródła. Strata odbicia będzie nieskończona.

Nieciągłości spowodowane niedopasowaniem impedancji w obwodach transmisyjnych 2-żyłowych lub brak równowagi w hybrydowych pomiędzy obwodami transmisyjnymi 2- i 4-żyłowymi, może powodować powstawanie echa i śpiewania. Stratę odbiciową można dokładniej zdefiniować w kategoriach straty odbiciowej echa (ERL) i straty odbiciowej śpiewu (SRL) w następujący sposób:

Strata odbicia echa (ERL) to średnia ważona wartości strat odbicia w zakresie częstotliwości 500 Hz i 2500 Hz.

Strata odbiciowe (SRL) to niższa wartość średnich strat odbiciowych w paśmie od 200 Hz do 500 Hz i od 2500 Hz do 3200 Hz.

Wymagania dotyczące strat ERL i SRL są określone w dB, mierzone przy określonej impedancji odniesienia.

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11. 2-Wire to 4-Wire Gain

This is the T-R to system gain and should be specified as part of the loss plan for the system.

12. 4-Wire to 2-Wire Gain

This is the system to T-R gain and should be considered in conjunction with the above.

13. Frequency Response

The operational bandwidth template required for the interface. For voice communications, this is generally the loss, in dB from 300 Hz to 3400 Hz relative to the loss measured at 1000 Hz. A typical value is ± 0.1 dB. The template should also detail any tone rejection. All tone rejections should be specified in the "Other Information" section.

14. Transhybrid Loss

This is a measure of the return signal power from the input pair to the output pair of the same 4-wire interface. A typical value is 20 dB.

15. Longitudinal Balance

This is a measure of the degree of balance to ground for both Tip and Ring circuits. Improper longitudinal balance results in poor common mode rejection and produces a net voltage between the two sides, generating metallic noise audible to the user. A typical value is 53 dB at 3000 Hz.

16. Power Supply Rejection

This is the ability of the interface to prevent any ripple or noise on the power supply rails from entering the transmission path. A typical value is 30 dB.

C. Detect Functions

17. Ringing Voltages and Frequencies

It is necessary to specify minimum and maximum values for reliable ringing detection. A typical B type ringing in North America is 40 V_{RMS} to 150 V_{RMS} at 15 Hz to 68.0 Hz, superimposed on -56.5 V battery voltage. Any special requirements such as pulse and burst suppression should be detailed in the "Other Information" section.

18. Ring Ground/Tip Ground

If ground start signalling is used in the network it may be necessary to detect a ground condition on either, or both wires. Please state "Tip", "Ring" or "Both".

19. Loop Signalling Detection

If the network uses reverse battery signalling, circuitry to detect this condition must be provided by the interface. Please state the types of detection that are required: forward current, reversed current.

D. Other Functions

20. Ground/Loop Start Trunk

This is a control function of the interface. In loop start system, the interface can make an outgoing call after receiving instruction from the system to activate the termination to seize the trunk. In a Ground Start System, the outgoing call is made by a sequence of events. The interface first receives instruction from the system to ground the Ring lead. The Central Office (CO) recognizes the ground condition and connects the Tip lead to ground. The interface senses the Tip ground and will be instructed by the system to apply active termination. At the same time, the interface removes the Ring ground to complete the outgoing call. Please state "Loop" "Ground" or "Both".

21. Maximum Fault Condition

The maximum voltage, current and duration of a fault condition, that can be withstood by the interface. The conditions would be determined by the equipment design.

E. Specifications

22. Size

The maximum physical size allowed for the device should be specified. Please also state SIL (Single-in-Line) or DIL (Dual-in-Line) package.

23. Operating Temperature

The normal operating temperature should be specified.

F. Other Information

Any other details which will assist Mitel in the proposal of the interface design should be stated here. An understanding of the system design and application is generally helpful.

Please Note

To assist in the assessment of your interface requirements, the options labelled with an asterisk (*) **MUST** be answered. The other options are referenced to

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Custom CO Trunk Interface

illustrate the capability of Mitel Custom CO Trunk Interface Circuits. Many of the functions have default values which will be an inherent feature of the design.

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DIGITAL SWITCHES

PRZEŁĄCZNIKI CYFROWE

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Product Summary

Digital Switches

November 1989

Product Family

MT8980D	Digital Switch
MT8981D	Digital Switch
MT8982	Small Digital Switch
MT9080	SMX™ Switch Matrix Module
MT9085	PAC™ Parallel Access Circuit

Applications

- Digital PBX and LCTS
- Central office switches/Digital Cross Connects
- T1/CEPT multiplexor
- Digital loop carrier
- ST-BUS™ controller

Key Features

MT8980/81

- Non-blocking digital switches
- Low power CMOS
- 256/128 channel capacity (64 kb/s)
- 8 or 4 2 mb/s serial ST-BUS inputs/outputs
- Parallel microprocessor interface
- Patented message broadcast capabilities

MT8982

- 64 channel capacity
- 2 serial input/output streams - 2mb/s max.
- Serial microprocessor interface
- Small size 16 pin package

MT9080

- Flexible building block for >500 line switches
- Data memory and connect memory modes
- 16 bit wide parallel interface
- 16 MHz maximum clock rate
- Per channel single or double buffering

MT9085

- Serial-to-parallel, parallel-to-serial companion chip for SMX
- 32/16 serial inputs to 8 bit parallel interface
- 1024 channel capacity
- 2 mb/s, 4 mb/s serial rates

Description

The MT8980 provides simultaneous time slot switching capabilities for up to 256/128 64 kb/s channels. Data interface to the device is via 8 serial inputs and outputs operating at 2 mb/s. The MT8980 also provides microprocessor read/write access to individual ST-BUS channels, providing access to the control and status information of other Mitel ST-BUS components.

The MT8981 is identical to the MT8980 but provides the switching capabilities for four serial input and output streams (128 channels).

The MT8982 MiniDX is a low cost time switch providing simultaneous connections for up to 64 kb/s channels, in two serial input and output streams. Control interface to the device is via a microprocessor port.

The MT9080 Switch Matrix Module (SMX) is a flexible memory module suitable for construction of large digital switches. It can be configured as either Connection Memory (CM) or Data Memory (DM). Connection Memory operation allows the MT9080 to be used in 16 bit wide parallel bus, with clock rates up to 16 MHz.

SMX is optimized for use in applications larger than 500 lines. The basic configuration of two SMX's (1 DM, 1 CM) will handle switching of up to 1024 16 bit words in either a low delay single-buffered, or double-buffered configuration. Larger size matrices can be constructed with multiple MT9080s.

The MT9085 Parallel Access Circuit (PAC) provides an interface between 2/4 mb/s serial architectures and parallel SMX interface. It provides eight serial to parallel (or parallel to serial) conversion between 32 serial streams and an 8 bit wide parallel bus. Additionally, it provides relevant SMX timing signals from ST-BUS timing signals.

Package Options

MT8980D	C,E	40 pin
	P	44 pin
MT8981D	C,E	40 pin
	P	44 pin
MT8982	C,E	16 pin
	S	16 pin
MT9080	P	84 pin
MT9085	P	68 pin

Note: C=CerDIP, E=SideBrazeDIP, P=PDIP, S=SOIC

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PRIMARY RATE INTERFACES

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Product Summary

Primary Rate Interfaces

November 1989

Product Family

T1 (1.544 mb/s)

- MH89750 T1 Framer & Interface
- MT8976 T1/ESF Framer Circuit
- MH89760 T1/ESF Framer & Interface
- MH89761 T1 Transmit Equalizer

CEPT (2.048 mb/s)

- MT8978 CEPT PCM 30 Framer Circuit
- MH89780 CEPT PCM 30 Framer & Interface
- MT8979 CEPT PCM 30/CRC-4 Framer
- MH89790 CEPT PCM 30/CRC-4 Framer & Interface
- MH89791 CEPT PCM 30 Transmit Equalizer

Applications

- T1/CEPT Multiplexor
- PBX
- Central Office Switches
- Digital Loop Carrier
- Primary Rate ISDN

Key Features

- Selectable framing/line codes
  - MT8976/8979/89760/89790 D3/D4, ESF, B8ZS, AMI
  - MT8978/89780 CRC-4, HDB3, AMI
- 2 Frame elastic buffer with 32 µs jitter buffer
- Insertion/Detection of A,B,C,D signalling bits with optional debounce
- Frame/multiframe sync, Tx and Rx
- Pin compatible devices between T1 and CEPT devices
- Per channel loopback and remote loopback
- Performance monitoring capability

Description

The MT8976 provides a simple interface to DS1 transmission links. All of the framing and signalling insertion and detection is done by the device. Various programmable options in the MT8976 include D3/D4 or ESF framing, ZCS or B8ZS line code suppression, alarms and, local and remote loopback.

The MH89760 is a hybrid module which encompasses the MT8976 plus additional line interface and clock recovery circuitry. The MH89750 provides the same functionality, except for ESF.

The MT8979 is a CEPT digital trunk framing circuit operating at 2.048 kb/s. It provides such features as frame and multiframe word insertion and detection, generation of synchronization patterns, optional cyclical redundancy check and far end error performance reporting, HDB3 decoding and optional coding, channel associated or common channel signalling, programmable digital attenuation and a 2 frame received elastic buffer.

The MT8978 is a first generation framer, providing similar features to the MT8979, with the exception of the CRC-4 error check.

The MH89790 is a hybrid module which encompasses the MT8979 plus additional line interface and clock recovery circuitry.

The MT8976 and MT8979, as well as the MH89760 and MH89790 are pin compatible with each other, providing considerable flexibility in addressing both North American and CEPT applications.

The MH89761 and MH89791 provide programmable, 1200 ohm impedance equalization for T1 and CEPT requirements respectively.

Package Options

MT8976	C,E	28 pin
	P	44 pin
MT8978	C	28 pin
MT8979	C,E	28 pin
	P	44 pin
MH89750	DIL Hybrid	40 pin
MH89760	DIL Hybrid	40 pin
MH89761	SIP Hybrid	20 pin
MH89780	DIL Hybrid	40 pin
MH89790	DIL Hybrid	40 pin
MH89791	SIP Hybrid	20 pin

Note: C = CerDIP P = PLCC S = SOIC

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BASIC RATE INTERFACES

STAWKA PODSTAWOWA

INTERFEJS

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November 1990

Product Family

MT8910	Digital Subscriber Line Interface Circuit (DSLIC)
MT8930	Subscriber Network Interface Circuit (SNIC)
MT8971B/72B	MT8971 Digital Subscriber Interface Circuit (DSIC) MT8972 Digital Network Interface Circuit (DNIC)
MT8972A	Digital Network Interface Circuit
MH89726/728	MT8972 Loop Extender Circuits

Applications

- Digital subscriber lines
- PBX digital sets and line cards
- ISDN NT1/NT2
- ISDN LAN's
- Digital multiplexors and concentrators
- Pair gain/line doubler/s
- High speed limited distance modems

Key Features

- Common ST-BUS system interface
- Low power CMOS, single 5V supply

MT8910

- Compatible with ISDN U-Interface standard
- Full duplex transmission over twisted pair
- High performance 2B1Q line code
- Over 5.5km loop range at 160kbps
- Full activation state machine

MT8930

- Compatible with ISDN S-Interface standard
- Full duplex 2B + D, 192 kbps transmission
- Point-to-point, point-to-multipoint and star configuration
- Selectable NT/TE modes of operation
- On-chip HDLC
- No crystal required (on-chip PLL/VCO)

MT8972

- Full duplex, biphase line code transmission over single twisted pair
- Up to 5km at 80kbps and 4km at 160kbps
- ISDN 2B + D compatible format
- Selectable master/slave modes of operation
- Transparent modem capability
- Extended temperature range with MT8972B

MT8971B

- Similar features as the MT8972 but with shorter loop range - up to 3.0km at 80kbps and 160kbps

MH89726/728

- Extends transmission performance of the MT8972
- Over 6km at 80kbps on 24AWG twisted pair

Description

The MT8910 (DSLIC) provides the ISDN basic rate access at the U-Interface. Full duplex digital transmission at 160 kbit/s on single twisted pair is achieved using 2B1Q line code and echo cancellation technology. Complies with all loop length requirements as defined by ANSI T1.601 1988.

The MT8930 (SNIC) is an ISDN Basic Rate S and T interface, compatible to CCITT I.430. Provides point-to-point and point-to-multipoint 2B + D transmission up to 1km over 2 twisted pairs. Includes HDLC protocoller and Motorola/Intel compatible microport.

The MT8972 (DNIC) is a full duplex, bi-phase line code transceiver using echo cancellation technique enabling up to 5km loop performance over twisted pairs. Data rates of 80 and 160 kbit/s are supported in the "transparent modem" or "2B + D" operation. For greater flexibility, the MT8972B offers extended temperature range operation and additional control features.

The MT8971 has features similar to the MT8972 but with loop performance of approximately 3.0 km over twisted pair. A perfect choice for applications with no line length demands but still requiring high quality, cost effective, error and noise immune transceiver functions.

The MH89726 (160kbps) and MH89728 (80kbps transmission) are thick film hybrid circuits that may be used to extend the loop range capability of the MT8972. Over 6km can be achieved at 80kbps and over 5km at 160kbps.

Package Options

MT8910	C,D	28 pin
MT8930	C,E	28 pin
MT8971B	E	22 pin
MT8972A/72B	C,E	22 pin
MT8972A/72B	P	28 pin
MH89726/728	SIL Hybrid	10 pin

Note: C = CerDIP D = Sidebraze E = PDIP P = PLCC S = SOIC

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Product Summary

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RATE ADAPTORS

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Product Summary

Rate Adaptors

November 1990

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Product Family

MH89500	R-Interface Module (RIM)
MT8950	Data Codec

Applications

- Featured telephone sets
- Integrated Voice/Data terminals
- Digital PBX/KTS
- Terminal adaptors

Key Features

- ST-BUS compatible
- Low power CMOS
- Single 5 Volt supply
- Loopback and test modes

MH89500

- Implements ISDN R-Interface function
- Rate adapts to basic rate B and D channels
- User selectable synchronous and asynchronous data rates
- V.24, X.20 and X.21 terminal interfaces
- Compatible with V.110 and ECMA 102 recommendations

MT8950

- Transparent coding and decoding of 0 to 8, 9.6 and 19.2 kbps data
- Rate adapts to 56kbps or 64kbps basic rate channel

Description

The MH89500 (RIM) implements the ISDN R-Interface terminal adaptor function. The RIM will rate adapt V.24 (RS-232 type), X.20 and X.21 terminal interfaces to basic rate B and D channels. It is compatible with V.110 and ECMA 102 recommendations and handles both asynchronous and synchronous data rates from 50 bps to 19.2 kbps.

The MT8950 data codec uses the position encoded modulation technique to transparently encode/decode low speed data to and from a 56kbps or 64kbps channel. It can accept either asynchronous or synchronous data up to 8kbps, 9.6kbps and 19.2kbps. The MT8950 is a low cost solution to interface RS-232C type terminals to basic rate channel in, for example, digital PABX applications.

Package Options

MH89500	DIL Hybrid	40 pin
MT8950	C	24 pin

Note: C = CerDIP D = Sidebraze C = CDIP P = PDIP P = PLCC S = SOIC

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CODEC AND DIGITAL PHONE COMPONENTS

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Product Summary

Codec and Digital Phone Components

November 1990

Product Family

MT8960/61/62/63/64/65/66/67	Integrated PCM Filter/Codec
MT8993/3B	Digital Telephone with HDLC (H-Phone)
MT8994/5B	Digital Telephone (D-Phone)

Applications

- Basic to fully featured telephone sets
- Integrated Voice/Data terminals
- Cellular radio sets
- Digital PBX/KTS
- Channel banks/multiplexers

Key Features

- ST-BUS compatible
- Low power CMOS
- Loopback and test modes

MT8896X

- Integrated single chip transmit/receive filters and PCM Codec
- Meets AT&T D3/D4 and CCITT G.711 and G.712 specifications
  - µ-Law: MT8960/2/4/6
  - A-Law: MT8961/3/5/7
- Digital Coding Options
  - MT8964/5/6/7 CCITT Code
  - MT8960/1/2/3 Alternative Code
- Programmable filter gains
- ± 5V supplies

MT899X

- Integrated single chip digital telephone circuit
- µ-Law and A-Law versions
- Programmable receive gain
- DTMF/tone generator and tone ringer
- Speakerphone operation
- On-chip transducer interfaces
- X.25 Level 2 HDLC formatting (MT8992/3B only)
- Single 5V supply

Description

The MT896X family consists of A-Law and µ-Law integrated single chip filter/codecs. All are fully compliant with D3/D4 and G.711/712 specifications and offer independently accessible filters with programmable gain adjustments. Up to six uncommitted scan/drive ports are available to simplify system design.

The MT8994/5B (D-Phone) is a highly integrated digital phone IC which combine either an A-Law or µ-Law filter/codec with all basic telephony functions and interfaces to permit the design of a fully featured digital telephone using a minimum of components. To simplify the set design, speakerphone operation, DTMF/tone and ringing generations and programmable gain control are all included on chip as is a Motorola/Intel compatible microprocessor port. It is also easily interfaceable to any of Mitel's basic rate transceivers (DNIC, DSLIC and SNIC) through the ST-BUS to offer 2B + D connectivity. The D-Phone operates on only a single 5 Volt supply and its low power consumption provides the set designer the option of line power feeding.

The MT8992/3B (H-Phone) is a further enhancement of the D-Phone. In addition to all the features of the MT8994/5B, the H-Phone includes a fully integrated X.25 HDLC data formatter. Digital set design has never been simpler!

Package Options

MT8960/1	E	18 pin
MT8964/5	C,E	18 pin
MT8962/3	E	20 pin
MT8962/3/6/7	S	20 pin
MT8992/3,4/5B	C	40 pin

Note: C = Ceramic DIP E = Plastic DIP P = PLCC S = SOIC

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COMMON CONTROL PRODUCTS

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November 1990

Product Family

MT8920/ MT8920-1	ST-BUS Parallel Access Circuit
MT8940	T1/CEPT Digital Trunk PLL
MT8941	Advanced T1/CEPT Digital Trunk PLL
MT8952B	HDLC Protocol Converter

Applications

- T1/CEPT multiplexor
- PBX
- Central office
- Digital loop carrier
- ISDN

Key Features

MT8920

- High speed parallel access to ST-BUS
- Access time MT8920 - 80ns - MT8920
  120ns - MT8920-1
- Flexible interrupts

MT8940

- Supplies 1.544 and 2.048 MHz clock, phase-locked to an 8 kHz reference signal

MT8941

- Supplies 1.544, 2.048 and 4.096 MHz clocks phase-locked to an 8 kHz reference signal
- Pin compatible to MT8940
- Typical output jitter 0.07UI from 2 Hz to 40 kHz

MT8942

- Provides 512 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz and 8.192 MHz clocks phase-locked to an 8 kHz reference signal
- Selectable clock and frame pulse output ST-BUS or GCI mode
- Typical output jitter 0.04 UI from 2 Hz to 40 kHz

MT8952

- Formats as per X.25 level 2 standard
- Send and receive 19 byte FIFO
- ST-BUS and Motorola microprocessor interface

Description

The MT8920 provides a simple interface between Mitel's ST-BUS and parallel system environments.

It can be used to provide parallel data interfaces to various Mitel basic and primary rate components. Additionally, the MT8920 can be used as a parallel control interface to the MT8976/79 instead of using an MT8980 digital switch.

The MT8940 is a dual digital phase locked loop providing the timing and synchronization signals for the T1 or CEPT transmission links and the ST-BUS. The first PLL provides the T1 clock (1.544 MHz) synchronized to the input frame pulse at 8 kHz. The timing signals for the CEPT transmission link or the ST-BUS are provided by the second PLL locked to an internal or an external 8 kHz reference signal.

The MT8941 is an advanced T1/CEPT digital trunk phase locked loop that is a pin compatible variant of the MT8940 featuring enhanced jitter performance. The device also provides timing and synchronization signals for T1 or CEPT transmission links and the ST-BUS, all locked to an 8 kHz reference signal.

The MT8952 HDLC Protocol Controller frames and formats data packets according to X.25. This single channel device has a 19 byte FIFO and provides a parallel access to the ISDN D-channel, or any other applications requiring HDLC functionality.

Package Options

MT8920/-1	C, E, P	28 pin
MT8940	C, E	24 pin
MT8941	E, P	24, 28 pin
MT8952B	C, E, P	28 pin

Note: C = CerDIP D = Sidebraze E = PDIP P = PLCC S = SOIC

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SOFTWARE

OPROGRAMVVARE

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Product Family

MS6000 MS6050	IES ISDN EXPRESS™ Evaluation Software
MS6010 MS6060	ISDN EXPRESS LAPD
MS6020 MS6070	ISDN EXPRESS Call Control

Applications

- ISDN Voice and Data Workstations
- ISDN application software development platform
- ISDN protocol monitoring
- ISDN protocol conversion

Key Features

- Implementation of data link entity as defined by CCITT Q.921
- Written in Kernighan & Ritchie C programming language
- Conformance Testers
- Test Drivers
- Device Drivers
- ISDN Workstation Demonstration
- Demonstrated on Basic Rate and Primary Rate ISDN EXPRESS products
- Operating System Independence

Description

MS6000/MS6050 is the object and source code for the ISDN EXPRESS Evaluation System. An application for this software is test development using the development product hardware.

MS6010/MS6060 Mitel's ISDN EXPRESS LAPD is an ISDN Software Development Tool Kit for Q.921 applications. It is designed to make the implementation of ISDN applications D-Channel processing requirements quick and easy.

MS6020/MS6070 Mitel's ISDN EXPRESS Call Control is an ISDN Development Tool Kit implementing Q.931 and call control for AT&T and Northern Telecom switches; additional switches will be added.

The ISDN EXPRESS Call Control, LAPD, Physical Entities and Card provide users most of the building blocks for an ISDN system. All that is required is the environment and the application.

Ordering Information

MS6000	IES Object Code
MS6010	ISDN EXPRESS LAPD Object Code
MS6010-EV1.0	ISDN EXPRESS LAPD Evaluation Package
MS6020	ISDN EXPRESS Call Control Object Code
MS6020-EV1.0	ISDN EXPRESS Call Control Evaluation Package
MS6050	IES Source Code
MS6060	ISDN EXPRESS LAPD Source Code
MS6070	ISDN EXPRESS Call Control Source Code

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DEVELOPMENT/OEM PRODUCTS

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Development/OEM Products

November 1990

Product Family

MB89000C	The ISDN EXPRESS™ Card
MB89010	ISDN EXPRESS DSLIC Card
MB89050	ISDN EXPRESS RIM Card
MB60XX	ISDN EXPRESS Ancillary Components

Applications

- ISDN component evaluation
- ISDN system emulation
- Communications interface for voice processing systems
- Hardware/Software development system
- Test system

Key Features

- Component evaluation and Hardware/Software development system
- ISDN system emulation
- Comprable with Multi-Vendor Integration Protocol (MVIP™) PC interconnection Standard
- IBM PC/XT/AT™ 286/386 plug in cards support basic rate, primary rate and support components
- Eases familiarization with standard interfaces
- Menu driven software with full size display window for each component
- Help facility for all major system functions and component registers

Description

MB89000 The ISDN EXPRESS Card is an evaluation platform for a broad range of ISDN components. These include ISDN EXPRESS LAPD Software, T-1, CEPT, SNIC, DNIC, Digital Phone, Digital Switch, HDLC and DPLL. The ISDN EXPRESS Card has an MVIP compatible interface.

MB89010 The ISDN EXPRESS DSLIC Card is a PC Card that operates as a stand alone card or in conjunction with other ISDN EXPRESS Cards. It provides an evaluation platform for the HMP Digital Switch and the DSLIC which is the "U"-interface device. The MB89010 is MVIP compatible.

MB89050 The ISDN EXPRESS RIM Card operates in conjunction with The ISDN EXPRESS Card. It provides an evaluation platform for the RIM which is the "R"-interface device. The MB89050 is MVIP compatible.

MB60XX ISDN EXPRESS Ancillary Components are used to assist in evaluating and designing with Mitel products. The Ancillary Components include handset, speakerphone enclosure, and a variety of transformers, crystals and inductors.

Ordering Information

MB89000C	The ISDN EXPRESS Card
MB89010	ISDN EXPRESS DSLIC Card
MB89050	ISDN EXPRESS RIM Card
MB60000	ISDN EXPRESS Speakerphone
MB60001	ISDN EXPRESS Handset
MB60010	T-1 MH89760 Magnetics Kit
MB60012	DNIC Accessory Kit
MB60013	MT8940 Crystal Oscillator Kit
MB60014	RIM Crystal Kit
MB60016	75Ω CEPT/MH89790 Magnetics Kit
MB60017	120Ω CEPT/MH89790 Magnetics Kit
MB60022	MT8941 Crystal Oscillator Kit
MB60024	DSLIC Accessory Kit (Low inductance)

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APPLICATION NOTES

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Applications of the MT8804 8 X 4 Analog Switch Array

Zastosowania MT8804 8 X 4 Analogowy Układ Przełączający

ISSUE 1 August 1982

WYDANIE 1 Sierpień 1982

Contents

- The MT8804 in detail
- Modular line interface circuit
- DTMF Receiver tester control circuit
- Test equipment switching system
- 4-Channel 4-bit D/A converter
- Programmable attenuator
- Multi output programmable frequency divider
- MT8804 status indicator

Zawartość

- MT8804 w szczegółach
- Modułowy obwód interfejsu liniowego
- Obwód sterujący testerem odbiornika DTMF
- System przełączania sprzętu testowego
- 4-kanałowy przetwornik cyfrowo-analogowy 4-bitowy
- Programowalny tłumik
- Wielowyjściowy programowalny dzielnik częstotliwości
- Wskaźnik stanu MT8804

Introduction

The constant trend in electronic design is towards circuits which minimize power and space requirements while improving on the performance characteristics of the predecessors. The field of analog switching is no exception to this design strategy. The Mitel MT8804A CMOS 8 x 4 Analog Switch Array is a micropower device which replaces several CMOS MSI packages and meets the stringent specifications required in analog switching systems. The 8 x 4 array configuration and minimal interchannel crosstalk make the MT8804A ideal for crosspoint switching applications. This application note provides both functional and parametric details of the device that would normally be required in designing the MT8804A into such systems. A series of application circuits and descriptions is presented to further illustrate the use and versatility of the MT8804A in communications and other more general areas.

Wstęp

Stałym trendem w projektowaniu elektroniki jest tworzenie obwodów, które minimalizują wymagania dotyczące mocy i przestrzeni, jednocześnie poprawiając charakterystyki wydajności poprzedników. Dziedzina przełączania analogowego nie jest wyjątkiem od tej strategii projektowania. Mitel MT8804A CMOS 8 x 4 Analog Switch Array to urządzenie mikromocy, które zastępuje kilka pakietów CMOS MSI i spełnia rygorystyczne specyfikacje wymagane w systemach przełączania analogowego.

Dzięki konfiguracji 8 x 4 i minimalnemu międzykanałowemu przesłuchowi sprzęt MT8804A doskonale nadaje się do zastosowania przełączanie crosspoint. Niniejsza nota aplikacyjna zawiera zarówno szczegóły funkcjonalne, jak i parametryczne urządzenia, które normalnie byłyby wymagane przy projektowaniu MT8804A w takich systemach. Przedstawiono serię opisów aplikacji, aby lepiej zilustrować zastosowanie i wszechstronność MT8804A w komunikacji i innych bardziej ogólnych obszarach.

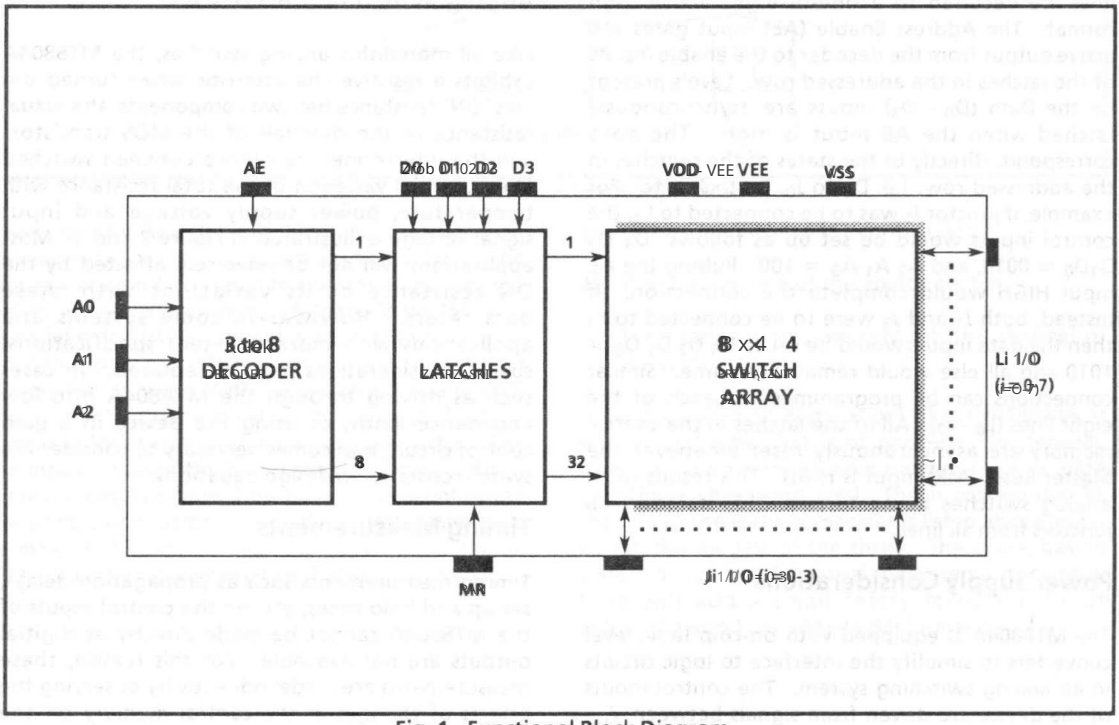

Fig. 1 - Functional Block Diagram

Rys. 1 - Schemat blokowy funkcji

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MT8804A w szczegółach

Konfiguracja i kontrola

32 przełączniki analogowe w układzie MT8804A są skonfigurowane w układzie 8 x 4, jak pokazano na rysunku 1. Osiem przełączników w każdej kolumnie jest podłączonych do złącza wejścia/wyjścia (Jo-J3), a podobnie cztery przełączniki w każdym rzędzie są podłączone do linii wejścia / wyjścia (Lo - L7). Każdy przełącznik krzyżowy zapewnia izolację lub transmisję między powiązaną linią a złączem. Stany przełączników są kontrolowane przez zestaw 32 zatrzasków ułożonych w układzie 8 x 4 odpowiadającym macierzy przełączników analogowych. Logiczny stan WYSOKI przechowywany w zatrzasku włącza odpowiedni przełącznik, podczas gdy stan NISKI wyłącza przełącznik. Dane są asynchronicznie zapisywane do zatrzasków sterujących, gdy wejście Address Enable (AE) jest WYSOKIE.

Wyjścia zatrzasków są bezpośrednio podłączone do wejść sterujących przełączników analogowych. To bezpośrednie połączenie powoduje „ciągły odczyt" pamięci sterującej (zatrzasków) przez przełączniki analogowe.

Zapis danych do pamięci sterującej odbywa się w taki sam sposób jak w przypadku standardowej pamięci o dostępie swobodnym. Jednakże, ponieważ nie są wymagane żadne sygnały sterujące odczytem, pamięć sterująca może być jednoznacznie traktowana jako pamięć tylko do zapisu. Osiem wierszy jest wybieranych przez trzy wejścia Address (Ao - A2). Sygnały na tych liniach są dekodowane do jednego z ośmiu aktywnych formatów wysokich. Wejście Address Enable (AE) bramkuje aktywne wyjście z dekodera do wejść enable zatrzasków w adresowanym wierszu. Poziomy obecne na wejściach Data (Do - D3) są asynchronicznie blokowane, gdy wejście AE jest wysokie. Dane odpowiadają bezpośrednio stanom przełączników w adresowanym wierszu, tj. Do do Jo, D, do J, itd. Na przykład, jeśli złącze J miałoby być podłączone do L4, wejścia sterujące byłyby ustawione następująco: D3 D2 D, Do = 0010, i A2 A, Ao = 100. Impulsowanie wejścia AE na WYSOKO zakończyłoby połączenie. Jeśli zamiast tego, zarówno J, jak i J3 miałyby być podłączone do L4, to wejścia danych byłyby ustawione na D3D2 D, Do = 1010, a wszystkie inne pozostałyby takie same. Podobne połączenia można zaprogramować dla każdej z ośmiu linii (Lo - L7). Wszystkie zatrzaski w pamięci sterującej są asynchronicznie resetowane, gdy wejście Master Reset (MR) jest na WYSOKO. Powoduje to wyłączenie wszystkich przełączników analogowych, izolując wszystkie złącza od wszystkich linii.

Rozważania dotyczące zasilania

MT8804A jest wyposażony w przetworniki poziomu logiki na chipie, aby uprościć interfejs do obwodów logiki w analogowym systemie przełączającym. Wejścia sterujące urządzenia są sterowane z sygnałów między Voo a Vss. Wszystkie wejścia sterujące są aktywne na poziomie WYSOKIM, przy czym Voo jest logicznym poziomem WYSOKIM, a Vss a logicznym poziomem NISKIM. Sygnały analogowe lub cyfrowe przełączane przez układ mogą się wahać między Voo i VEE.

Napięcia wejściowe zasilacza są zdefiniowane następująco:

5V.5Voo Vss :513V Cyfrowe
5V.5Voo VEE:513VAnalog
OV.5Vss VEE:58V Konwertery poziomu

Te napięcia definiują zakresy zasilania operacyjnego wejść cyfrowych i analogowych oraz przetworników poziomu logicznego. Podczas gdy zasilacze analogowe i cyfrowe mają identyczne limity, poziomy mogą być różne w danym zastosowaniu. Na przykład, prawidłowa konfiguracja zasilania jest następująca:

Voo = +5 V, Vss = OV i VEE = -6 V. Wejścia sterujące są zatem sterowane z układu logicznego CMOS 5 V, podczas gdy sygnały na liniach i złączach mogą wahać się od +5 V do -6 V. Należy zachować ostrożność, aby spełnić wszystkie trzy ograniczenia zasilania podczas podejmowania decyzji o konfiguracji zasilania. Poniżej przedstawiono przykład nieprawidłowego napięcia zasilania: Voo = +5 V, Vss = OV i VEE = -12 V. W tym przypadku Voo VEE = 17 V, co przekracza zakres zasilania analogowego.

Charakterystyka przełącznika analogowego

Podobnie jak wszystkie monolityczne przełączniki analogowe, MT8804A po włączeniu wykazuje charakterystykę rezystancyjną. Rezystancja „włączona" składa się z dwóch składników: rzeczywistej rezystancji kanałów tranzystorów MOS oraz rezystancji połączeń między przełącznikami. Potencjalna zmiana całkowitej rezystancji w zależności od temperatury, napięcia zasilania i napięcia sygnału wejściowego jest zilustrowana na rysunkach 2 i 3. Większość zastosowań nie będzie negatywnie dotknięta rezystancją ON ani jej zmianami w zależności od tych parametrów. Jednak w niektórych systemach i zastosowaniach o bardziej rygorystycznych specyfikacjach mogą być wymagane specjalne rozważania. W przypadkach takich jak sterowanie MT8804A w obciążeniach o niskiej impedancji lub używanie urządzenia w obwodzie sterowania wzmocnieniem, konieczne staje się uwzględnienie rezystancji przełącznika w równaniach projektowych.

Pomiary czasu

Pomiary czasowe, takie jak opóźnienia propagacji, czasy ustawiania i utrzymywania itp. na wejściach sterujących MT8804A nie mogą być wykonywane bezpośrednio, ponieważ wyjścia cyfrowe nie są dostępne. Z tego powodu pomiary te są wykonywane pośrednio, poprzez obserwację efektów zmian w pamięci sterującej na

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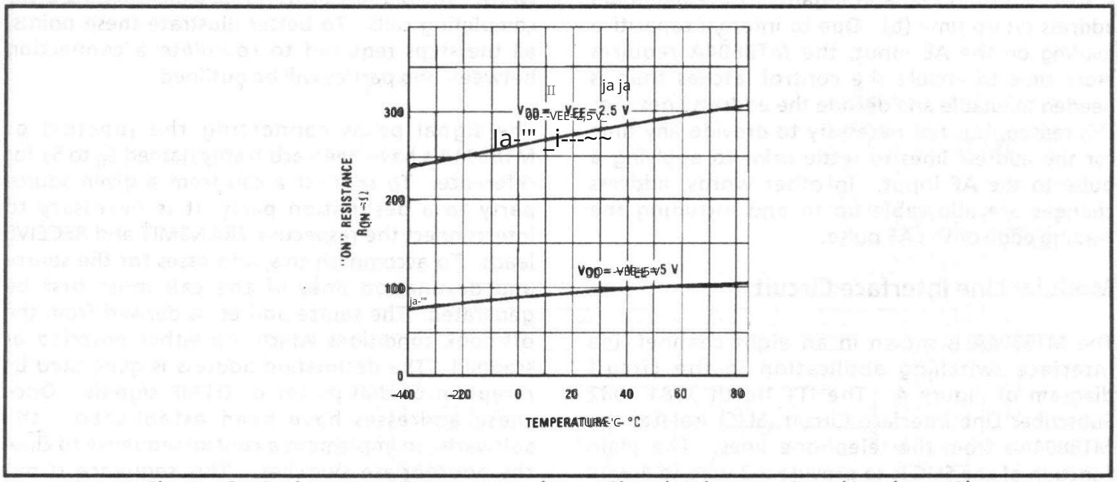

Fig. 2 - On Resistance vs Temperature (Input Signal Voltage = Supply Voltage/2)

Rys. 2 - Rezystancja włączenia w zależności od temperatury (napięcie sygnału wejściowego = napięcie zasilania/2)

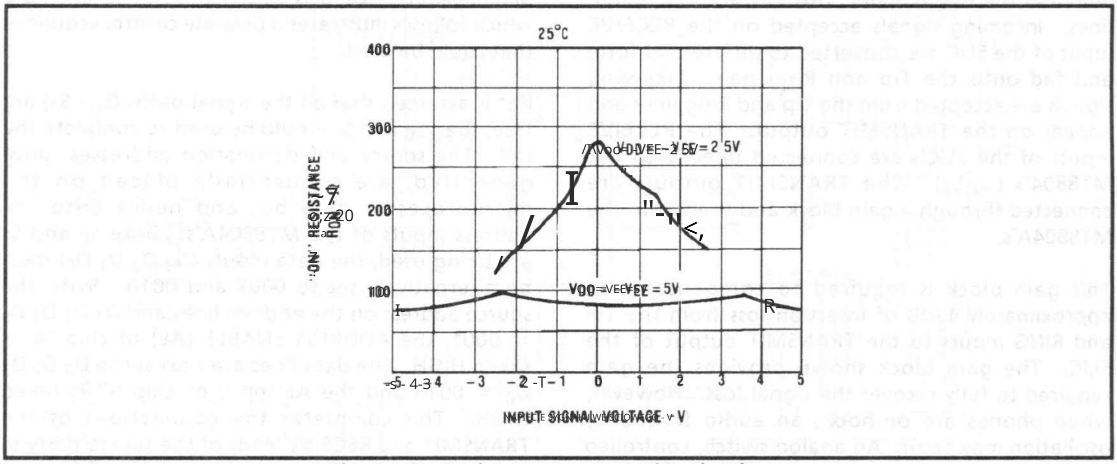

Fig. 3 On Resistance vs Input Signal Voltage

Rys. 3 W zależności od rezystancji napięcia sygnału wejściowego

states of the analog switches. For example, to measure t_{PAE}, the propagation delay from the address enable (AE) input to the signal output, the following steps are taken. A load circuit (500 Ω in parallel with 10K) is connected from a given junctor to ground (V_{SS}). One of the lines (L_0 - L_7) is connected to V_{DD}. With all switches initially OFF, the control inputs are set up to connect the load circuit to V_{DD} through the appropriate switch. The AE input is pulsed HIGH and the propagation delay time is measured from the 50% voltage point of the resulting signal across the load. In both cases time is measured from the leading edge of the signal. The actual time measured has three components.

1) The time to write to the control latch

2) The time to turn on the analog switch

3) The propagation time through the channel of the switch

In digital switching applications of the MT8804A, it is this total time which is of concern. In general, however, there is no need to write data into the latches [illegible] the first of the three components listed above and is by far the largest of the three. Therefore, basing system design on the total measurement of total time [illegible] margin of safety without sacrificing significant performance.

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Szczególną uwagę należy zwrócić na minimalne czas konfiguracji adresu (ts). Ze względu na wewnętrzny pojemnościowy ładowanie na wejściu AE, MT8804A wymaga więcej czasu na włączenie kontroli zatrzaski niż jest potrzebne do włączenia i zdekodowania linii adresowych. Z tego powodu nie ma potrzeby podawania żadnego czasu aby linie adresowe ustabilizowały się przed zastosowaniem impuls do wejścia AE. Innymi słowy, adres zmiany są dozwolone do i włącznie narastająca krawędź impulsu AE.

Modułowy obwód interfejsu liniowego

MT8804A jest pokazany w linii ośmiokanałowej Schemat przełączanie aplikacji w obwodzie diagram na rysunku 4. ITT North 3081/3082 Obwód interfejsu linii abonenckiej (SLIC) izoluje MT8804A z linii telefonicznych. Główny Funkcja SLIC to umożliwiająca przełączanie z 2 przewodów na 4 przewody konwersja między zbalansowanym TIP i RING linie i pojedyncze końce TRANSMISJI i ODBIORU linie. Sygnały przychodzące akceptowane na RECEIVE dane wejściowe SLIC are przekonwertowane na formę różnicową i podawane do pary Tip i Ring. Podobnie, sygnały są akceptowane z linii Tip i Ring oraz pojawiają się na wyjściu TRANSMIT. ODBIERZ Wejścia SLIC są podłączone bezpośrednio do MT8804 (L0-L7). Wyjścia TRANSMIT połączone przez blok wzmocnienia, a następnie do MT8804A.

Ten blok wzmocnienia wymaga około 17dB zrekompensować Do tłumienia wstawiania z TIP i wejścia RING do wyjścia TRANSMIT SLIC. Pokazany blok wzmocnienia zapewnia wzmocnienie wymagane do całkowitego odzyskania utraconego sygnału. Jednakże, gdy słuchawka telefonu jest odłożona, częstotliwość dźwięku może wystąpić oscylacja. Przełącznik analogowy sterowany za pomocą wyjścia wykrywania Switchhook SLIC, zmniejsza wzmocnienie prądu przemiennego do jedności, zapobiegając oscylacjom. Mały kondensator umieszczony wokół pętla sprzężenia zwrotnego eliminuje fałszywe sygnały o wysokiej częstotliwości oscylacja.

Kontrola sieci

Ogólnie rzecz biorąc, aby zakończyć rozmowę telefoniczną, należy wykonać to Systemu Konieczne jest podłączenie TRANSMISJI wyjście strony wywołującej do wejścia ODBIORU nazywana strona i odwrotnie. Tak więc dla każdego rozmowa telefoniczna, dwie ścieżki mowy, są wymagany. W konfiguracji pokazanej na rysunku 4, możliwe są cztery równoczesne rozmowy. Z wszystkie MT8804A resetują się, złącza (J_0 - J_3) są pływający i nie przypisany do żadnego konkretnego linia telefoniczna. W ten sposób złącze może być całkowicie sterowany przez oprogramowanie w systemie mikroprocesorowym, niezależnie od konkretnej linii telefonicznej przełączony. Oprogramowanie musi przechowywać zapis które skrzyżowania są w użyciu, a które są wolne kończące połączenia. Aby lepiej zilustrować te punkty, wszystkie kroki wymagane do nawiązania połączenia pomiędzy dwiema stronami zostaną nakreślone.

Ścieżki sygnałowe łączące układy MT8804A skrzyżowania zostały arbitralnie nazwane od S_0 do S_7. odniesienia. Aby połączyć call z danego źródła strona do strony docelowej, konieczne jest połączyć odpowiednie moduły TRANSMISJI i ODBIORU prowadzi. Aby to osiągnąć, adresy źródłowe i linie docelowe połączenia muszą być najpierw wygenerowany. Adres źródłowy jest pochodną stany odłączenia słuchawki, które są zakodowane jako zeskanowano. Adres docelowy jest generowany przez odbiór impulsów wybierania lub sygnałów DTMF. Po te adresy zostały ustalone, oprogramowanie może zaimplementować sekwencję kontrolną w celu zamknięcia odpowiednia sekwencja jest. Unikalny jak kolejność, w jakiej przełącza się MT8804A są zamknięte, nie jest krytyczna. Przykład poniżej przedstawiono możliwą sekwencję sterowania która można by wykorzystać.

Jeżeli przyjmiemy, że wszystkie ścieżki sygnałowe (S_0 - S_7) są bezpłatne, następnie S_0 i S_1 zostaną wykorzystane do uzupełnienia call. Adresy źródłowe i docelowe, once generowane, są umieszczane sekwencyjnie na magistrali danych mikroprocesora i stąd na adresy wejść MT8804A S_0 i S_1. są używane, dane wejściowe (D_3 D_2 D_1 D_0) muszą można ustawić alternatywnie na 0001 i 0010. W przypadku adres źródłowy w liniach adresowych D_3 D_2 D_1 D_0 = 0001 ADDRESS ENABLE (AE) układu scalonego „A" to wzięte WYSOKO. Linie danych są następnie ustawione na D_3 D_2 D_1 D_0 = 0010 i pobierane jest wejście AE układu scalonego „C" WYSOKI. To kończy połączenia TRANSMIT i RECEIVE strony źródłowej do S_0 i S_1 odpowiednio. Pozostaje tylko połączyć docelowy TRANSMIT prowadzi do S_1 i RECEIVE prowadzi do S_0, aby zakończyć połączenie dwukierunkowe. W tym celu należy ustawić adres docelowy na adresy wejść MT8804A. Linie danych są ponownie ustawione na D_3 D_2 D_1 D_0 = 0010 i wejście AE chip 'A' jest ustawiony na WYSOKO.

Na koniec, przy D_3 D_2 D_1 D_0 = 0001, wejście AE chip 'C' jest pulsowany wysoko. Łączy to TRANSMIT i ODBIERZ przewody linii adresowej do S_1 i S_0 odpowiednio w razie potrzeby. Wszystkie konieczne połączenia międzysieciowe są w ten sposób kompletne proces może swobodnie obsługiwać inne połączenia.

Aby rozłączyć połączenie telefoniczne, wykonaj następujące czynności: są podejmowane. Po zmianie stanu podniesionej słuchawki wykryto, adres z obwodów skanujących jest umieszczona na liniach adresowych i liniach danych są wszystkie

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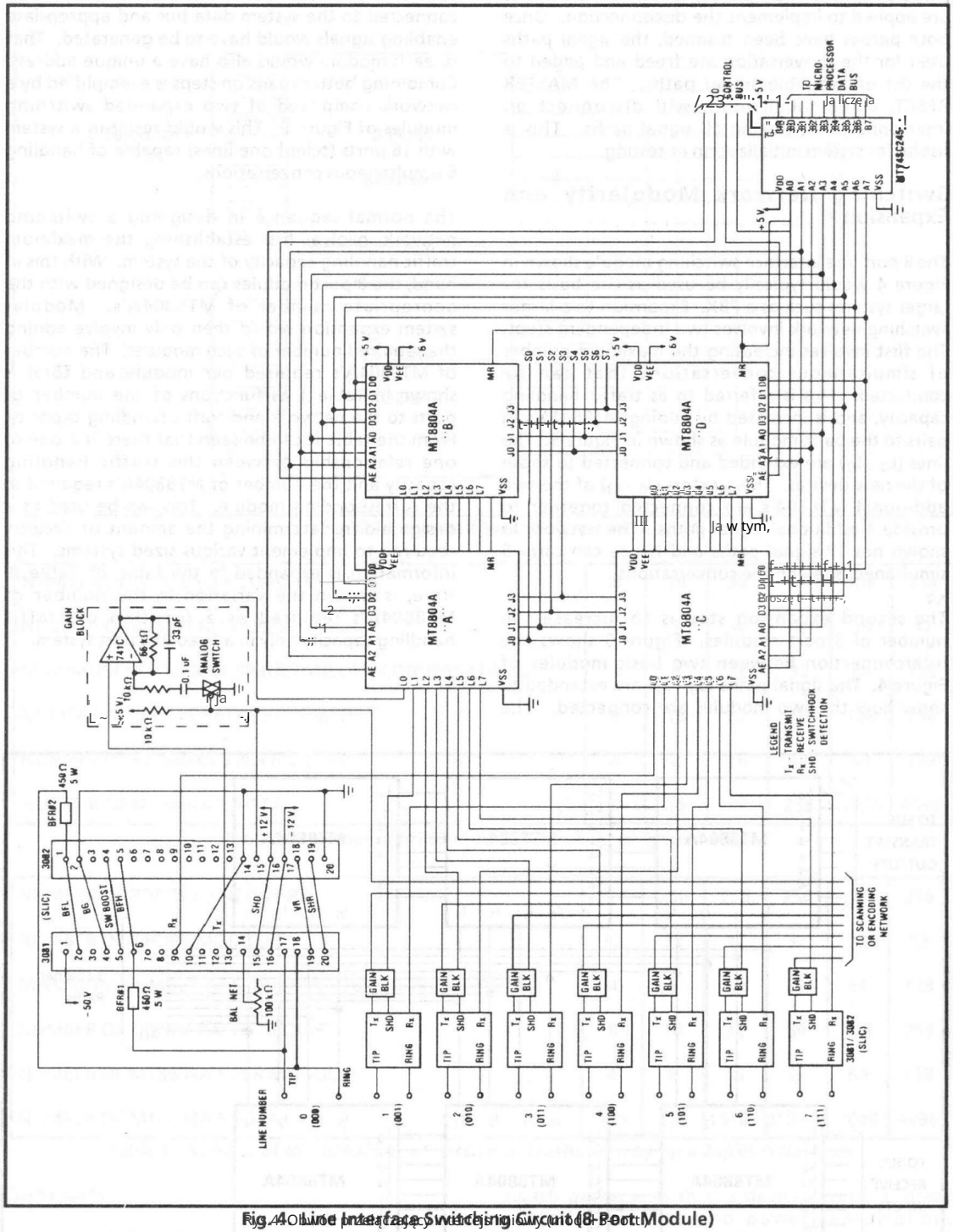

Fig. 4 Line Interface Switching Circuit (8-Port Module)

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set to zero. The appropriate Address Enable pulses are applied to implement the disconnection. Once both parties have been scanned, the signal paths used for the now vacated connection are freed and added to the list of available signal paths. The MASTER RESET will be taken high which will disconnect all interconnections, making all signal paths available for system initialization or testing.

Modularity and Expansion

The 8 port line interface switching module shown in Figure 4 is considered typical as the basis for larger systems such as a PBX. Expansion to a larger switching network involves two independent steps. The first involves increasing the maximum number of simultaneous conversations that can be conducted. This is referred to as traffic handling capacity and is increased by adding MT8804A's in pairs to the basic module as shown in Figure 5. The lines (L_7) are extended and connected to those of the new devices. The junctors (J_0 - J_3) of the two additional MT8804's are connected together to provide 4 additional signal paths. The network as shown has 12 signal paths and hence can carry 6 simultaneous telephone conversations.

The second expansion step involves increasing the number of 8 port modules. Figure 6 shows the interconnection between two basic modules of Figure 4. The signal paths (5) are extended to show how the two modules are connected. The control lines of each module (not shown) would be connected to the system data bus and appropriate enabling signals would have to be generated. That is, each module would also have a unique address. Combining both expansion steps is exemplified by a network comprised of two expanded switching modules (Figure 5). This would result in a system with 16 ports (telephone lines) capable of handling 6 simultaneous conversations.

The normal sequence in designing a switching network involves first establishing the maximum traffic handling capacity of the system. With this in hand, the number of ports can be designed with the appropriate MT8804A's. Modular system expansion would then involve adding the required number of such modules. The number of MT8804A's required per module and total is shown in Table 1 as a function of the number of ports to the network and traffic handling capacity. From the table it can be seen that there is a one to one relationship between this traffic handling capacity and the number of MT8804A's required in the corresponding modules. This can be used as a design aid in determining the amount of circuitry required to implement various sized systems. This information is expanded in the table of Table 2. Here it is shown how the number of MT8804A's required is a function of traffic handling capacity only in a fixed 256 port system.

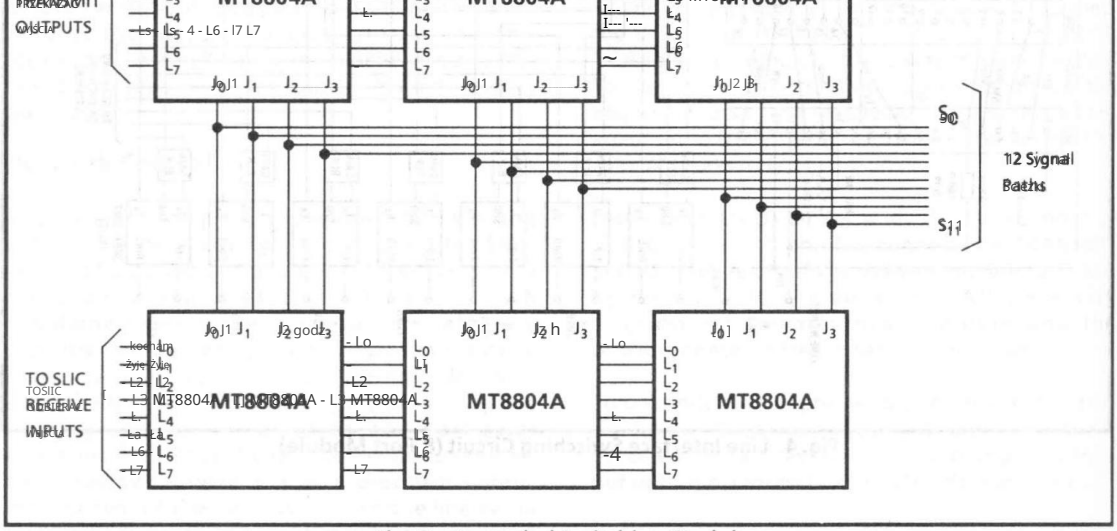

Fig. 5 Expanded Switching Module

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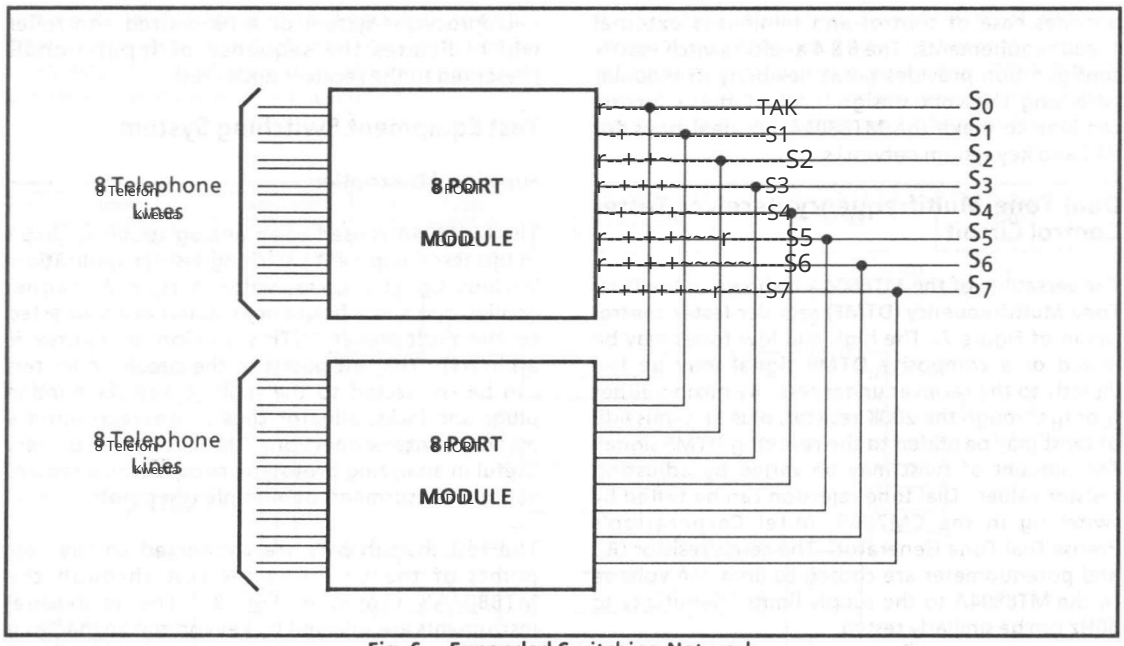

Fig. 6 - Expanded Switching Network

Rys6 - Rozszerzona sieć przełączająca

NUMBER OF PORTS TO NETWORK Liczba portów w sieci	8	16	32	64	128	256
NUMBER OF 8 PORT MODULES Liczba modułów 8 portów	1	2	4	8	16	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS Maksymalna liczba jednoczesnych rozmów	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED Liczba wymaganych ścieżek sygnałowych	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE Liczba MT8804A w module	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL Liczba MT8804A w całym systemie	4	16	64	256	1024	4096

Table 1 - Number of MT8804A's as a Function of System Size

Tabela 1 - Liczba MT8804A w zależności od rozmiaru systemu

NUMBER OF PORTS TO NETWORK Liczba portów w sieci	256	256	256	256	256	256
NUMBER OF 8 PORT MODULES Liczba modułów 8 portów	32	32	32	32	32	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS Maksymalna liczba jednoczesnych rozmów	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED Liczba wymaganych ścieżek sygnałowych	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE Liczba MT8804A w module	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL Liczba MT8804A w całym systemie	128	256	512	1024	2048	4096

Table 2 - Number of MT8804A's as a Function of Traffic Density for a 256 Port Network

Tabela 2 - Liczba MT8804A jako funkcja gęstości ruchu dla sieci 256 portowej

Summary

Using the MT8804A in line interface switching systems offers many advantages over conventional circuit elements. Replacing relays or smaller analog switch packages with this device results in great reductions in size and power consumption. Simultaneously a low level of interchannel crosstalk is maintained. The on-chip control memory with microprocessor compatible inputs

Streszczenie

Korzystanie z przełączania interfejsu liniowego MT8804A systemy oferują wiele zalet w porównaniu z konwencjonalnymi elementy obwodu. Wymiana przekaźników lub mniejszych przełączanie pakietów z tym urządzeniem daje świetne rezultaty redukcja rozmiarów i zużycie energii. jednocześnie niski poziom międzykanałowości przesłuch jest utrzymywany. kompatybilny z pamięć z mikroprocesorem układ sterujący wejścia

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provides ease of control and minimizes external circuit requirements. The 8 x 4 analog switch matrix configuration provides great flexibility in modular switching network design. All of these factors combine to make the MT8804A an ideal basic for PBX and key system networks.

Dual Tone Multifrequency Receiver Tester Control Circuit

The versatility of the MT8804A is shown in the Dual Tone Multifrequency (DTMF) receiver tester control circuit of Figure 7. The high and low tones may be mixed or a composite DTMF signal may be fed directly to the receiver under test. By mixing either f_L or f_H through the 200K resistor, plus or minus 6dB of twist may be added to the resulting DTMF signal. The amount of twist may be varied by adjusting resistor values. Dial tone rejection can be tested by switching in the CM7065, Mitel Corporation's Precise Dial Tone Generator. The series resistor (R_S) and potentiometer are chosen to limit the voltage to the MT8804A to the supply limits. Sensitivity to 60Hz can be similarly tested.

If the receiver under test has the facility to accept dial pulses, these may be generated by switching the power supplies in and out at the required rates. A single pole double throw relay, R1, is added to provide a switchable output impedance to simulate long line conditions. The relay drive is also switched by the MT8804A. The control of the MT8804A is provided by a stored test program in a microprocessor system or a hardwired controller which dictates the sequence of input signals presented to the receiver under test.

Test Equipment Switching System

Functional Description

The MT8804A is used as an analog coupling circuit in this test equipment switching system application. Various signal sources, voltmeters, a 2-channel oscilloscope and a frequency counter are connected to the multiplexer. (This section, of course is arbitrary). The test points of the circuit under test can be connected to the multiplexer via banana plugs and jacks, aligator clips or any appropriate means of interconnection. This circuit can be very useful in analyzing prototype circuits which require various measurments at multiple test points.

The test instruments are connected to the test points of the circuit under test through the MT8804A's as shown in Fig. 8. The individual instruments are selected by keys on the keypad as is the particular test point to which this equipment is connected. The system is operated as follows. First the 'TEST POINT' switch is pressed, followed by one of the numbered keys on the keypad. These correspond to the test points. Next, a sequence of keys designated the same as the test equipment is pressed. Finally the 'CONNECT' button is pressed. This completes the connection of the test equipment keyed in to the selected test point. This

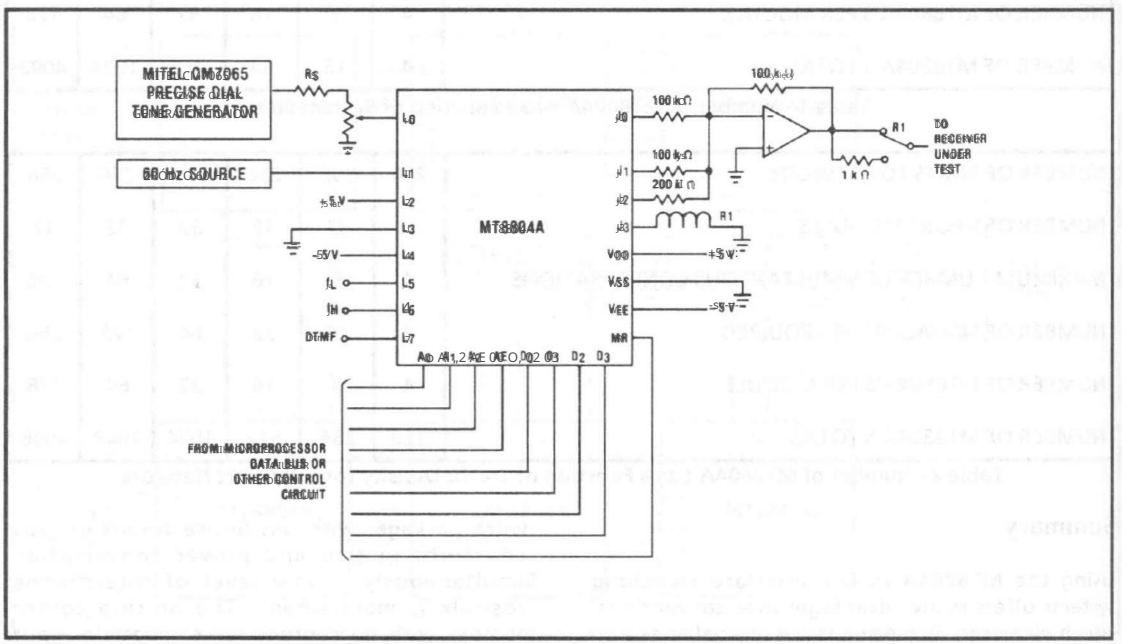

Fig. 7 DTMF Receiver Tester Control Circuit

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procedure can be repeated until each test point has been connected to all of the test instruments assigned. The signal sources may be simultaneously connected to any desired number of test points.

It is a simple matter to disconnect all of the test instruments from a given test point. This is accomplished by again pressing the "TEST POINT" switch, keying in the number corresponding to the appropriate test point, and then pressing the

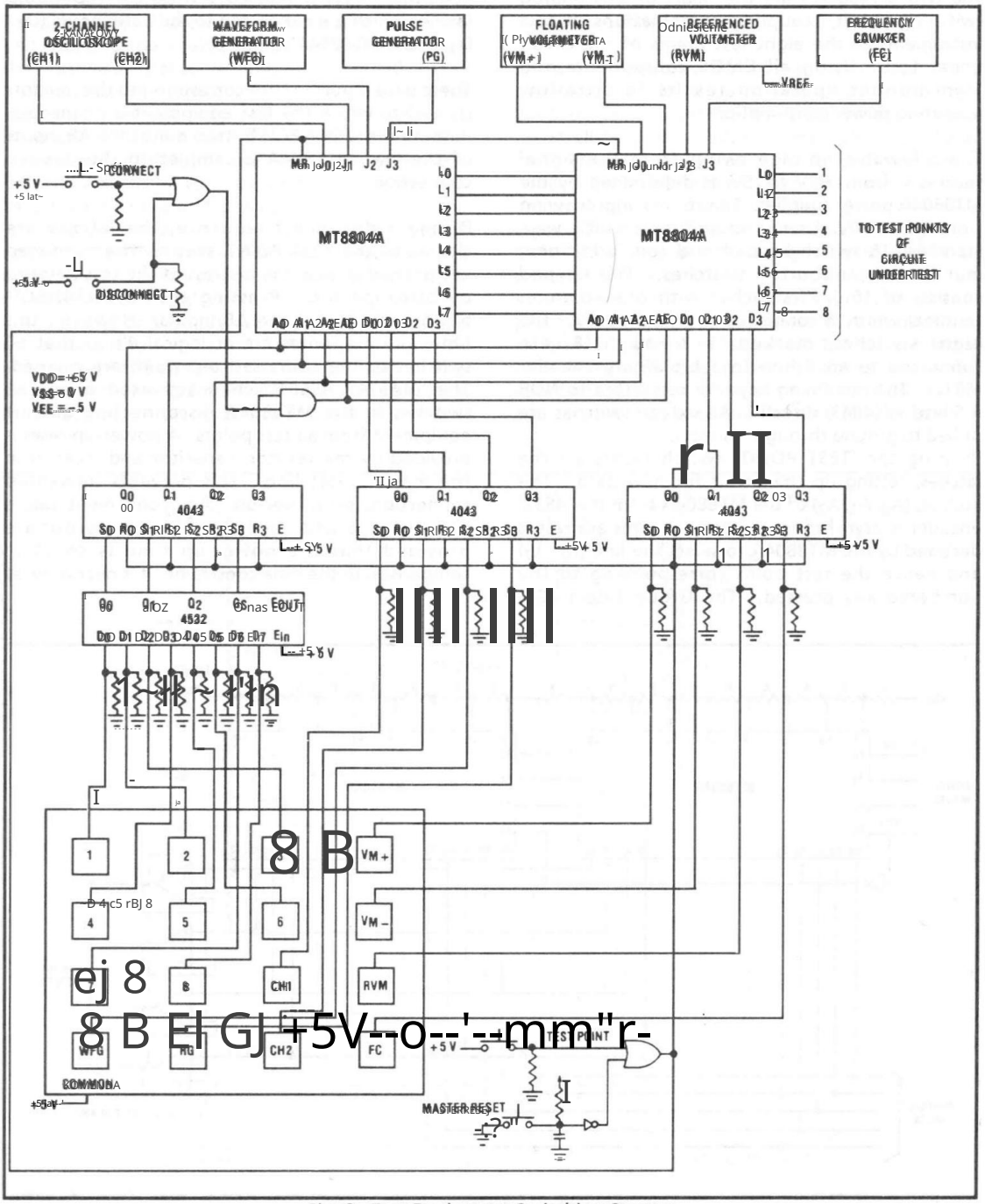

Fig 8. Test Equipment Switching System

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'DISCONNECT' button. Pressing the 'MASTER RESET' switch at any time disconnects all test instruments from all test points.

Przycisk „DISCONNECT" Naciśnięcie tego przycisku „MASTER Przełącznik RESET" powoduje natychmiastowe rozłącza wszystkie testy przyrządy z każdego punktu testowego .

Circuit Operation

Działanie obwodu

The two MT8804A's are the heart of this analog switching circuit, coupling combinations of test instruments to the eight test points of the circuit under test. Using all CMOS components and asynchronous operation results in ultra-low operating power consumption.

Dwa MT8804A są sercem tego analogu obwód przełączający , łączący przyrządy z ośmioma punktami testowymi obwodu testowanego. Dzięki wykorzystaniu wszystkich komponentów CMOS asynchroniczna praca skutkuje bardzo niskimi kosztami zużycie energii elektrycznej podczas pracy.

The allowable voltage swing from the signal sources is from +5V to -5V as determined by the MT8804A power supplies. The control inputs swing from 0V to 10V. User control of the circuit is via a standard 16 switch keypad and four additional momentary pushbutton switches. The keypad consists of 16 SPST switches with one common terminal which is connected to V_{DD} = +5V. The eight switches, marked '1' through '8' are connected to an 8 line to 3 bit binary encoder (4532). The remaining keys are connected to NOR R-S latches (4043) directly. All sixteen switches are pulled to ground through resistors.

Pressing the 'TEST POINT' switch clears all the latches, setting up the circuit for new data. The address (A_0-A_2) of the MT8804A from the '4532' encoder is asynchronously latched. This address is decoded by the MT8804A to select the line (L_0 - L_7) and hence the test point corresponding to the numbered key pressed. The Group Select (GS) output of the '4532' goes high whenever one of its eight data inputs goes high. This signal is also latched and used to gate the AE pulse to the MT8804A. This ensures that test point number has been entered and hence prevents unwanted or accidental connections. A series of designated test equipment keys is pressed, setting corresponding latches which are connected to the data inputs (D_0 - D_3) of the MT8804A's.

These data inputs in turn correspond to the junctors (J0 - J3) to which the test equipment is connected. Pushing the 'CONNECT' button pulses the AE inputs of the two MT8804A's, completing the desired connection.

During a disconnect sequence, the latches are cleared by the 'TEST POINT' switch. The numbered key pressed sets up the address of the test point to be disconnected. Pressing the 'DISCONNECT' button next pulses the AE inputs. However, this time, all data inputs are at logical 0's so that all switches to the addressed test point are opened. The 'MASTER RESET' when activated opens all switches in the MT8804A disconnecting all test equipment from all test points. A power-up reset is provided by the resistor, capacitor and inverter in the master reset line. This prevents unwanted connections on power-up. Any convenient values of resistance and capacitance are appropriate provided that the power-up time is short in comparison to the time constraint. It is necessary, at

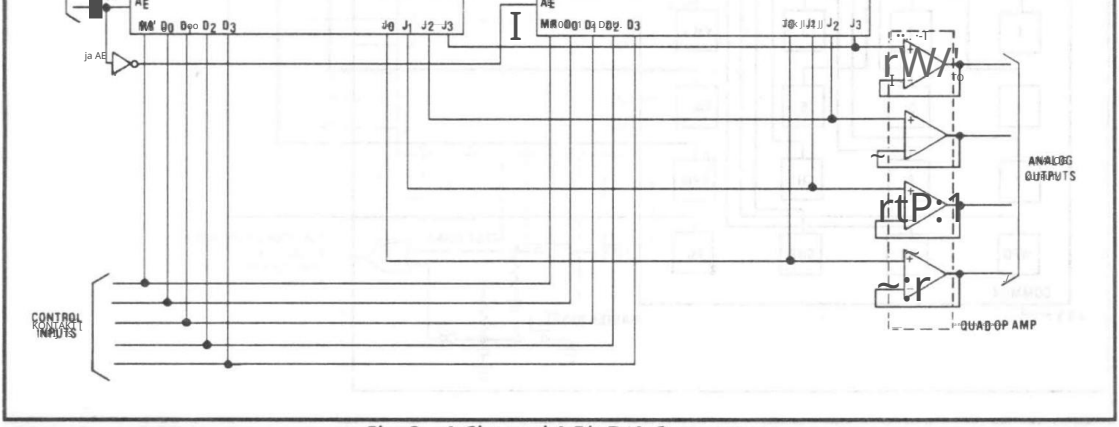

Fig. 9 - 4-Channel 4-Bit D/A Converter

Rysunek 9 - 4-kanałowy 4-bitowy przetwornik cyfrowo-analogowy

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all times to supply power to the switching circuit prior to energizing signal sources.

4-Channel 4-Bit D/A Converter

The circuit of Figure 9 can be used to implement a low resolution (4-Bit), multichannel D/A converter. The digital signals are input on the address lines (A_0 - A_1, A_E) and the analog signals are switched from the respective channel to the MT8804A (I_0 - I_3) and onto the junction as selected by the data inputs. Any voltage profile can be programmed be it linear, logarithmic etc., by selecting the appropriate resistors for the divider network. The linearity and monotonicity of the converter are determined by the matching of resistors used. The temperature stability of the converter is dependent upon the relative tracking of the resistors in the network with temperature. The resistor network is shown with one end connected to V_{DD} and the other to V_{SS}. By setting $V_{SS} = -V_{REF}$, the converter outputs will swing from $+V_{REF}$ to 0V in one mode and symmetrically about 0V from $\pm V_{REF}$ in the other. The op amp buffers are used to reduce the effects of the ON resistance of the MT8804A.

The four analog outputs can simultaneously provide four independent voltages or any combination of outputs may be set to the same voltage. The converter can be expanded to more digital inputs by extending the resistive ladder and adding MT8804's.

Programmable Attenuator

The programmable attenuator shown in Figure 10 is capable of providing up to 60dB of attenuation or 20dB of gain. Selecting the input attenuation is accomplished via the address inputs (A_0 - A_2) and can be chosen in 3dB steps. The range is selected in 20dB steps by gating an attenuated input signal onto the appropriate junction (J_0 - J_3) via the data inputs (D_0 - D_3). The attenuated input signal is buffered after passing through the MT8804A to provide a low impedance source to the attenuator circuit. The resistors are chosen to provide the logarithmic profile of attenuation, calibrated in dB. A linear profile for use in control system applications is accomplished easily by appropriate choice of resistors. The attenuation accuracy is purely a function of resistor tolerances.

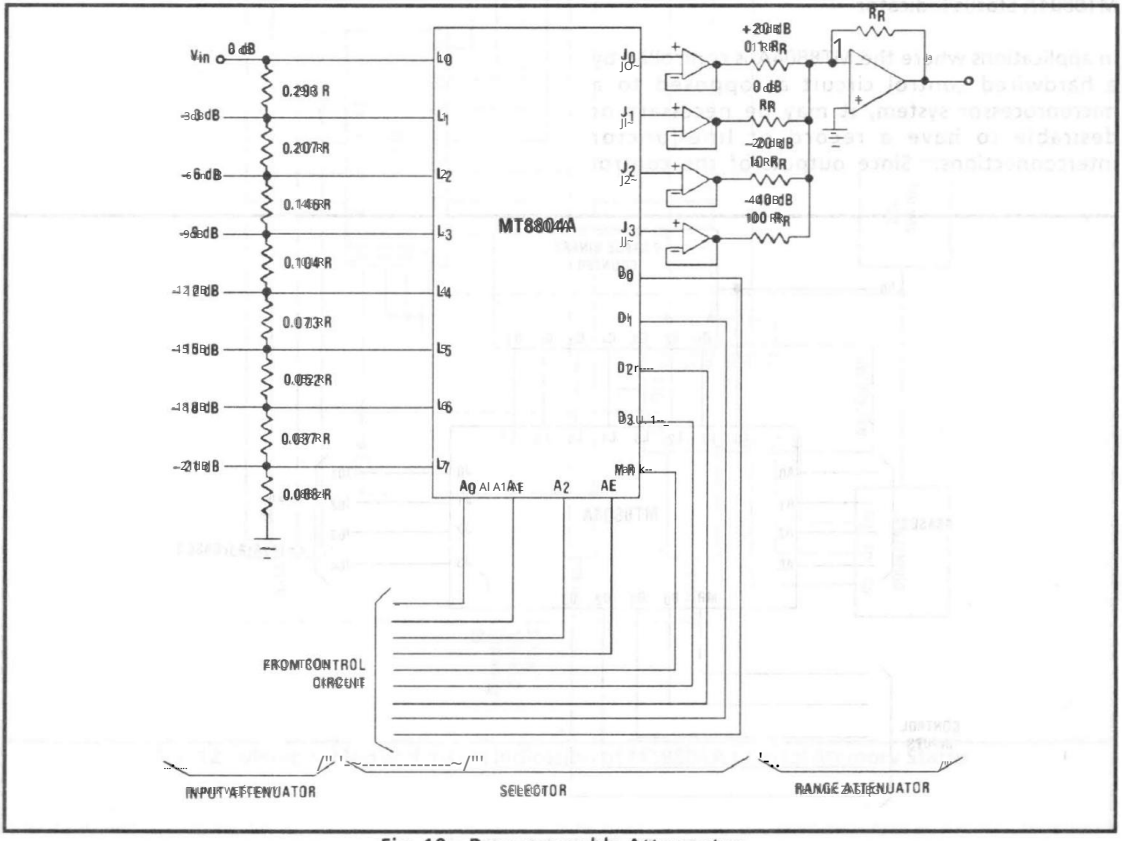

Fig. 10 Programmable Attenuator

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The circuit attenuation can be expressed as follows:

FOR ADDRESS (A$_0$ A$_1$ A$_2$)$_2$ = N$_{10}$

$A_{dB} = -(V_0/V_I)_{dB} = (3 \times N_{10} + A_R)$ dB

Where (A$_0$ A$_1$ A$_2$)$_2$ = Address expressed as binary number

A$_R$ = Attenuation in dB of range attenuator

Multi-Output 2n Programmable Frequency Divider

The circuit of Figure 11 provides up to 4 independent output frequencies each of which is a binary weighted multiple of a given input frequency. The frequency division factor is represented by the binary coded number of the address inputs of the MT8804A. The division range for the circuit shown is from 2^0 to 2^7. This range can be increased by adding counters for frequency division and MT8804A's to do the switching. The four data inputs (D$_0$ to D$_3$) control which output line or lines are switched to a particular frequency. The master reset (MR) when taken high turns all switches off.

MT8804A Status Indicator

In applications where the MT8804A is controlled by a hardwired control circuit as opposed to a microprocessor system, it may be necessary or desirable to have a record of the octal three state buffer, MT74SC241.

latches are not available, a duplicate memory map is required. A 8 x 4 array of light emitting diodes is used to provide visual output of the information (See Fig. 12). Control data written into the MT8804A is copied into a Random Access Memory. The RAM shown, the Fairchild 4710BX, is a CMOS device organized as 16 four bit words. As such, 2 MT8804A's could be mapped with one device. The RAM outputs can be used for control purposes as well as visual outputs as shown in the diagram.

A scanning oscillator and counter (negative edge triggered) are used to continuously read data out of the RAM and refresh the LED matrix. The address provided by this binary counter is decoded to a one of eight active low output format by the MD74SC138. Drive current is provided by two 74367 hex TTL buffers. A variable duty cycle waveform may be applied to the output enables to provide intensity modulation. When data is written into the MT8804A and RAM, the address is provided by the control circuit. This address is isolated from the scanning counter by the octal three state buffer, MD74SC241.

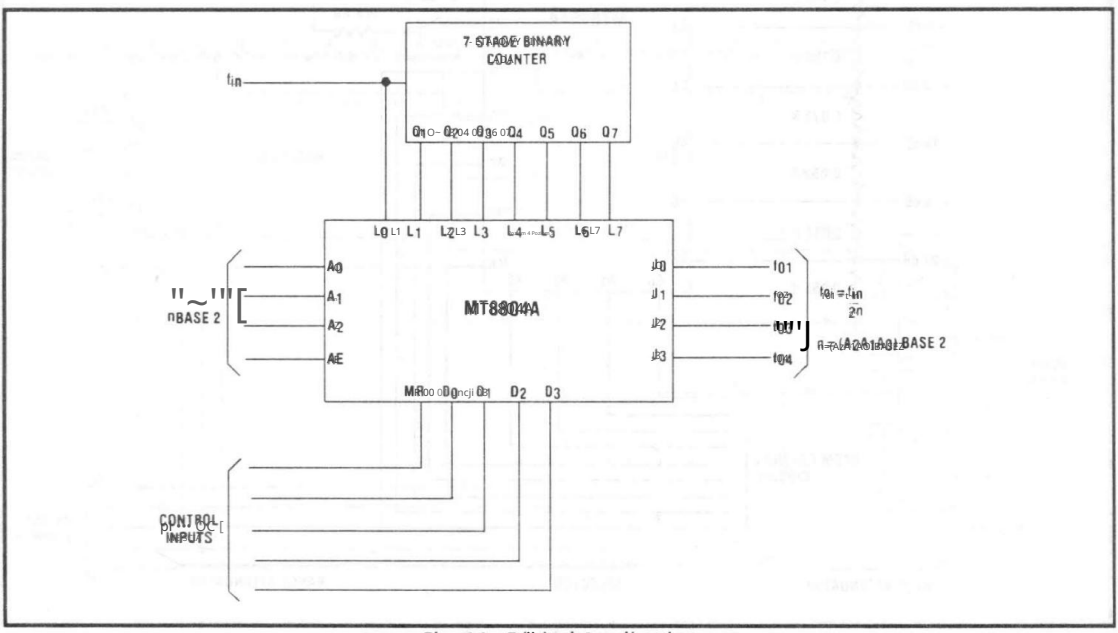

Fig. 11 - Application

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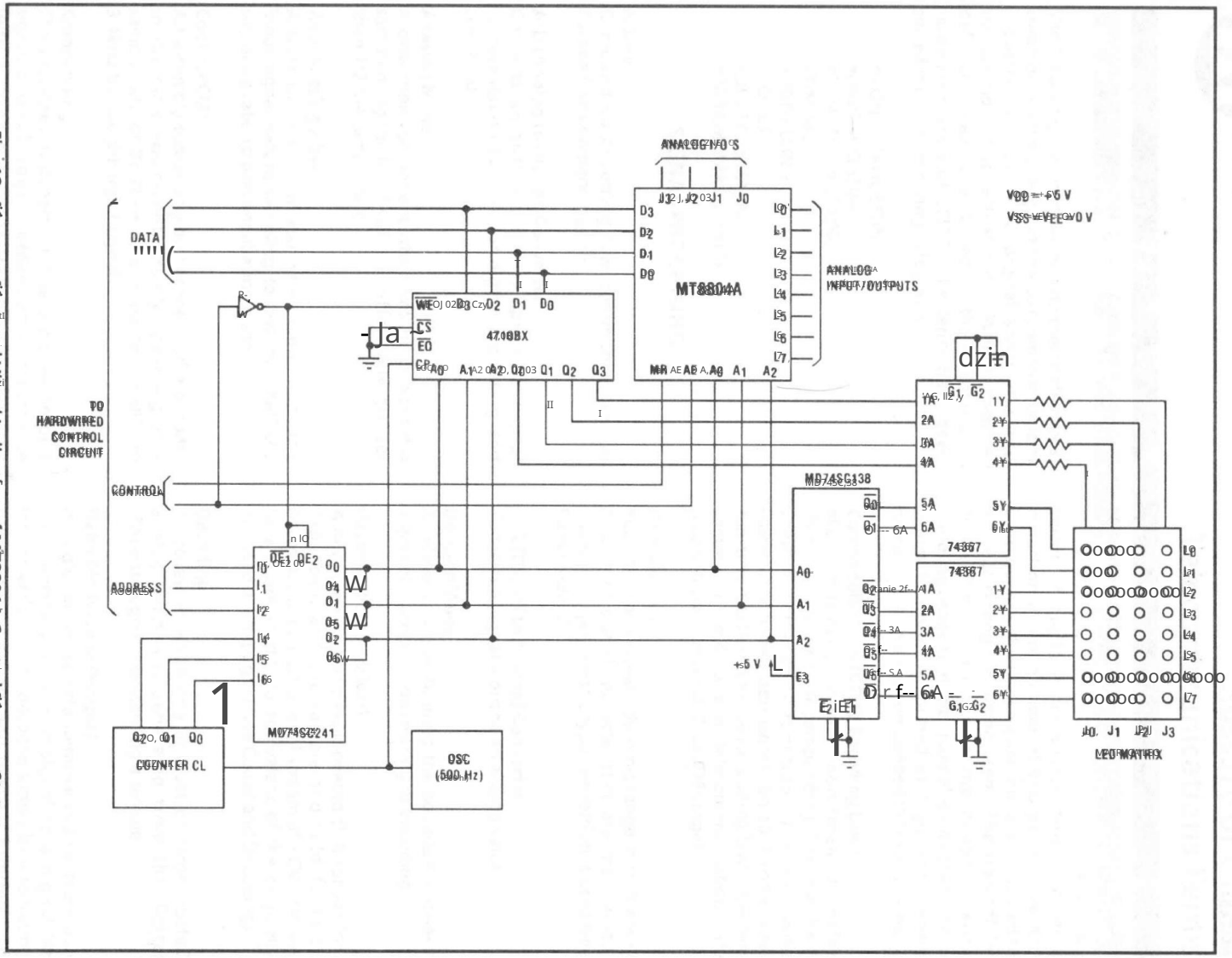

Fig. 12. Memory Map and Visual Indication of MT8804A Control Memory Status

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NOTES:

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sierpień 1986

The following is a list of terms and their definitions, commonly encountered in the telecommunications industry in relation to digital switching and transmission of speech signals. Where possible, definitions have been based on the international recommendation of CCITT. The terms have been sorted into the following categories:

Poniżej znajduje się lista terminów i ich definicji powszechnie spotykanych w branży telekomunikacyjnej w odniesieniu do przełączania cyfrowego i transmisji sygnałów mowy. Tam, gdzie było to możliwe, definicje zostały oparte na nimi dzynarodowych zaleceniach CCITT. Terminy zostały posortowane w następujące kategorie:

- SIGNAL PROCESSING
- DIGITAL SIGNALS
- PCM MULTIPLEXING
- TIMING
- SIGNALLING
- CODES
- DIGITAL SYSTEMS
- PARAMETERS & UNITS

- PRZETWARZANIE SYGNAŁU
- SYGNAŁY CYFROWE
- MULTIPLEKSOWANIE PCM
- TIMING
- SYGNALIZACJA
- KODY
- SYSTEMY CYFROWE
- PARAMETRY I JEDNOSTKI

SIGNAL PROCESSING

A-Law

Companding/encoding law, commonly used in Europe (see Companding Law).

Kompandowanie/kodowanie prawo powszechnie stosowane w Europy (patrz Kompandowanie prawa).

A/D (Analog to Digital) Converter

Converts an analog signal sample to a digital representation suitable for digital processing and switching.

Konwerter A/D (analogowy/cyfrowy) przetwarza próbkę sygnału analogowego na słowo cyfrowe nadające się do przetwarzania cyfrowego i przełączania.

Aliasing Noise

A distortion component which will be created if a sampled signal bandwidth is effectively greater than 1/2 the sample rate.

Szum aliasingu

Składnik zniekształcenia, który powstanie, jeśli szerokość pasma próbkowanego sygnału będzie efektywnie większa niż połowa częstotliwości próbkowania.

Anti-Aliasing Filter

A filter (normally, lowpass) which band limits the input signal before sampling to less than half the sampling rate, to prevent aliasing noise.

Filtr antyaliasingowy Filtr

(zwykle dolnoprzepustowy), który ogranicza pasmo sygnału wejściowego przed próbkowaniem do wartości mniejszej niż połowa częstotliwości próbkowania, aby zapobiec szumowi aliasingu.

Codec (PCM)

An assembly comprising an encoder and a decoder in the same equipment, usually operating at a sample rate of 8kHz, to accomodate a 300Hz to 3.4kHz bandwidth input signal.

Kodek (PCM)

Zespół składający się z enkodera i dekodera w tym samym urządzeniu, zwykle pracujący z częstotliwością próbkowania 8 kHz w celu dostosowania się do sygnału wejściowego o szerokości pasma od 300 Hz do 3,4 kHz.

Companding

The processes of dynamic range compression of a signal and subsequent expansion in accordance with a given non-linear transfer characteristic (companding law) which is usually logarithmic. The purpose of companding is to allow transmission of the signal via a channel incapable of carrying the uncompressed dynamic range of the signal. In terms of digital transmission, this involves a reduction in the number of bits per sample and consequently the transmission bit rate compared to a linear coding law being used. The tradeoff for this effective increase in the dynamic range handling capacity of the channel is a degradation in signal to noise performed at high signal levels compared with an uncompanded (linear) systems.

Kompandowanie

Procesy kompresji zakresu dynamiki sygnału, po którym następuje rozszerzanie zgodnie z daną nieliniową charakterystyką przenoszenia (prawo rozszerzania), która jest zwykle logarytmiczna. Celem kompandowania jest umożliwienie transmisji sygnału przez kanał niezdolny do przenoszenia nieskompresowanego zakresu dynamiki sygnału. W terminach transmisji cyfrowej oznacza to zmniejszenie liczby bitów na próbkę, a w konsekwencji szybkość transmisji w porównaniu z liniowym prawem kodowania. Kompromisem za ten efektywny wzrost zakresu dynamiki obsługi zdolności kanału elektronicznego jest degradacja sygnału do szumu przy wysokich poziomach sygnału w porównaniu z systemami nieskompresowanymi (liniowymi).

Companding Law (CCITT Encoding Law)

Mathematically defined non-linear transfer characteristic used for companding. This may be a smooth continuous function or a piecewise (commonly linear) approximation to a continuous function (CCITT segmented encoding law). The two commonly used laws in telecommunications are μ-Law (North America), A-Law (Europe).

Prawo kompandujące (Prawo kodowania CCITT)

Matematycznie zdefiniowana nieliniowa charakterystyka transferu używana do rozszerzania. Może to być gładka funkcja ciągła lub przybliżenie po kawałku (zwykle liniowe) do funkcji ciągłej (prawo CCITT segmented encoding). Dwa powszechnie stosowane prawa w telekomunikacji to prawo μ (Ameryka Północna), prawo A (Europa).

Compression

Reduction of a signal's dynamic range in such a way that small signal characteristics are maintained. Usually a logarithmatic type conversion is used (see Companding).

Kompresja

Zmniejszenie zakresu dynamiki sygnału w taki sposób, aby zachować niewielkie parametry charakterystyki sygnału. Zwykle stosuje się konwersję logarytmiczną (patrz Kompandowanie).

D/A (Digital to Analog) Converter

Converts a digital word to an analog value.

Konwerter D/A (cyfrowy na analogowy)

Zamienia słowo cyfrowe na wartość analogową.

Decision Value

A reference value defining the boundary between adjacent intervals in quantizing or encoding.

Wartość decyzyjna

Wartość odniesienia definiująca granicę pomiędzy sąsiednimi interwałami podczas kwantyzacji lub kodowania.

Decoder (PCM Receiver)

A device which performs repeated D/A conversion, expansion and the sample and hold function necessary to convert a serial stream of PCM samples to a sample and hold equivalent of the originally encoded analog signal (see Codec and Decoding).

Dekoder (odbiornik PCM)

Urządzenie, które wykonuje wielokrotną konwersję C/A, ekspansję i funkcję próbkowania i zapamiętania potrzebne do konwersji szeregowego strumienia sygnałów PCM na próbkowanie i zapamiętanie ekwiwalentu oryginalnie zakodowanego sygnału analogowego (patrz Kodowanie i zakodowanie).

Decoding

A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Dekodowanie

Proces, w którym jeden z zestawu zrekonstruowanych próbek analogowych jest generowany z cyfrowego sygnału znakowego reprezentującego próbkę.

Delta Modulation (Simple)

A single bit per sample iterative coding technique for converting an analog signal to a digital bit stream which can be decoded simply by integrating the digital bit stream and lowpass filtering. To obtain telephony quality transmission requires a sample rate of approximately 8kHz.

Modulacja Delta (Prosta)

Pojedyncza technika kodowania iteracyjnego bit na próbkę do konwersji sygnału analogowego na cyfrowy strumień bitów, który można zdekodować po prostu przez zintegrowanie cyfrowego strumienia bitów i filtrowania dolnoprzepustowego. Aby uzyskać transmisję o jakości telefonicznej, wymagana jest częstotliwość próbkowania około 8 kHz.

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Delta-Sigma Modulation (Simple)

Modulacja Delta-Sigma Kerady'ma (Prosty)
Technika kodowania pojedynczego bitu na próbkę
Kor konwertuje sygnał analogowy na bit cyfrowy
strumień. Powstały strumień przedstawia sobą ciąg impulsów
zmiana sygnału analogowego, który może być
Odzyskany po prostu przez zliczanie przechwytywania
dominującego. Aby uzyskać transmisję o jakości telefonicznej
wymaga czę stotliwości próbkowania około

A single bit per sample iterative coding technique for converting an analog signal to a digital bit stream. The resulting bit stream is a pulse density function of the original analog signal which can be recovered simply by low pass filtering the bit stream. To obtain telephony quality transmission requires a sample rate of approximately 8kHz.

Dynamic Range

Zakres Dynamiki
Zakres dynamiki przetwornika jest miarą jego
możliwość obsługi szerokiego zakresu amplitudy wejściowej
jednocześnie z najwyższej możliwej rozdzielczości liczby
sygnałów do najmniejszego sygnału, jaki można obsłużyć.

The dynamic range of a converter is a measure of its ability to handle a wide range of input amplitude and is defined as the ratio of the largest resolvable signal to the smallest signal that can be handled.

Encoder (PCM)

Enkoder (PCM)
Urządzenie, które wykonuje powtarzalną kompresję i próbowanie,
konwersję analogowo-cyfrową w celu konwersji
sygnał analogowy do strumienia szeregowego lub próbek PCM
reprezentujący sygnał analogowy (patrz także
kodowanie).

A device which performs repeated sampling, compression and A/D conversion to convert an analog signal to a serial stream of PCM samples representing the analog signal (see Codec and Encoding).

Encoding

Kodowanie

Coding

Generacja cyfrowa reprezentuje charakter sygnały do
skwantowane analogowe próbki.

The generation of digital character signals to represent quantized analog samples.

Encoding Law (see Companding Law)

Prawo rozszerzania (patrz prawo rozszerzania)
Prawo określające względne wartości kwantowe
kroki wykorzystywane w kwantyzacji i kodowaniu.

The law defining the relative values of the quantum steps used in quantizing and encoding.

Error Ratio

Stopa błędów
Miara zniekształcenia sygnału cyfrowego jest
współczynnik bię dów, który jest określany jako liczba bię dnie
odebranych bitów podzielona
przez całkowitą liczbę otrzymanych bitów.

A measure for the distortion of a digital signal is the error ratio which is defined as number of wrongly received bits divided by the total number of received bits.

Expansion

Rozszerzanie
Zakres odzyskiwania skompresowanego sygnału z powrotem do niego
oryginalnej dynamiki. Expansion (patrz Companding)

Expansion of a compressed signal back to its original dynamic range (see Companding).

HIDM (High Information Delta Modulation)

HIDM (High Information One) Modulacja delta
Jeden z wielu zintegrowanych systemów delta modulacji
modulacyjnych). Działa przy niższych czę stotliwościach próbkowania niż
prosta delta modulacja odpowiednik, to ru
wykonanie.

One of many companded delta modulation schemes. Operates at lower sample rates than simple delta modulation for equivalent performance.

Instantaneously Companded Delta-Sigma Modulation

Modulacja złożony Delta Sigma
Natychmiastowe
Jak sama nazwa wskazuje, jest to schemat modulacji delta-sigma łowiowany
schematów HIDM.

As its name implies, an equivalent scheme in delta-sigma modulation to the HIDM scheme.

Linear Quantizing

Kwantowanie liniowe
Kwantowanie, w którym wszystkie przedziały są równej
Linear A/D converter.

Quantizing in which all the intervals are equal, i.e., linear A/D converter.

Non-Linear Quantizing

Kwantowanie nieliniowe
kwantowanie, w którym interwały nie są jednakowe.
Dzię ki temu kwantyzacja jest możliwa.

Quantizing in which the intervals are not all equal. This keeps the quantizing distortion as low as possible.

Pulse Code Modulation (PCM)

Modulacja kodowo-impulsowa (PCM)
Proces, w którym próbkowany jest sygnał analogowy,
wielkość każdej próbki w odniesieniu do
Spię trzona referencji jest kwantowana i konwertowana przez
kodowanie do sygnału cyfrowego. To jest powszechne
systemów cyfrowych przesyłanie
komunikacyjnych.

A process in which an analog signal is sampled, and the magnitude of each sample with respect to a fixed reference is quantized and converted by coding to a digital signal. This is the prevalent technique for digital transmission in communications systems.

Quantizing

Kwantowanie
Proces, w którym próbki są zaokrąglane do
liczba sześciu przedziałów (kroków amplitudy) każdy
krok interwału reprezentowany przez pojedynczą wartość
call wskazał wartość skwantowaną.

A process in which samples are classified into a number of adjacent intervals (amplitude steps) each interval step being represented by a single value called the quantized value.

Quantizing Distortion

Kwantowanie dystorcji
Due to the restriction of a finite number of
wynikające z ograniczenia
przekazywanych informacji a pierwotna różnica
nazywana jest zniekształceniem kwantyzacyjnym.

Due to the restriction of a finite number of produced amplitude steps, a difference inevitably occurs between the information which can be transmitted and the original information. This difference is called quantizing distortion.

S&H (Sample and Hold)

S&H (próbkowanie i przechowywanie)
Układ, który pobiera próbkę sygnału przechowuje ją
wartość próbki do momentu pobrania następnej próbki. W
konwersji jest zwykle sprzę żone z analogowym
konwersja cyfrowo-analogowa może być wykonana
cyfrowo, korzystając w sposób ciągły z D/A
przetwornik lub przetwornik cyfrowo-analogowy może być współdzielony przez
inne funkcje i jego sygnał wyjściowy utrzymywany przez
analogowy dowód próbkowania i podtrzymywania.

A circuit which samples a signal and holds the sample value until the next sample is taken. In A/D conversion S/H is usually an analog function. In D/A conversion the S/H may be performed digitally, making continuous use of the D/A convertor or the D/A convertor may be shared by other functions and its output signal held by an analog sample and hold circuit.

Sample

Próbka
Wartość określonej charakterystyki sygnału przy
wybranym czasie.

The value of a particular characteristic of a signal at a chosen instant.

Sampled Data System

System danych próbkowanych
System działający na próbkach analogowych
sygnały wejściowe. Mogą być analogowe (np. przełączane
kondensatorowy) lub cyfrowy (kodowanie mowy, cyfrowy
przetwarzania (filter) lub sobu.

A system that operates on samples of the analog input signals. Can be either analog (e.g., switched capacitor filter) or digital (speech coding/digital filter) processing or both.

Sampling

Próbkowanie
Proces pobierania próbek, zazwyczaj w tym samym czasie
odstępy czasu.

The process of taking samples, usually at equal time intervals.

Sampling Rate

Czę stotliwość próbkowania
Liczba pobranych próbek w jednostce czasu.

The number of samples per unit time.

Segmented Encoding Law

Prawo Segmentacji
Gładkie prawo kodowania uzyskuje się prawo, które jest przybliżeniem
za pomocą liczby liniowej
segmenty.

An encoding law which an approximation to a smooth law is obtained by a number of linear segments.

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Single Channel Codec

Codec which is designated to operate on a single signal source and not a multiplexed mode performing the codec functions for more than one signal source.

Single Chip Codec

A single integrated circuit capable of performing all codec functions and in some cases providing an auxiliary signalling interface. It may be either single channel or multiplexable.

Smoothing (Decode or Reconstruction) Filter

Usually low-pass. Restores the desired analog signal at the S&H D/A or decoder output by blocking high frequency components produced by sampling.

Working Range

The permitted range of values of an analogue signal over which a transmission or other processing equipment can operate.

Virtual Decision Value

Two hypothetical decision values, used in quantizing or encoding. Located at the ends of the working range used and obtained by extrapolation from the real decision values. Effectively specify the maximum input signal amplitude.

μ-Law

Companding encoding law commonly used in North America (see Companding Law).

DIGITAL SIGNALS

ADI

Alternate digit inversion. Used with A-Law to ensure sufficient 1-0/0-1 transitions for clock extraction (timing recovery) in PCM multiplex transmission equipment.

Asynchronous Transmission

A mode of communication characterized by start/stop transmissions with undefined time intervals between transmissions.

Binary Digit

A member selected from a binary set, e.g., 1,0; V+, V−; H,L.

Note: Bit is an abbreviation for binary digit.

Character Signal

A set of signal elements representing a character, or in PCM representing the quantizing value of a sample.

Note: In PCM terminology, the term "PCM word" may be used in this sense.

Digit

A member selected from a finite set.

Note 1: In digital transmission, a digit may be represented by a signal element, being characterized by the dynamic nature, discrete condition and discrete timing of the element, e.g., it may be represented as pulse of specified amplitude and duration.

Note 2: In equipment used in digital transmission, a digit may be represented by a stored condition being characterized by special physical condition, e.g., it may be represented as a binary magnetic condition of a ferrite core or voltage condition in a semiconductor memory cell.

Note 3: The context of the use of the term should be as such as to indicate the radix of notation. (The meaning of "digit" in Notes 1, 2, and 3 translates into French as "élément numérique".)

Note 4: In telephone subscriber numbering, a digit is any of the numbers 1, 2, 3...9 or 0 forming the elements of a telephone number (Recommendation Q.10). (This meaning of "digit" translates into French as "chiffre".)

Digital Signal

A signal constrained to have a discontinuous characteristic in the form of permitted discrete values.

Equivalent Bit Rate

In a line coded signal, the number of binary digits that can be transmitted in a unit of time.

Note: The point which the equivalent bit rate is referred may be either real or hypothetical.

Intersymbol Interference

Interference in digital (or any Time Division) transmission system caused by a symbol in one signalling interval being spread out and overlapping the sample time of a symbol in another signalling interval.

Jitter

Short-term variations of the significant instants of a digital signal from their ideal positions in time.

Regardless of the stability of clocks at both ends of a digital transmission system, certain amounts of instability occur due to changing signal because of external electrical disturbances and changing physical parameters of the transmission link. The resulting instability in the line clock is referred as "jitter".

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Regeneration
The process of recognizing and reconstructing a digital signal so that the amplitude, waveform and timing are constrained within stated limits.

Synchronous Transmission
A mode of digital transmission in which discrete signal elements (symbols) are transmitted at a fixed and continuous rate.

PCM MULTIPLEXING

Channel Bank
Terminal equipment for a transmission system used to derive individual channels using FDM or TDM techniques.

Digital Multiplex Equipment
Equipment for combining, by time division multiplexing (multiplexer), a defined integral number of digital input signals into a single digital signal at a defined digit rate, and also for carrying out the inverse function (demultiplexer).

Frame
A set of consecutive digit timeslots in which the position of each digit slot can be identified by reference to a framing signal. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Highway
A common path or a set of parallel paths over which signals from many sources pass with separation achieved by time division.

Justification (Pulse Stuffing)
A process of changing the rate of a digital signal in a controlled manner so that it can accord with a rate different from its own inherent rate, usually without loss of information.

Multiframe
A set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal. The multiframe signal does not necessarily occur, in whole or in part, in each multiframe.

Multiplexing
The process of combining the multiple signals into a single channel for transmission over common facilities.

PCM Multiplex Equipment
Equipment for deriving a single digital signal at a defined digit rate from two or more analogue channels, employing pulse code modulation and time division multiplexing (multiplexer) and also for carrying out the inverse function (demultiplexer). The description should be preceded by the relevant equivalent binary digit rate, e.g. 2048 kbit/s PCM multiplex equipment.

Primary Block (American Digroup)
A basic group of PCM channels assembled by time division multiplexing.

Note: The following conventions could be useful:

Primary block - a basic group of channels derived from 1544 kbit/s PCM multiplex equipment.

Primary block - a basic group of PCM channels derived from 2048 kbit/s PCM multiplex equipment.

Time Division Multiplexing
Several information channels are multiplexed (time shared) over a single communication circuit by sampling each channel periodically and allocating each sample an assigned timeslot in the circuit.

T1 Carrier System (North America)
PCM multiplex equipment using 8 digit A-Law encoding to provide 24 channels (timeslots).

30 Channel Mux (U.K. & Europe)
PCM multiplex equipment conforming to CCITT recommendations for PCM, digital multiplex equipment, digital line systems. Using 8 digit A-Law encoding, 30 speech channels + 2 utility channels (32 timeslots in all) transmission rate 2,048 kbit/s.

Transmultiplexer
An equipment which transforms signals derived from frequency division multiplex equipment to time division multiplexed signals having the same characteristics as those derived from PCM multiplex equipment and vice versa.

24 Channel Mux (U.K.)
Early PCM multiplex equipment using 7 digit A-Law, 1 signalling bit associated with each sample, 24 channels (timeslots) transmission rate 1536 kbit/s.

TIMING

Channel Timeslot
An interval of time occurring at a particular phase in a frame and allocated to a channel for transmitting a character, signal combination or possibly information signalling or other information.

Digit Timeslot
A timeslot allocated to a single digit.

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Frame Alignment
Wyrównanie ramki
The state in which the frame of the receiving equipment is correctly phased with respect to that of the received signal.
Stan, w którym ramka urządzenia odbiorczego jest poprawnie sfazowana względem ramki odebranego sygnału.

Frame Alignment Signal
Sygnał wyrównania ramki
The distinctive signal used to enable frame alignment to be secured.
Charakterystyczny sygnał umożliwiający zabezpieczenie wyrównania ramki.

Frame Alignment Timeslot
Przedział czasowy wyrównania ramki
A timeslot starting at particular phase in each frame and allocated to the transmission of a frame alignment signal.
Szczelina czasowa rozpoczynająca się w określonej fazie każdej ramki i przydzielona do transmisji sygnału wyrównania ramki.

Master Clock
Zegar główny
A clock which generates accurate timing signals for the control of other clocks and possibly other equipments.
Zegar, który generuje dokładne sygnały czasowe do sterowania innymi zegarami, a także innym sprzętem.

Mesochronous
Mezochroniczne
Two signals are mesochronous if their corresponding significant instants occur at the same average rate.
Dwa sygnały są mezochroniczne, jeśli ich odpowiednie istotne momenty występują z taką samą średnią częstotliwością.

Non-Synchronous Network (Asynchronous Network)
Sieć asynchroniczna
A network in which the clocks need not be synchronous or mesochronous.
Sieć, w której zegary nie muszą być synchroniczne ani mezochroniczne.

Signalling Timeslot
Przedział czasowy sygnalizacji
A timeslot starting at particular phase in each frame and allocated to the transmission of signalling.
Szczelina czasowa rozpoczynająca się w określonej fazie każdej ramki i przydzielona do transmisji sygnalizacji.

Synchronous
Synchroniczne
Two signals are synchronous if their corresponding significant instants have a desired phase relationship.
Dwa sygnały są synchroniczne, jeśli ich odpowiednie istotne momenty mają pożądaną zależność fazową.

Synchronous Network
Sieć synchroniczna
A network in which the clocks are controlled so as to run ideally at identical rates, or at the same mean rate with limited relative phase displacement.
Sieć, w której zegary są kontrolowane tak, aby działały idealnie z identyczną częstotliwością lub z taką samą średnią częstotliwością przy ograniczonym względnym przesunięciu fazy.

Timeslot
Przedział czasowy
A specific time interval which can be recognized and characterized uniquely.
Określony przedział czasowy, który można jednoznacznie rozpoznać i scharakteryzować.

Timing Recovery (Timing Extraction)
Odzyskiwanie czasu (Ekstrakcja czasu)
The derivation of a timing signal from a received signal.
Wyprowadzenie sygnału czasowego z odebranego sygnału.

Timing Signal
Sygnał czasu
A cyclic signal used to control the timing of operations.
Sygnał cykliczny służący do sterowania czasem operacji.

SIGNALLING
SYGNALIZACJA

CCIS
Sygnalizacja za pomocą wspólnego kanału
Common channel interoffice signalling.
Wspólna międzycentralowa sygnalizacja kanałowa.

Common Channel Signalling
Sygnalizacja za pomocą wspólnego kanału
A signalling method using a link common to a number of channels for the transmission of signals necessary for the traffic via these channels.
Metoda sygnalizacji wykorzystująca łącze wspólne dla wielu kanałów w celu transmisji sygnałów niezbędnych dla ruchu przez te kanały.

Signalling
Sygnalizacja
The exchange of electrical information (other than by speech) associated with the establishment, control and management of communication over and between telecommunication networks and computer systems and data networks.
Wymiana informacji elektrycznych (innych niż za pomocą mowy) związanych z ustanawianiem i kontrolowaniem połączeń w sieci telekomunikacyjnej oraz zarządzaniem nimi, a także między systemami komputerowymi i sieciami danych.

Signalling (sometimes called Bit Stealing)
Sygnalizacja (czasami nazywana kradzieżą bitów)
Signalling in which digit timeslots primarily used for the transmission of encoded speech are periodically used for signalling.
Sygnalizacja, w której przedziały czasowe cyfr, przeznaczone głównie do transmisji zakodowanej mowy, są okresowo wykorzystywane do sygnalizacji.

CODES
KODY

A-law or μ-law Companded 8-bit PCM Binary Code
Kod binarny PCM 8-bit z kompresją A lub μ
The codes almost universally used for PCM digital switching and transmission. When reference is made to PCM it is almost invariably these codes which are being referred to (A-law version in Europe and μ-Law version in North America).
Kody powszechnie używane do cyfrowej komutacji i transmisji PCM. Mówiąc o PCM, prawie zawsze mamy na myśli te kody (wersja A-law w Europie i wersja μ-Law w Ameryce Północnej).

Alternate Mark Inversion Signal (AMI) (Bipolar Signal)
Sygnał z naprzemiennym znakiem (AMI) (sygnał dwubiegunowy)
A pseudo-ternary signal conveying binary digits in which successive "marks" are normally of alternate polarity and equal in amplitude and in which "space" is of zero amplitude.
Sygnał pseudotrójkowy przenoszący cyfry binarne, w którym kolejne "znaki" są normalnie naprzemiennie przeciwne w polaryzacji i równe w amplitudzie, przy czym "spacja" ma zerową amplitudę.

HDB-3 Code High Density Bipolar 3 Code
Kod HDB-3 Kod bipolarny o wysokiej gęstości 3
Here two consecutive violations (bits) of the same polarity are permitted (interrupting a zero sequence which is too long). These violation bits, however, are arranged to form an AMI sequence in itself. (See modified AMI).
Kod bipolarny o wysokiej gęstości, w którym dopuszcza się dwa kolejne bity o tej samej polarności (przerywając zbyt długą sekwencję zer). Te bity naruszenia są jednak ułożone tak, aby same w sobie tworzyły sekwencję AMI. (Patrz zmodyfikowany AMI).

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Line Code

A code chosen to suit the transmission medium and giving the equivalence between a set of digits generated in a terminal or other processing equipment and the pulses chosen to represent that set of digits for the line transmission.

Modified Alternate Mark Inversion

An AMI signal which does not strictly conform with alternate mark inversion but includes violations in accordance with a defined set of rules.

PCM Binary Code

A pulse code in which the quantized values are identified by binary numbers taken in order.

Note: This term should not be used for line transmission.

Pulse Code

A code giving the equivalence between the quantized value of a sample and the corresponding character signal.

DIGITAL SYSTEMS

'Blocking' System

Telephones is one in which more telephones than through connection paths so dynamic channel allocation is needed on a demand basis. If all channels are busy, new calls are are blocked from completion or are delayed until a channel becomes available.

Connection

The circuits and equipment which together provide a communication path between two subscriber stations.

Digital Switching

A process in which analog signals are converted to digital signals and connections are established by operations on the digital signals. Alternatively, digitally encoded signals are transmitted by operating on the digital signals directly without converting to analog.

'Non-Blocking' System

Each telephone has a guaranteed through connection when needed. This may be in the form of dedicated channels (fixed channel asignment) which guarantees a phone ten same communication channel at any time.

STS Switch

Space Time Space Switch, large switch consisting of a time switch block between two space switch blocks.

Space Division

Use of different physical paths to transmit two or more channels (N.B. 'space division multiplex' is a contradiction in terms).

Space Switch (Abbrev.) Space Division Switch

Multiport switch in which ports are interconnected by use of different physical paths.

TST Switch

Time Space Time Switch, large switch consisting of a space block between two time switch blocks.

Time Switch (Abbrev.) Time Division Multiplex Switch

Multiport switch in which all ports have access to the same physical path on which transmitted data from individual ports are allocated unique timeslots. Send and receive paths are connected by both accessing the same timeslot. The path may be a serial data or parallel data highway.

PARAMETERS & UNITS

dB

Decibel, unit of measure of relative power level defined as $10 \log_{10}(P_1/P_2)$ assuming R1 = R2 where P_1 and P_2 are the power levels.

dBm

Power in decibels relative to 1 mW.

dBm0

dBm referred to or measured at a point of zero transmission level.

dBmp

dBm psophometrically weighted. Unit of power in dBm measured with psophometric weighting. Conversion is as follows:

$$dBmp = 10 \log_{10} pWp - 90$$
$$= dBa - 84$$
$$= dBm - 2.5 \text{ (for flat noise 300-3400 Hz)}$$

dBm0p

Circuit noise in dBm0 measured on a line with a noise measuring set having psophometric weighting.

dBr

dB relative to point of zero transmission level.

dBrn

(decibels above reference noise). Weighted circuit noise power in dB relative to 1 picowatt (−90 dBm) which is defined as 0dBrn. Type of weighting is indicated by next letter (see dBrnc).

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Note: With 'C' message weighting, a 1mW 1 kHz tone will read +90 dBrn, but the same power with the noise randomly distributed over 3 kHz band (300-3400 cps) will read +88dBrn.

dBrnc

Weighted circuit noise power in dBrn, measured on a line by noise measuring set with 'C' message weighting.

dBrnc0

Noise power in dBrnc referred to zero transmission level point (0TLP).

$$dBrnC0 = dBrnc - 20 \log_{10} R_{LOAD}/600$$

Gain Level Linearity (U.K.)

See Gain Tracking Error.

Gain Tracking Error (N.A)

Gain Level Linearity

A measurement of the dependence of a device gain on signal level. The output signal is compared to the input signal (assuming unity gain) over a range of input signals. The variation of gain from a reference gain (determined at 0dBm input level) is the gain tracking error.

Idle Channel Noise

The total signal energy measured at the output of the device under the condition of no input signal. Unless otherwise specified, this is a wideband noise measurement.

Load Capacity (Overload Point)

In PCM, the level expressed in dBm0 of a sinusoidal signal, the positive and negative peaks of which coincide with the positive and negative virtual decision values of the encoder.

Peak Limiting

In PCM, the effect caused by the application to an encoder of an input signal whose value exceeds the virtual decision values of the encoder.

Quantizing Distortion

The distortion resulting from the process of quantizing.

Quantizing Distortion Power

The power of the distortion component of the output signal resulting from the process of quantizing.

Signal to Distortion Ratio (S/D)

The ratio between a reference signal level and the level of all components that are present when the input signal (1.020 kHz sinusoid) is eliminated from the output signal (by filtering for example).

Weighting Filters

Several different filters have been used to represent the transmission characteristics of different terminations. The two most frequently used are C-message (N.A) and Psophometric (Europe) weighting filters.

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MITEL®

Application Note MSAN-106

An Introduction to Mitel DTMF Receivers

November 1981

Dual tone multi-frequency (DTMF) receivers have been built using various filtering techniques. The most recent relies on MOS/LSI for higher quality and reduced cost. LSI DTMF detection relies on algorithms developed both empirically and analytically. New generations of receivers are just emerging: miniature hybrid receivers are already available in volume production. General acceptance in the marketplace has resulted in an accelerated rate of the innovation and the pricing trends made possible by the latest advances in LSI technology.

DTMF Signalling

Introduced over 25 years ago, DTMF signalling (also known as Touch-Tone*, Tel-Touch, etc.) has been steadily gaining ground at the expense of dial-pulse signalling. Not only is Touch-Tone telephone more convenient and more efficient to use, but it offers a higher reliability in transmission of signals. As a result signalling is no longer confined to telephony but has seen its domain expanded to various fields such as answering machines, radio communications, data transmissions and remote control.

The telephone handset generates a composite audio signal made of the superposition of two tones selected by line-and-column addressing of a keyboard. This scheme is shown in Figure 1.

These frequencies were chosen in such a way that neither their harmonics nor their intermodulation products fall in one of the tone bands. Separation between tones is typically 10%.

The fourth column of buttons (1633 Hz tone) is not usually present in today's telephone sets. However, it is available for future use. A 4 x 4 matrix of buttons is presently used in some military phones and is suitable for implementation in telephone sets intended for multiple functions such as financial transaction terminals, credit checking machines and some PBX or CBX systems.

The dual tone signal is heard in the ear-piece and is sent over the telephone lines to the private branch exchange (PBX) or directly to the central office, where it must be decoded into the digit that it represents. The decoder or receiver - will convert the DTMF signal to a binary format or to a 2-of-8 format. For traditional dial-pulse equipment, a further conversion is needed to achieve a complete Touch-Tone to dial-pulse interface, allowing telephone companies to offer subscribers Touch-Tone in areas where the equipment is not compatible. Such an application is termed a tone-to-pulse converter.

Before 1974 a number of techniques were used to achieve DTMF detection. Passive filters using LC networks for each frequency can still be found in some installations. When integrated operational amplifiers became more readily available, the designers switched to active filters using IC's and RC networks. With the advent of the phase-lock-loop in IC form, new designs were introduced embodying this approach.

Every solution outlined so far had technical or cost-related disadvantages. Advances in MOS/LSI technology have made it possible to solve the problem of DTMF decoding at considerable cost savings.

Digital DTMF Detection

The basic method of discriminating various frequencies from each other using digital logic is to relate the number of cycles of some reference clock signal to each period of the unknown frequency. Typically the DTMF signal is sent first through a band-splitting filter which separates the high and

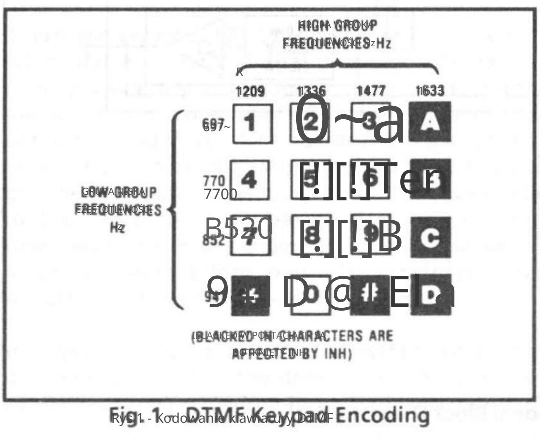

Fig. 1 - DTMF Keypad Encoding

* Touch-Tone is a registered service mark of AT&T

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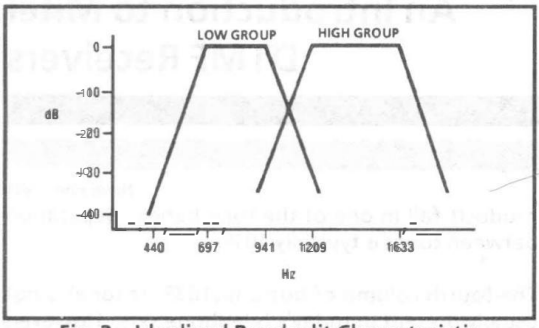

Fig. 2 - Idealized Bandsplit Characteristic

Rys. 2 - Charakterystyka idealnego podziału pasma

Fig. 4 - MH88305 Input Signal Characteristics

Rys. 4 - Charakterystyka wejściowa układu MH88305

low-band frequencies (Figure 2). Each frequency is then square-shaped and processed separately. The problem consists of establishing whether a frequency is recognizable as a DTMF tone, considering that this is within a certain frequency tolerance, or that it is simulation of a true DTMF tone such as produced by speech. As a result, the designer is faced by a dilemma: if the "accept" criteria are too relaxed, DTMF tone pairs are quickly recognized, as valid and so are speech segments which simulate real DTMF signal. This is referred to as "talk off". Now, if the "accept" criteria are too strict, detection time is inordinately stretched and the receiver is no longer in compliance with timing requirements. In other words, if detection time is fixed, this becomes a compromise between:

A. Tolerance to received tone imperfections and noise.

B. Immunity to tones simulated by speech (talk-off).

Modern receiver design can successfully deal with this problem by optimizing both the front-end filtering and the digital detection algorithm. Such a product, the MH88305, has been developed by Mitel to serve the most exacting requirements of DTMF receiver as found in central office applications. The MH88305 is a self-contained hybrid DTMF receiver measuring 1.5x2.5x0.25 inch (3.8x6.3x0.63cm).

No external components are needed to operate this receiver (even the time base crystal is enclosed), although the addition of a single resistor or capacitor allows the designer to modify three of the device parameters: detect time (time to detect the presence of a valid tone-pair); sensitivity (minimum acceptable signal level); and twist acceptance (degree of mismatch between the

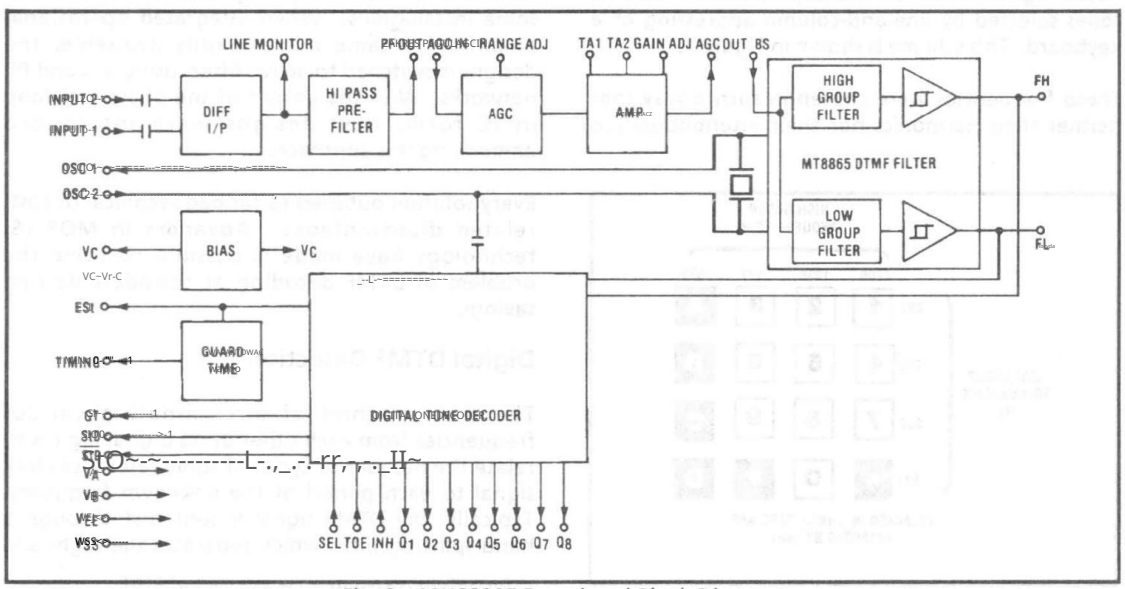

Fig. 3 - MH88305 Functional Block Diagram

Rys. 3 - Schemat blokowy funkcjonalny MH88305

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amplitudes of the two tones of a pair). The unit connects directly to the telephone line. Talk-off immunity is excellent; less than five "hits" on the Mitel test tape CM7291. Error rate is typically better than 1 error in 100,000 applied tones and third-tone tolerance meets the CEPT (A-16) recommendation of (A-16) dBm for a swept in-band tone applied simultaneously with undesired signal frequencies. Power consumption at 5V is a mere 50 mW and input sensitivity can be adjusted down to -42 dBm giving a maximum dynamic range of 55 dB as illustrated in Figure 4.

DTMF Receiver Specification

The worst case specifications of a DTMF receiver are typical of Central Office requirements:

Input Dynamic range	: -26 dBm to + 6 dBm
Twist (V_{FH}/V_{FL})	: 8 dB to + 4 dB
Dial Tone	: 350 Hz mixed with 440 Hz
Tone Burst (min.)	: 40 ms ON, 40 ms OFF
Repetition rate (max.)	: 12 pps
Valid tone accept	: ±1.5%
Invalid tone reject	: ±3.5%
Signal to noise ratio	: 16 dB
Silence gap bridging	: 15 ms

For other applications such as keyphone systems, the specifications are less stringent. No dial tone is used. No little twist exists on the line. In this case, some circuitry such as the dial tone rejection filter can be omitted.

Digital Detection Algorithm

There are several MOS/LSI devices on the market which perform DTMF digital detection. Some are even proprietary to companies involved in the manufacture of complete DTMF receivers, and thus are not sold as chips. All these devices have a basic tenet in common: digital period counting relying on a zero crossing detector. Little difference exists in the choice of pass bandwidths. The two main divergences lie in the choice of criteria leading to accept or reject a tone-pair. It is instructive to discuss one of the more general techniques.

In order to reduce the overall system cost, the designer tries to shift the design complexity to the converters i.e. the LSI/MOS devices, rather than the front-end filtering which is typically costlier. Thus, when the band-splitting filters have less-than-ideal attenuation the separated tones will carry a residue from the other band. This, in addition to random noise, results in jitter of the zero crossings (Figure 5).

Averaging several pulses eliminates most of the jitter effects. However it also allows easier speech simulation of tone-pairs. In order to improve speech rejection single period counting is made to concur with the counting of several periods. Such a technique is used in the Mitel MT8860 decoder and its variants the MT8862 and MT8863. The Mitel MH88305, which uses the MT8863 digital decoder, also uses the LSI bandsplit filter the MT8865. This device uses switched capacitor filters implemented in Mitel's double poly ISO2-CMOS™ technology.

The MT8860/8865 chip pair integrates an entire functional receiver, the external circuitry required being independent of the user's system environment and specification. Typical enhancements might be a differential input amplifier for line interfacing; profiltering for extra dial-tone rejection; agc circuitry for extended dynamic range. All of these enhancements are incorporated into the MH88305 hybrid.

In addition to the digital detection algorithm, Mitel tone receivers incorporate a further validation check during a period termed the guard-time. This time is user accessible since it is set by an external RC time constant and it offers the designer further flexibility in optimizing receiver performance while complying with his particular system timing requirements. Use of the guard-time feature is fully described in the data sheets of the devices referenced here. Figure 6 tabulates the four main system timing parameters which may be adjusted.

Future LSI Receivers

Work is being conducted at Mitel to develop still smaller and more cost effective receivers. The first of the new generation monolithic receivers now under development is the MT8870, which combines the filter and decoder functions in one chip contained in a compact 18-pin package. Gains in performance as well as reductions in cost and size are expected from this ISO2-CMOS device, making

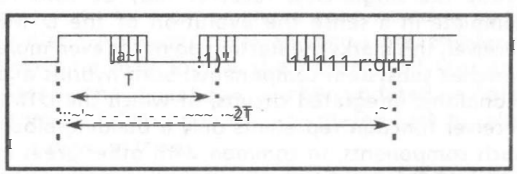

Fig. 5 - Zero Crossing Jitter

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Tone Pair Uznanie	Timing Chronometraż Stan rozrządu*	Typowe wartości parametrów systemu
SHALL EXIST / Istnieje	Tp > tREC	tREC < 38ms
MAY EXIST / MOŻE ISTNIEĆ	tREC ≤ Tp ≤ tREC	tREC > 30ms
SHALL NOT EXIST / NIE POWINNO ISTNIEĆ	Tp < tREC	tID < 38ms
Ustanie / SHALL CEASE	TA > tID	tDO > 20ms
MAY CEASE / MOŻE ZAPRZESTAĆ	tDO ≤ TA ≤ tID	
SHALL NOT CEASE / NIE PRZESTANIE	TA < tDO	

*Tp = Ciągła obecność prawidłowej pary tonów.
TA = Ciągła nieobecność ważnego tonu pary.

Fig. 6 - Typowe ograniczenia synchronizacji systemu

możliwe wykorzystanie technologii odbiorników DTMF w wielu nowych aplikacjach i obszarach.

Funkcje analogowe zaimplementowane w dzisiejszych czasach hybrydy (np. różnicowy przedni koniec, czułość sterowanie, agc dla szerokiego zakresu dynamiki) również podatne na możliwości integracji przy użyciu analogowej technologii ISO²-CMOS. Przyszłe zmiany mogą zatem pozwolić na umieszczenie większej części obwodu analogowego w chipie, w celu uzyskania jeszcze bardziej kompaktowego rozwiązania.

Rozwój ten stanowi zwieńczenie ostatnich pięciu generacji DTMF:

I. Odbiorniki LC i aktywnych filtrów.

II. Odbiorniki chipów detektora MOS/LSI.

III. Hybrydowe odbiorniki.

IV. Dwu-chipowe odbiorniki CMOS.

V. Jednoukładowe odbiorniki CMOS.

Dywidendy tej progresji są dobrze znane dzisiaj:

- lepsza wydajność;
- wyższa niezawodność;
- mniejszy rozmiar systemu;
- niższy koszt systemu.

Choć można powiedzieć, że odbiornik jednoprocesorowy w pewnym sensie zakończył ewolucję odbiornika DTMF, to staje się on coraz bardziej komponentem podsystemu zarówno w układach hybrydowych, jak i monolitycznych, w których odbiornik DTMF funkcjonuje jako element składowy. Takie komponenty, podobnie jak w innych obszarach, w których VLSI jest wykorzystywany do granic możliwości, będą niezbędne

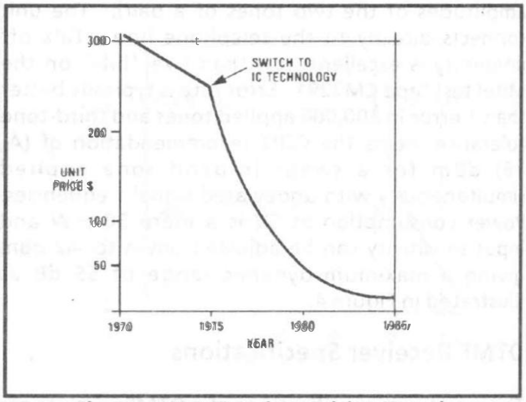

Fig. 7 - Trendy cenowe odbiornika DTMF

wysoce wyspecjalizowany pod kątem zamierzonego zastosowania (np. radiotelefony, zdalne sterowanie, odbiorniki danych itp.).

Trendy cenowe

Operatorzy telefoniczni przyspieszyli konwersję swojego sprzętu na wybieranie tonowe. Powodem tego jest to, że oprócz dodatkowej wygody sygnalizacji DTMF, koszt instalacji DTMF jest szybko amortyzowany przez dodatkowe przychody dostępne na linii DTMF. Postęp w projektowaniu i przyjęcie MOS/LSI co roku obniżają cenę. Do wygenerowania krzywej cenowej pokazanej na rysunku 7 wykorzystano rzeczywiste liczby. Przyszłe ceny można przewidzieć na podstawie postępu projektowego i trendów cenowych zarówno w branży telekomunikacyjnej, jak i półprzewodnikowej.

Zgodnie z tą krzywą, cena odbiornika poniżej $10 została już przewidziana na 1985 r., chociaż inflacja działa w przeciwnym kierunku. I należy podkreślić, że mówimy o w pełni przetestowanym produkcie w pojedynczym, kompaktowym opakowaniu.

Na to zjawisko wpływają cztery główne czynniki:

1. Wzrost konkurencji pomiędzy producentami odbiorników DTMF.
2. Przejście na technologię MOS/LSI, wykorzystując w ten sposób zalety krzywych cenowych półprzewodników.
3. Akceptacja przez firmy telekomunikacyjne nowszych technologii i redukcja cyklu zamówień.
4. Powstawanie nowych aplikacji dla sygnalizacji DTMF.

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An Alternative to Modems?

The emerging new application areas for DTMF signalling deserve some special consideration, as it is these applications which are today being stimulated by the cost-effectiveness of the DTMF approach and which will in turn benefit as growing volume pushes receivers further down the pricing curve.

Today, DTMF receivers are found primarily in central office and PABX equipment, where the two principal applications are in the reception of dialled pulse or tone pulse codes (Figure 8). Diminishing costs are now permitting the use of receivers at the subscriber end of the installation, transforming the standard voice channel into an economical means of data transmission. The attractiveness of this approach lies in the fact that data may be entered through any standard (DTMF) telephone keypad, eliminating the need for modems, acoustic couplers and other specialized interfacing equipment. Without specialized subscriber equipment, DTMF data transmission is one way only and has limited transmission speed and character-set compared to modem solutions but many applications exist where these shortcomings do not impose a limitation on system performance. Such applications would be characterized as requiring only a numeric data (plus possibly the 2 to 6 extra codes embodied in the DTMF specification); as requiring only a moderate data rate (e.g. when data speed is limited by speed of operator input); and as being either 'one-way' or else susceptible to some alternative means of data reception (such as achieved by voice synthesis). Many applications of this sort are emerging in fields extending well beyond the telecommunications industry itself.

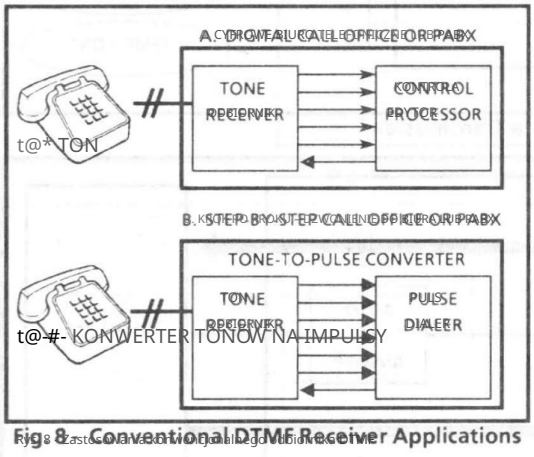

Fig. 8 Conventional DTMF Receiver Applications

New DTMF Receiver Applications

DTMF technology lends itself to a variety of remote-control applications, in the home (control of heating appliances, pay-television, etc.) and in industry (control of remotely located installations such as data loggers, radio transmitters, pumping stations, etc.). The only added expense is at the controlled location (auto answer receiver, security logic and controller), the controlling location may be any DTMF telephone including call boxes and radiotelephones. Certain of these remote control applications will benefit from the low power consumption of CMOS technology. Remote data-entry is an application which benefits from the concept of data input through any telephone. For example, a salesman on the road may enter his orders directly into a central computer from any convenient location without specialized portable equipment, eliminating equipment and maintenance costs and enhancing user convenience. All that is required is a DTMF receiver installation at the central computer, with the appropriate interface software. A similar application might allow an individual to order goods via his telephone keypad.

Remote control and data-entry are two applications requiring essentially 'one way' data transmission (Figure 9), although some audible response would normally be implemented to confirm to the user that correct data has been entered. A more sophisticated approach (Figure 10) would be where some two-way call progression is required to give a more detailed response. This concept is typified by an application such as credit card verification, where a central computer must provide a confirmation number in response to a keyed-in card number. The existing voice-synthesis, which maintains cost and convenience advantage of eliminating specialized equipment at the point of sale. This technology may allow the introduction of the functions of today's 'electronic banking' directly into the home, again without additional subscriber equipment.

One of the installations which may conveniently be connected to a remote telephone is the answering machine. The user may command replay of messages and update his own recorded message at will. The machine may also be programmed to store messages intended for specific callers only and activated by a pre-arranged code keyed in by the caller. An economical all-solid state answering machine may follow the concept of storing a 'follow me' telephone number updated remotely through DTMF signalling and played back to callers in voice synthesis.

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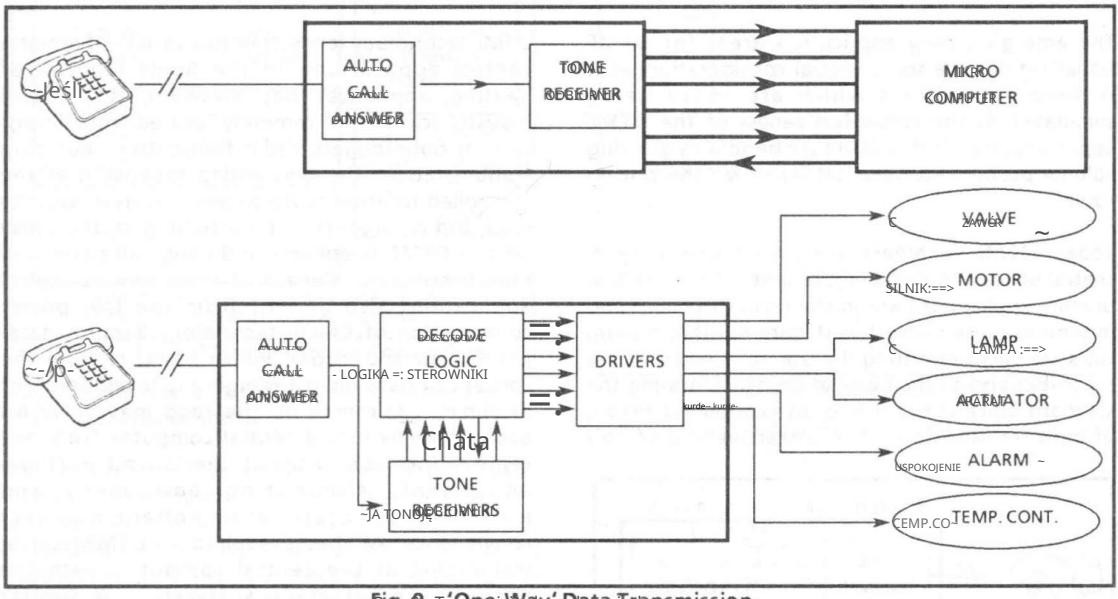

Fig. 9 - 'One-Way' Data Transmission

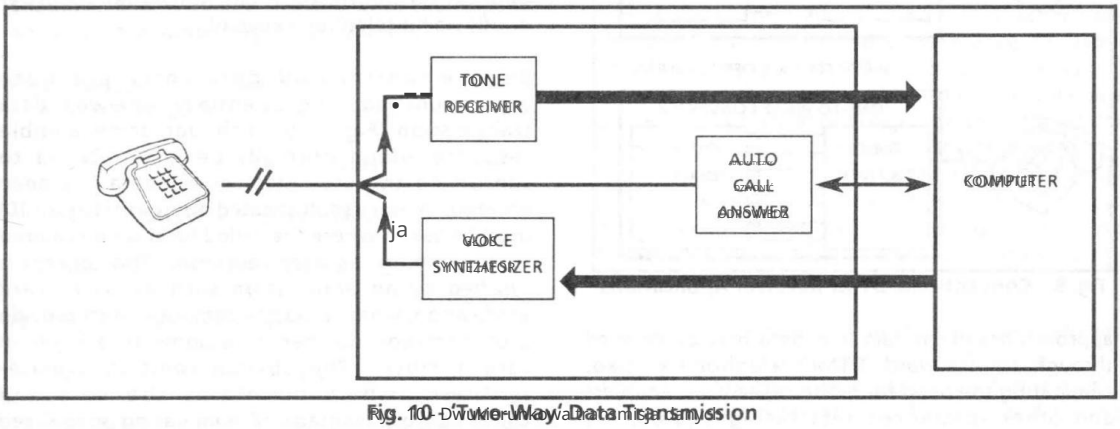

Fig. 10 - Two-Way Data Transmission

One of the more exciting of domestic applications is the home communications system which brings together telephone, intercom, appliance control, answering machine and home computer in one integrated network. Accessing such a system from any remote telephone clearly adds flexibility to the concept, and might even be applicable to two-way communication between home computers.

Although some of the major benefits of DTMF signalling stem from an extension of the utility of existing telephone installations, its power and reliability would allow it to be used in any multiple-location signalling network (Figure 11) such as might be found in industrial control systems. The system does not necessarily have any interface to the telephone network but must operate reliably over long distances in the presence of noise and other disturbances. In such an off-line network, the designer has the flexibility to adjust signalling parameters, such as tone durations and amplitudes, to conform to his specific application needs.

DTMF signalling is also being extended into mobile-radio telephone applications (Figure 12). This allows the radio link to 'plug in' transparently to the telephone network, simplifying the interface, and the same DTMF encoding may be used to transmit channel and other information to and from the mobile. Noise and talk-off considerations are rather different in radiotelephone networks, and adjustment of timing parameters can be made to optimize performance in this environment.

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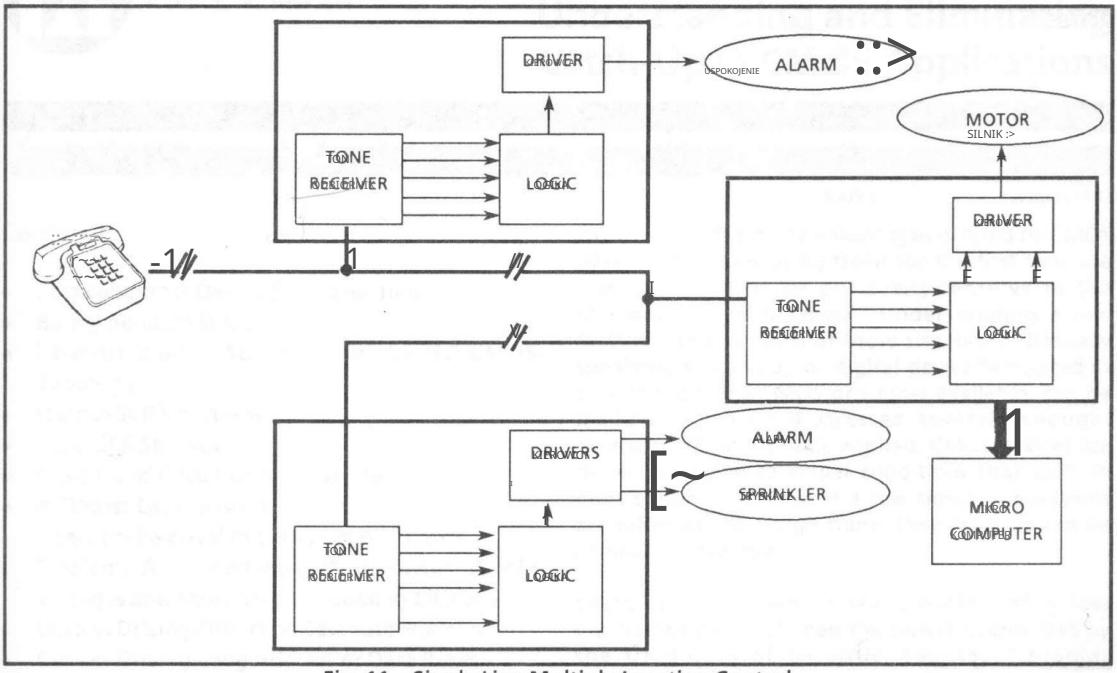

Fig. 11 Single Line Multiple Location Control

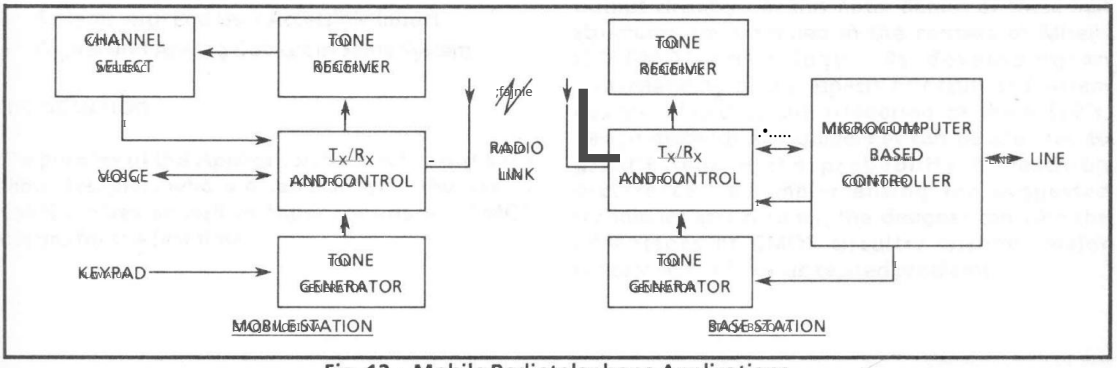

Fig. 12 Mobile Radiotelephone Applications

Conclusion

A description of the DTMF signalling medium has been presented, its main features both for conventional dialing applications and for certain data transmission and remote control applications. An overview of the "state of the art" as illustrated by the Mitel DTMF receivers has shown the benefits of performance, cost and size which are now available.

Usage of DTMF signalling is enjoying an explosive growth, driven primarily by three interacting factors:

1. Increased cost-effectiveness due to LSI implementation.
2. General availability of an input medium (the subscriber telephone).
3. Existence of complementary technologies (such as voice synthesis).

It remains to be seen what other new applications will be stimulated by the availability of the DTMF signalling medium.

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NOTES:

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MITEL

Application Note MSAN-107

Understanding and Eliminating Latch-Up in CMOS Applications

ISSUE 1 August 1982

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Introduction

The purpose of this Application Note is to assist both designers familiar with the use of CMOS devices, as well as those designing CMOS for the first time, in understanding a few facts with respect to latch-up in CMOS circuits. Basically, latch-up is defined as the creation of a low impedance path between the power supply rails by the triggering of parasitic four layer bipolar structures (SCR's) inherent in CMOS output circuitry. In this note, details of these SCR structures are examined in the context of Mitel's ISO-CMOS technology. By providing an understanding of the aspects necessary to minimize system design problems related to the triggering of these SCR's, design methods and guidelines can be acquired to greatly reduce the probability of latch-up occurrence. By implementing the suggested techniques and circuitry, the designer can gain the advantages of CMOS circuitry without major concern about latch-up related problems.

- Rozważania dotyczące półprzewodnikowych przyrządów
- Informacje ogólne na temat SCR
- Pasożytnicze bipolarne struktury w topologii ISO-CMOS
- Inne struktury SCR
- Struktury wejściowe
- Układy i rozważania dotyczące układów
- Układ "najgorszego przypadku"
- Usuwanie zatrzasku
- Problemy związane z wieloma zasilaczami
- Napięcia i związane z nimi układy odsprzęgające
- Urządzenia sterujące innymi na oddzielnych płytkach PCB
- Urządzenia sterujące długimi magistralami adresowymi lub danych
- Kable taśmowe - przypadek szczególny
- Systemy z dostępnymi dla użytkownika końcowego wejściami
- Układy cyfrowe i analogowe w tym samym systemie

Wstęp

Celem niniejszej noty aplikacyjnej jest pomoc projektantom zarówno zaznajomionym z urządzeniami CMOS, jak i tym, którzy po raz pierwszy projektują układy CMOS. Przyglądając się kilku faktom dotyczącym zatrzasku w układach CMOS, omówiono podstawowe problemy związane z zatrzaskiem. Zasadniczo zatrzask definiowany jest jako utworzenie niskoimpedancyjnej ścieżki pomiędzy szynami zasilającymi poprzez wyzwolenie pasożytniczych czterowarstwowych bipolarnych struktur (SCR), które występują w obwodach wyjściowych CMOS. W niniejszej nocie szczegóły tych struktur SCR są badane w kontekście technologii ISO-CMOS firmy Mitel. Zrozumienie aspektów projektowania układów związanych z wyzwalaniem tych SCR pozwala projektantowi na zastosowanie technik projektowania i wytycznych, które znacznie zmniejszają prawdopodobieństwo wystąpienia zatrzasku. Stosując sugerowane techniki i układy, projektant może uzyskać zalety układów CMOS bez większych obaw o problemy związane z zatrzaskiem.

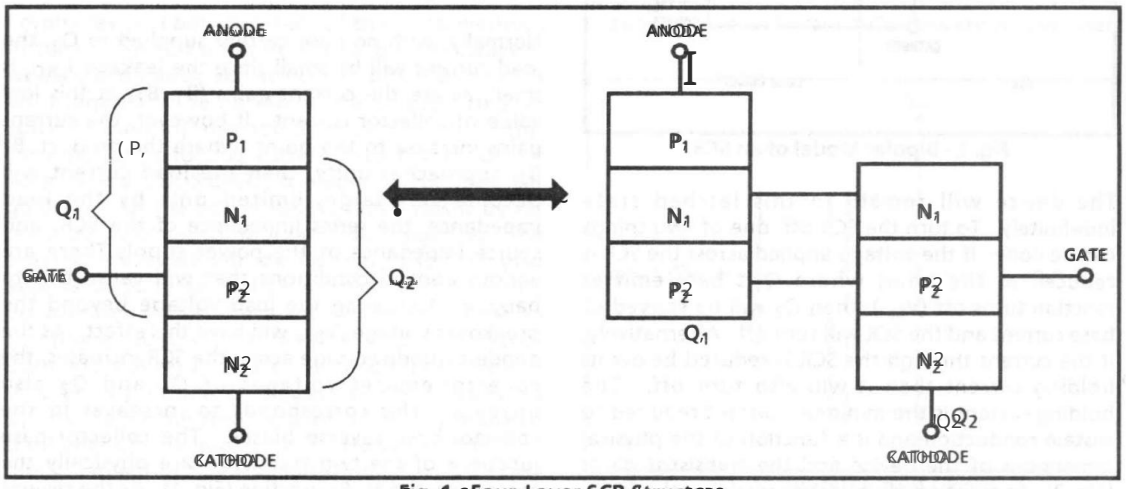

Fig. 1 - Four Layer SCR Structure

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Semiconductor Device Considerations

Background on SCR's

Prior to discussing latch-up in CMOS devices, it is advantageous to briefly review the basic theory of SCR operation. This will be helpful in developing an understanding of the relationships between external circuit conditions and the resultant triggering of latch-up in CMOS devices. The basic SCR structure is that of four-layer device as shown in Fig. 1 where the device has three terminals: Anode, Cathode and Gate. Fig. 2 shows how the SCR can be modelled with two bipolar transistors, one NPN and one PNP. In the normal mode of operation, the SCR is turned on by injecting sufficient current into the base of Q_2 to turn this transistor on. When this is done, Q_2 begins to draw collector current via the base-emitter junction of Q_1. As a result Q_1 also turns on, injecting additional current into Q_2's base. This in turn causes Q_2 to turn on harder, supplying more base current to Q_1. This positive feedback arrangement sustains conduction, and ensures that the SCR continues to conduct even if the gate current is interrupted.

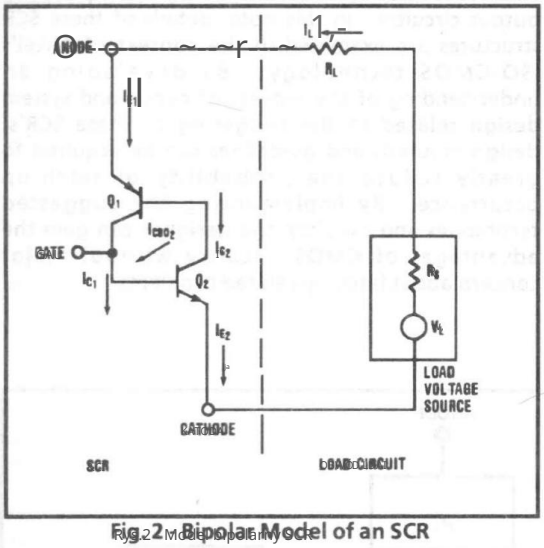

Fig. 2 - Bipolar Model of an SCR

The device will remain in this latched state indefinitely. To turn the SCR off, one of two things can be done. If the voltage applied across the SCR is reduced to the point where the base-emitter junction turns off (V_{BE} = 0), then Q_2 will be starved of base current and the SCR will turn off. Alternatively, if the current through the SCR is reduced below its holding current then it will also turn off. The holding current is the minimum current required to sustain conduction and is a function of the physical dimensions of the device and the transistor gains (Fig. 3). As mentioned, this is the way that the SCR is controlled in normal applications. There are various other ways that an SCR may be triggered. These must be examined as they are directly related to latch-up problems.

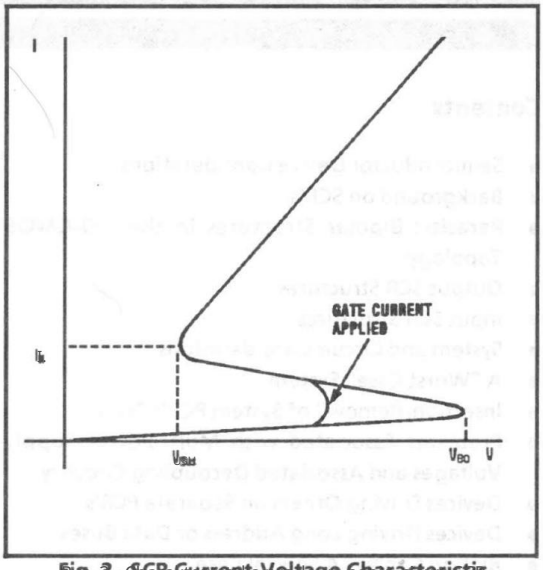

Fig. 3 - SCR Current-Voltage Characteristic

Looking at Fig. 2, it can be seen that the load current and the two emitter currents of Q_1 and Q_2 are all equal. Also the load current is equal to the sum of the two collector currents and a leakage current from Q_2's collector to its base (I_{CBO_2}). It can be shown (refer to Appendix) that:

$$I_L = I_{CBO_2}\left[\frac{(1+B_1)(1+B_2)}{(1-B_1B_2)}\right] \quad (1)$$

Where B_1 and B_2 are the current gains of Q_1 and Q_2 respectively.

Normally, with no base current supplied to Q_2, the load current will be small since the leakage I_{CBO_2} is small as are the current gains (B_1, B_2) at this low value of collector current. If however, the current gains increase to the point where the product, B_1 B_2, approaches unity, then the load current will become very large, limited only by the load impedance, the series impedance of the SCR, and source impedance of the power supply. There are various applied conditions that will cause this to happen, increasing the load voltage beyond the breakover voltage, V_{BO}, will have this effect. As the anode-cathode voltage across the SCR increases, the collector-emitter voltages of Q_1 and Q_2 also increase. This corresponds to increases in the collector-base reverse biases. The collector-base junctions of the two transistors are physically the same area, the N_1-P_2 junction (Fig. 1). As the reverse

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bias increases, the energy of the majority carriers increases, causing energy carriers to be dislodged, which, in turn pick up energy. This continues until the junction undergoes an avalanche breakdown resulting in an increase in the collector currents of Q_1 and Q_2. The resulting increase in B_1 and B_2 cause the SCR to latch on.

A very rapid change in the anode to cathode voltage of an SCR can also cause it to trigger. This is known as the "dV/dt" effect. The N_+P_- junction being reverse biased exhibits a capacitance. This capacitance varies with the reverse bias voltage applied across the junction. Hence the current through the capacitor is described by:

$$\frac{d(C_j V_{AK})}{dt} \quad (2)$$

$$= \frac{C_j dV_{AK}}{dt} + \frac{V_{AK} dC_j}{dt} \quad (3)$$

The junction capacitance, C_j decreases with increasing reverse bias and hence the second term of equation (3) is negative. If, however the rate of change of applied voltage is large enough the first term of equation (3) will dominate and the current through the SCR will increase. If the current increases sufficiently to cause the B_1B_2 product to approach unity, then the SCR will latch on.

When considering temperature effects, an increase in temperature will cause an increase in both the leakage currents through the SCR and in the current gains B_1, B_2 of the two bipolar transistors. As such the magnitude of the driving force required to turn the SCR on will decrease with increasing temperature. In other words, the SCR will be more easily triggered as temperature increases for any of the triggering mechanisms described.

Several different methods exist to trigger each of the SCR devices. Each of these methods of turning an SCR on, as described, and the ways in which the parasitic SCR structures of CMOS devices are triggered, will be examined in the next section in the context of the ISO-CMOS topology for both the output and input structures.

Parasitic Bipolar Structures in the ISO-CMOS Topology

As with any CMOS technology, ISO-CMOS contains certain parasitic bipolar structures associated with its output devices and input protection circuitry. These parasitic transistors are interconnected in such a way as to form four layer devices. As such, SCR devices are present at both the inputs and outputs of ISO-CMOS circuits. These devices are normally in their off state and will remain off as long as the absolute maximum ratings of the devices are not exceeded.

Output SCR Structures

A typical ISO-CMOS output driver contains one N-channel MOSFET with its source tied to V_{SS} and one P-channel MOSFET with its source tied to V_{DD}. The drains of the two transistors are connected together to form the output and the gates are commoned to form the input (Fig. 4). The fabrication of these transistors in close proximity results in the formation of a parasitic SCR connected directly across the power supply rails. When triggered, this SCR presents a low impedance to the power supply causing excessive current to flow. This situation is potentially destructive, resulting in damage to bond wires or metal supply tracks on the die due to localized overheating. The SCR is formed as follows. A vertical NPN transistor results from the fabrication of the N-channel device. The N- substrate serves as the collector and is biased at V_{DD}. The P- well acts as the base and the source and drain N+ diffusions are the emitters of the transistor. One emitter is tied to V_{SS} and the other to the output. A wide base lateral PNP transistor is formed when a P-channel device is located close to a N-channel transistor. The P-channel source and drain diffusions are two emitters

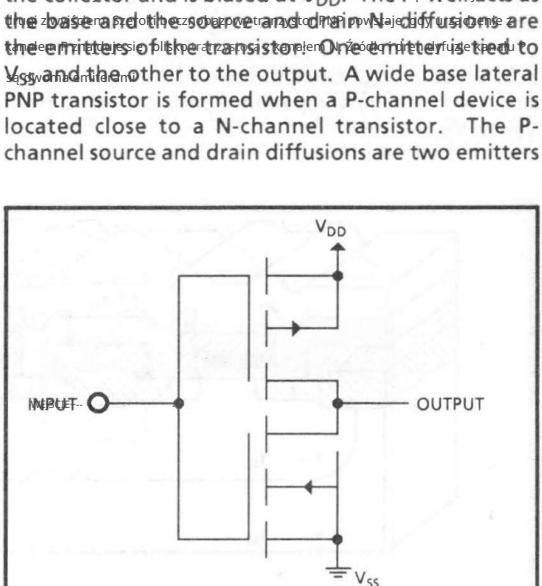

Fig. 4 Typical Output Circuit

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of the transistor is connected to V_{DD} and the other to the output. The N substrate acts as the base and hence is in common with the collector of the vertical NPN. The P well is the collector of the PNP which is also base of the NPN. Due to the shared diffusions, the vertical NPN and lateral PNP transistors are effectively connected as an SCR (Fig. 5). This parasitic SCR is connected directly across the supply rails. Hence, when triggered, it can cause excessive current to flow. The SCR is normally turned off for normal operating supply voltages and with all output voltages within the power supply limits. This SCR may be externally triggered causing the output structure to latch-up. The triggering mechanism can be any one of those mentioned in the previous section.

Output voltages being forced outside of the power supply limits is the most common cause of output latch-up. Two parameters are defined at this point for use in subsequent discussions. These are V_{trg} and V_{hold}. V_{trg} is the current which must flow through the output structure to cause latch-up to occur. V_{trg} is the voltage excursion outside of the power supply rails at the output pin that results in I_{trg} flowing through the output structure. In other words, I_{trg} and V_{trg} are the conditions at the output that will result in latch-up triggering. These same parameters also apply to input latch-up (see next section). Consider first an output voltage which goes below V_{SS} by more than V_{trg}. This causes the P-well to output base-emitter junction of the vertical NPN transistor to become forward biased. Since this acts as the SCR gate, triggering occurs. Current is pulled from V_{DD} through the lateral PNP and is injected into the P- well, causing a localized drop across this diffusion. This voltage drop will forward bias the base-emitter junction of the NPN which is referenced to V_{SS}. Once this occurs, latch-up will be sustained and a low impedance path is created from V_{DD} to V_{SS}.

A note must be taken here in regard to the amount of over voltage required to trigger latch-up. In the above paragraph, it was mentioned that voltages exceeding the supply rails by more than V_{trg} will cause a current I_{trg} to flow and hence trigger latch-up. The guaranteed values quoted in the data sheet are 0.3V and 10mA respectively for these parameters. These limits are used in production testing and hence appear in the Absolute Maximum Ratings of MITEL devices. In practice, it is more likely to require from 0.6V to 2V of overvoltage and from 50 to several hundred milliamps of current to cause output latch-up to occur. For input latch-up to occur, it can take several volts of over-voltage and similar currents to induce latch-up due to the series resistance of the input protection circuitry (Fig. 6).

When the V_{DD} supply rail is exceeded by a voltage greater than V_{trg}, a similar set of events occurs. In this case, the output to substrate base emitter junction of the lateral PNP becomes forward biased. Collector current from this transistor injected into the P well, again causing a lateral voltage drop. This voltage drop causes the P- well to V_{DD} referenced base-emitter junction of the NPN to become forward biased. This creates a low impedance path between the output and V_{SS}. Current pulled from the substrate causes a lateral voltage drop across the substrate. This voltage drop, in turn, will forward bias the V_{SS} to substrate base-emitter junction of the PNP. Thus latch-up will be sustained even if the output over voltage condition is removed and a low impedance path again exists between V_{DD} and V_{SS}.

There are two other causes of output latch-up that are less likely to occur, but nonetheless must be noted. The first of these is the result of over-voltages on the power supply pins. Excessive voltage between V_{DD} and V_{SS} (i.e. greater than the absolute maximum rating) can cause an avalanche breakdown of the reverse biased substrate to P- well collector base junction of the bipolar transistors.

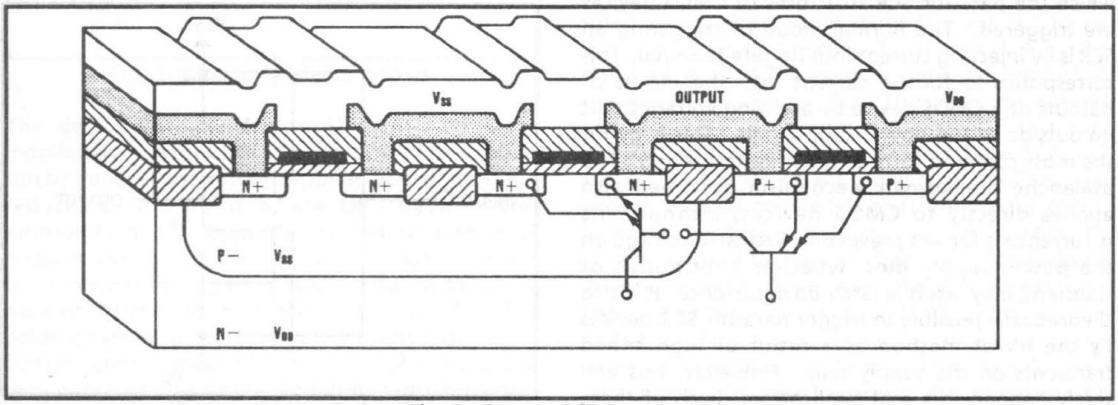

Fig. 5 Output SCR Structures

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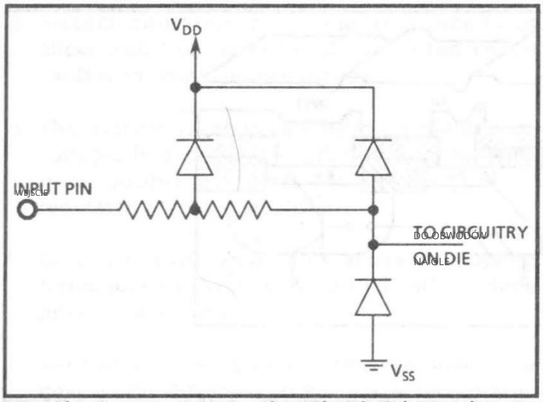


Rys. 6 Schemat obwodu ochrony wejściowej

Spowoduje to wyzwolenie SCR , jak opisano w poprzedniej sekcji. Drugi mechanizm wyzwalania bę dzie widoczny w bardzo niewielu systemach. Bardzo szybkie skoki napię cia na szynach zasilania mogą wywołać wyzwolenie SCR „dV/dt” , jak również opisano wcześniej. Może to potencjalnie spowodować uszkodzenie obwodu przez stany przejściowe , które same w sobie nie miałyby wystarczającej energii, aby spowodować uszkodzenie z powodu lokalnego rozproszenia mocy. Po wyzwoleniu SCR może pozostać zablokowany, dopóki napię cie zasilania nie spadnie poniżej napię cia podtrzymującego lub jeśli prąd nie spadnie poniżej prądu podtrzymującego .

Wprowadź SCR Structures

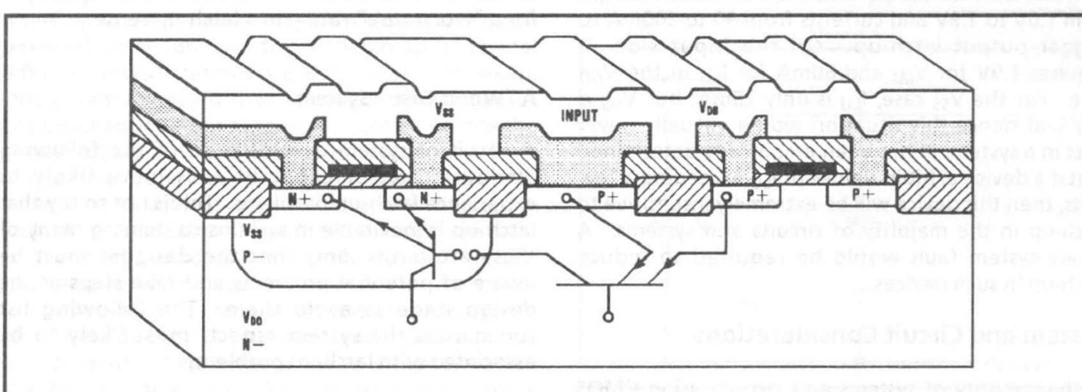
Struktury pasożytnicze SCR mogą również powstawać w wyniku produkcji obwodów zabezpieczających CMOS input . Schemat obwodu zabezpieczającego ISO-CMOS input pokazano na rys. 6. Jak pokazano, istnieje rozproszona dioda podłączona do Voo i inna dioda do Vss.

Rezystor szeregowy przeznaczony jest przede wszystkim do ochrony przed ładunkami elektrostatycznymi , ale zapewnia również ochronę przed zatrzaskiwaniem . Diody są połączone ze sobą w wę źle wejściowym. Struktura SCR powstaje, gdy dioda odniesienia Voo jest wytwarzana w bliskim sąsiedztwie tranzystora N-kanałowego (rys. 7) lub gdy dioda odniesienia Vss znajduje się w pobliżu elementu P-kanałowego (rys. 8).

Ważne jest, aby zwrócić uwagę na różnicę mię dzy strukturami SCR wejściowymi i wyjściowymi. SCR wyjściowy był podłączony bezpośrednio mię dzy Voo i Vss, a zatem jest bardziej prawdopodobne, że bę dzie destrukcyjny po wyzwoleniu. Struktura SCR wejściowy jest podłączona od wę zła wejściowego do jednej z szyn zasilających. Zatem, aby wejście pozostało zablokowane, obwód sterujący wejściem musi być zdolny do dostarczania prądu podtrzymującego SCR . Aby to zablokowanie było destrukcyjne, sterownik wejściowy musi być zdolny do dostarczania dużych ilości prądu. Potencjalnie bardziej niebezpieczna sytuacja ma miejsce, gdy tranzystor uzupełniający, do tego tworzącego SCR, znajduje się w pobliżu. W rezultacie powstaje wtórna struktura SCR , która jest podłączona przez szyny zasilające (rys. 7 i 8).

Najpierw rozważmy sytuację z diodą odniesioną do Vss Dyfuzje źródła i drenu tranzystora kanału P tworzą emitery bocznego tranzystora PNP. Podłoże działa jako baza, a dyfuzja P diody jest kolektorem. Ta dioda, z podłożem, tworzy pionowy tranzystor NPN.

Oba tranzystory są połączone jako SCR ze wzglę du na wspólne obszary dyfuzyjne. Jeśli napię cie wejściowe jest niższe od Vss o wię cej niż VLU, złącze bramka-katoda SCR zostanie spolaryzowane w kierunku przewodzenia i obróci SCR on. Ten stan zatrzasku bę dzie trwał tak długo, jak długo bę dzie trwał ten stan wejściowy lub jeśli obwód wejściowy bę dzie mógł dostarczyć minimalny prąd podtrzymujący. Jak wspomniano, potencjalnie bardziej niebezpieczna sytuacja może się rozwinąć, jeśli w pobliżu znajduje się również tranzystor z kanałem N. Studnia P tego tranzystora służy jako drugi kolektor otbocznego tranzystora PNP. Gdy napię cie wejściowe staje się ujemne, bramka SCR włącza się , jak wspomniano. Jednak ten drugi kolektor teraz wstrzykuje prąd do studni P, powodując drugi



Rys. 7 Wprowadź SCR Structure za pomocą Voo Diode

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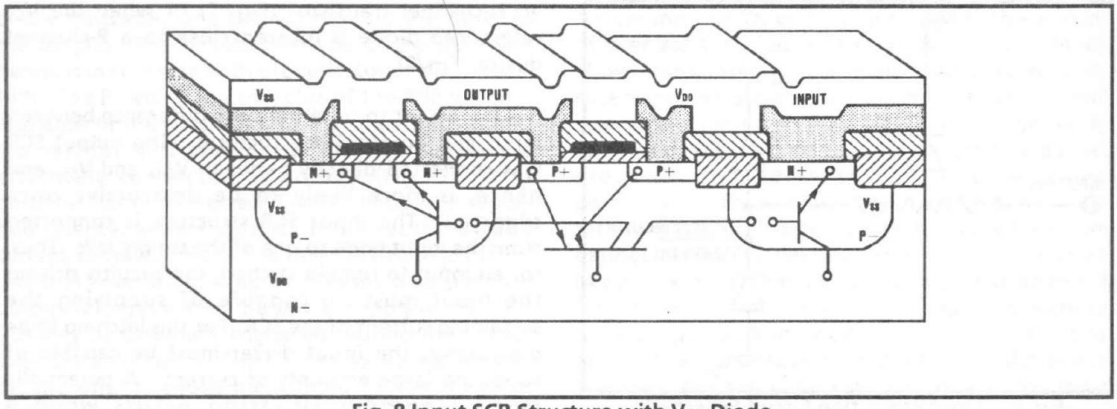

Fig. 8 Input SCR Structure with V_{SS} Diode

Forced I/O Condition	Latch-Up Inducing Conditions	
	V_{LU} (Volts)	I_{LU} (mA)
Outputs above V_{DD}	1.9	200
Outputs below V_{SS}	1.0	90
Inputs above V_{DD}	1.9	80
Inputs below V_{SS}	2500	25

Table 1 MD74SC540AC Latch-Up Inducing Voltages and Currents

SCR structure is latch-up. This device is connected across the power supply rails and hence can be destructive. This same situation can result with the V_{SS} referenced protection diode. In this case, SCR structures will be triggered by voltages which exceed V_{DD} by more than V_{LU}.

As was mentioned earlier, the actual values of V_{LU} and I_{LU} are typically much greater than the 0.3V and 10mA limits given in the data sheets. Table 1 shows some of the typical values obtained from a CMOS octal version of the MD74SC540AC device. As can be seen, the V_{DD} case. For the V_{SS} case, I_{LU} is only 25mA, but V_{LU} is 2.5V and, hence this situation would virtually never exist in a system. It has been empirically determined that if a device exhibits values of I_{LU} exceeding a few volts, then this device will be extremely insensitive to latch-up in the majority of circuits and systems. A severe system fault would be required to induce latch-up in such devices.

System and Circuit Considerations

In the majority of systems and circuits using CMOS devices, latch-up should not be a major cause for concern. Being aware of the causes of latch-up problems will aid the designer in even further reducing the probability of latch-up damage to his circuits. Implementing some of the precautionary measures suggested in the following sections will ensure a trouble-free system.

The aspects of system and circuit design that can result in latch-up occurrence will be examined in the context of a "worst case" system example. In other words, systems containing combinations of the attributes of this example system will be more likely to experience latch-up problems. The relationships between these systems aspects and the resultant latch-up triggering mechanisms will be described. Suggestions will be made intent upon reducing the risk of triggering the parasitic SCR's through careful design techniques. The protection circuits which will be illustrated should help in preventing circuit damage in case latch-up occurs. It should be noted at this point that in systems where the inputs and outputs will never be taken outside of the power supply rails either during power-up or in continuous operation, latch-up is not likely to ever occur. The first step then is to define a system which contains various components that qualify it for a "worst case" rating in a latch-up sense.

A "Worst Case" System

A circuit or system which has all of the following attributes and/or capabilities is more likely to experience latch-up problems. This is not to say that latch-up is inevitable in systems containing many of these attributes, only that the designer must be aware of potential problems and take steps at the design stage to avoid them. The following list summarizes the system aspects most likely to be associated with latch-up problems:

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1) System operation/maintenance procedures allow insertion or removal of printed circuit cards with system power applied.

2) The system is powered by multiple supply voltages (e.g. +12V, +5V and Gnd) or has a multi-supply at same voltage (e.g. +5V regulated, +5V unregulated).

3) Circuits utilize complex capacitive decoupling techniques particularly associated with multiple power supply voltages.

4) Integrated circuits on one system PCB drive other devices on different PCB's via a backplane, ribbon cable, etc.

5) Devices drive high capacitive loads such as long data or address busses.

6) System contains high speed address and/or data busses of sufficient length to cause their inductive properties to become significant at the frequencies in question (ribbon cables are a prime example).

7) System has electronic circuits that are directly accessible by the end user of the system.

8) Digital devices are driven from analog devices powered from power supply voltages, utilizing input diodes for clamping.

Each of the above criteria will now be examined in terms of its potential for triggering latch-up. The first four items are very interdependent. While each of these will be given consideration in separate sections, cross referencing will be extensive. The remaining items are relatively independent and thus, will be looked at in relative isolation.

Insertion/Removal of System PBC's "Live"

Inserting or removing printed circuit cards from a powered up system can trigger latch-up in several different ways if certain precautions are not taken. One potential hazard that can occur is for an input or output edge terminal to make contact before the power supply pins are connected. If driven by a device on another circuit card, this input/output pin could have a voltage applied with no supply voltage to the device. Even if this situation exists only briefly (typically <1 second), latch-up may be triggered when the power supply pin is connected. It is important to note that three state outputs are also vulnerable in this situation. Such output drivers typically present high impedances to voltages within the device supply rails. Voltages on these outputs exceeding the supply can indeed trigger latch-up.

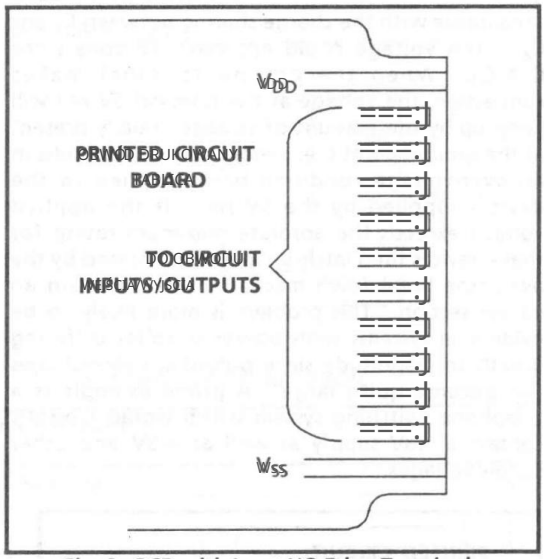

Fig. 9 PCB with Inset I/O Edge Terminals

One solution to this problem is to slightly extend the power supply terminals with respect to the remaining edge terminals on the PCB (Fig. 9). This will ensure that power supply connections are the first made and last broken on insertion and removal of the PCB respectively.

Plugging a circuit card live into a system with multi-power supply voltages can result in the application of power supply overvoltages to certain devices. Consider the local decoupling scheme shown in Fig. 10. If a PCB containing such decoupling was plugged into a system live, then the following situation could result. Assume that all capacitors are discharged and that C_1 is much greater than C_2. It is possible that when the PCB is inserted, the +12V terminal makes connection first, then the ground, and lastly the +5V connection is made. In this situation, C_1 and C_2 are momentarily connected in series. The +12 volts applied to C_1 causes the voltage at the ground point to increase in

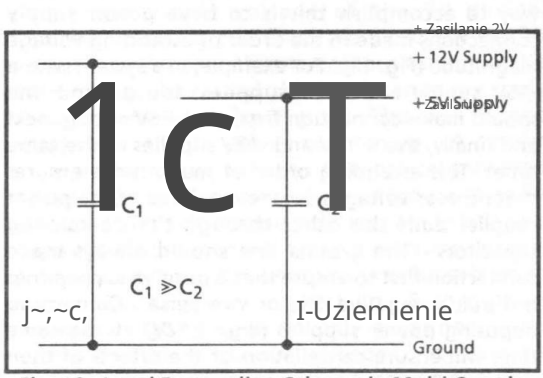

Fig. 10 Local Decoupling Scheme in Multi Supply System

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accordance with the charge sharing between C_L and C_C. This voltage could approach 12 volts since $C_L \gg C_C$. When the ground terminal makes connection the voltage at the nominal 5V rail will jump 12V) by the amount of voltage initially present at the ground point (i.e. almost 12V). This results in an over-voltage condition being applied to the devices supplied by the 5V rail. If the applied voltage exceeds the absolute maximum rating for these devices then latch-up may be triggered by the avalanche breakdown mechanism described in an earlier section. This problem is more likely to be evident in systems with power supplies differing greatly in magnitude since potential over voltages can become quite large. A prime example is a telephone switching system which would typically contain a -48V supply as well as +5V and other supply voltages.

zgodnie z podziałem ładunku pomiędzy C_L a C_C. Napięcie to może zbliżać się do 12 woltów, ponieważ $C_L \gg C_C$. Gdy zacisk uziemienia zostanie podłączony, napięcie na znamionowej szynie 5V podskoczy o wartość napięcia na początkowo obecnego w punkcie uziemienia (tj. prawie 12V) i to ujemne przepięcie zostanie przyłożone do zasilanych przez szynę 5V urządzeń (tj. prawie 12V). Jeśli napięcie to przyłożone przekracza maksymalną wartość znamionową dla tych urządzeń, wówczas zatrzask może zostać wyzwolony przez mechanizm przebicia lawinowego opisany we wcześniejszej części. Jest to bardziej prawdopodobny w systemach z zasilaczami różniącymi się znacznie pod względem wielkości, potencjalne przepięcia mogą być dość duże. Najlepszym przykładem jest system przełączania telefonicznego, który zazwyczaj zawiera -48 V, a także +5 V i inne napięcia zasilania.

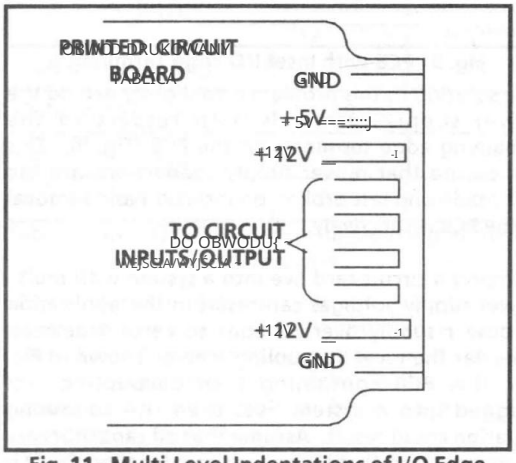

Fig.11. Multi-Level Indentations of I/O Edge Terminals

Rys.11. Wielopoziomowe wcięcia końcówek krawędzi dzielonych

This problem can also be overcome by indenting the edge terminals on PCB's. In this case there must be more than one level of indentation to ensure that the power supply connections are made in a sequence that will alleviate this problem. The safest way to accomplish this is to have power supply connections made in the order of ascending voltage magnitude (Fig.11). For example, in a system with a +5V supply and ±12V supplies, the ground line should make connection first, the +5V supply next and finally, the +12V and -12V supplies at the same time. This ascending order of magnitudes ensures that no over-voltages occur even if one of the power supplies pulls the other through the decoupling capacitors. The ground line should always make connection first to ensure that a positive supply does not pull a negative one or vice versa. Connecting opposing power supplies (e.g. ±12V) at the same time will ensure cancellation of the effects of their connection.

Ten problem można również przezwyciężyć poprzez wcięcie końcówek krawędzi dzielonych na PCB. W takim przypadku musi być więcej niż jeden poziom wcięcia, aby zapewnić połączenia zasilające w kolejności, która zaradzi temu problemowi. Najbezpieczniejszym sposobem osiągnięcia tego jest wykonanie połączeń zasilających w kolejności rosnącej wielkości napięcia (Rys. 11). Na przykład w systemie zasilanym +5V i ±12 V, linia uziemienia powinna zostać podłączona jako pierwsza, następnie zasilanie +5 V, a na końcu zasilanie +12 V i -12V w tym samym czasie. Ten rosnący porządek wielkości zapewnia, że nie wystąpią żadne przepięcia, nawet jeśli jedno z zasilaczy przeciągnie drugie przez kondensatory odsprzęgające. Linia uziemienia powinna zawsze zostać podłączona jako pierwsza, aby zapewnić, że dodatnie zasilanie nie przeciągnie ujemnego lub odwrotnie. Podłączanie przeciwnych zasilaczy (tj. ±12 V) w tym samym czasie zapewni anulowanie efektów ich połączenia.

In systems which have large number of power supplies to contend with it may not be feasible to provide the required number of indentations on the PCB. In this case a careful analysis of the decoupling used must be done to establish potential problem areas. Where possible decoupling capacitors on different supplies should be of equal magnitude. This will tend to minimize over-voltages dues to equal charge sharing between the capacitors. If after all possible precautions have been taken there is still a possibility of power supply over voltages occurring, then it may be necessary to provide some form of current limiting or local regulation to prevent circuit damage.

W systemach, w których występuje duża liczba zasilaczy, zapewnienie wymaganej liczby wgięć biegnących na płycie drukowanej może być niemożliwe. W takim przypadku należy przeprowadzić dokładną analizę zastosowanego odsprzęgania, aby ustalić potencjalne obszary problemowe. Jeśli to możliwe, kondensatory odsprzęgające na różnych zasilaczach powinny mieć równą wielkość. To zminimalizuje przepięcia dzięki równemu podziałowi ładunku między kondensatorami. Jeśli po podjęciu wszelkich możliwych środków ostrożności nadal istnieje możliwość wystąpienia przepięć w zasilaniu, konieczne może być zapewnienie jakiejś formy ograniczenia prądu lub lokalnej regulacji, aby zapobiec uszkodzeniu obwodu.

The simplest form of protection is to connect a resistor in series with the power supply (V_{DD} or V_{SS}) pin of the devices in question (Fig. 12a). The size of this resistor can be chosen to either prevent latch-up from occurring or to prevent circuit damage when latch-up does occur. If latch-up is to be prevented then the minimum resistor value is chosen as follows:

Najprostszą formą ochrony jest podłączenie rezystora szeregowo z pinem zasilania (VDD lub VSS) omawianych urządzeń (rys. 12a). Rozmiar tego rezystora można wybrać tak, aby zapobiec wystąpieniu zatrzasku lub uszkodzeniu obwodu, gdy zatrzask wystąpi. Jeśli zatrzask ma być zapobiegany, minimalna wartość rezystora jest wybierana w następujący sposób:

$$R = \frac{V_{Supply} - V_{DD_{Max}}}{I_{DD_{Max}}}$$

where V_{Supply} = Maximum Supply Voltage Generated

gdzie VSupply = maksymalne napięcie zasilania wygenerowane

$V_{DD_{Max}}$ = Absolute Maximum Rating for V_{DD}

Ocena bezwzględna dla V_{DD}

$I_{DD_{MAX}}$ = Supply Current at $V_{DD_{Max}}$

Prąd zasilania w $V_{DD_{Max}}$

This will ensure that $V_{DD_{Max}}$ is never exceeded at the device.

Dzięki temu będziesz mieć pewność, że $V_{DD_{Max}}$ nigdy nie zostanie przekroczony na urządzeniu.

To simply prevent damage due to latch-up, the resistor is chosen to limit the supply current to a few hundred milliamps at the maximum applied voltage. There are a few factors which must be taken into consideration when choosing the resistor. The source impedance of the power supply will be increased by the amount of the added resistance. This will result in a decrease in the current sourcing or sinking capacity of the device, depending on whether the resistor is in the V_{DD} or V_{SS} line respectively. There is also a corresponding increase in the output propagation delay, proportional to product of the protection resistor and the load capacitance. Finally there is a decrease in the noise immunity of the device proportional to the product of this resistor and the total instantaneous supply current (including the output currents). For devices such as the MD74SCXXX, it is recommended that this resistor be placed in the V_{DD} line as there is more available noise immunity for

Aby po prostu zapobiec uszkodzeniom spowodowanym zatrzaskiem, rezystor dobiera się tak, aby ograniczyć prąd zasilania do kilkuset miliamperów przy maksymalnym przyłożonym napięciu. Istnieje kilka czynników, które należy wziąć pod uwagę przy wyborze odpowiedniego rezystora. Impedancja źródła zasilania zostanie zwiększona o wartość dodanego oporu. Spowoduje to zmniejszenie pojemności źródła lub odbiornika prądu urządzenia, w zależności od tego, czy rezystor znajduje się w linii V_{DD} czy V_{SS}. Wystąpi również odpowiedni wzrost opóźnienia propagacji wyjściowej, proporcjonalny do iloczynu rezystora zabezpieczającego i pojemności obciążenia. Na koniec nastąpi zmniejszenie odporności na zakłócenia proporcjonalnego do iloczynu tego rezystora i całkowitego chwilowego prądu zasilania (w tym prądów wyjściowych). W przypadku urządzeń takich jak MD74SCXXX zaleca się umieszczenie tego rezystora w linii V_{DD}, ponieważ jest tam więcej dostępnej odporności na zakłócenia.

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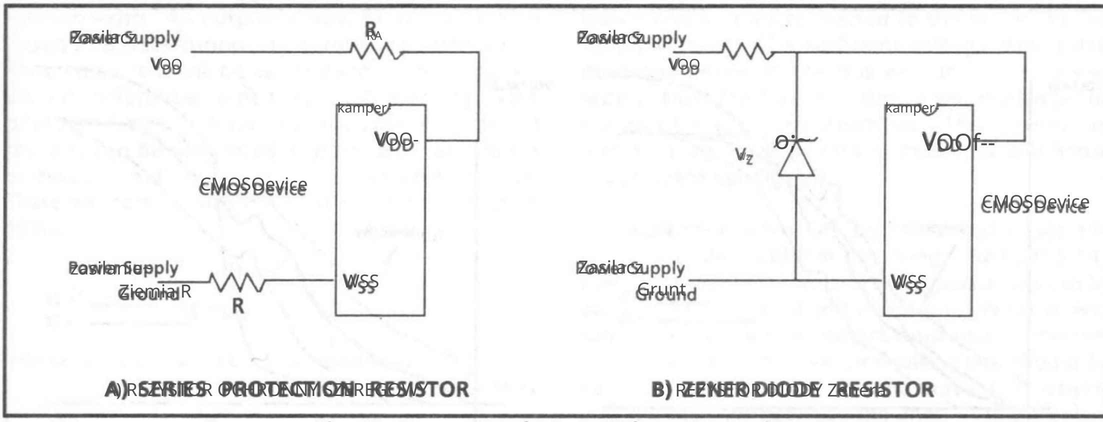


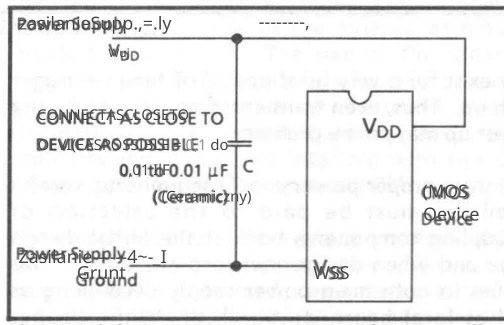
Rys. 12 - Zabezpieczenie przed przepięciem zasilacza

wyjścia wysokiego poziomu (podczas sterowania urządzeniami TTL lub innymi urządzeniami MD74SCXXX).

Jeśli rezystor ograniczający prąd nie może być użyty do ograniczenia prądu wyjściowego, prędkości lub odporności na zakłócenia, wówczas alternatywą jest podłączenie diody Zenera między VDD i VSS, aby zapobiec przepięciom urządzenia (rys. 12b). Rezystor ograniczający prąd może być nadal potrzebny, ale jego wartość może być bardzo mała, ograniczona jedynie przez zdolność przenoszenia mocy przez diodę Zenera.

Istnieje ostatnie potencjalne zagrożenie, które może powstać w wyniku „żywego" włożenia PCB. Na płytkach z niewielkim lokalnym odsprzęganiem, wkładanie karty może spowodować niezwykle szybkie stany przejściowe na przewodach zasilających urządzeń na płycie. Te stany przejściowe mogłyby teoretycznie spowodować zatrzaśnięcie z powodu efektu dV/dt opisanego wcześniej. Tego problemu można uniknąć, odsprzęgając zasilanie płyty za pomocą wystarczająco dużych kondensatorów, aby spowolnić wzrost napięcia zasilania, gdy płytka jest podłączona. Kiedy płyta musi zostać podłączona, należy wybrać takie rozwiązania, aby zapobiec problemowi przepięcia opisanemu powyżej.

Podobne przejściowe stany w zasilaczu mogą być generowane przez przełączanie szybkich, wysokoprądowych urządzeń, takich jak obwody ECL lub Schottky TTL, napędzających duże obciążenia pojemnościowe. Ponadto wsteczna SEM, generowana przez otwarcie obciążeń indukcyjnych, takich jak przekaźniki, może wywoływać nieduże skoki napięcia. Odpowiednie odsprzęganie wysokiej częstotliwości zwykle rozwiązuje ten problem. Ceramiczny kondensator 0,001 do 0,1 µF podłączony jak najbliżej urządzenia przez piny zasilania będzie odprowadzał wysokie energie o wysokiej częstotliwości (rys. 13). Zaleca się również podłączenie diod flyback w obciążeniach indukcyjnych w celu ograniczenia wstecznej SEM.



Rys. 13 - Odsprzęganie zasilania wysokiej częstotliwości

Problemy związane z wieloma napięciami zasilania i powiązanymi obwodami odsprzęgającymi

W systemach, które mają więcej niż jedno niezależne źródło zasilania, należy zadbać o zapewnienie prawidłowej kolejności sekwencji włączania i wyłączania zasilania, aby zapobiec stanom przepięć wejść-wyjść. Rozważmy na przykład urządzenie zasilane napięciem 5V, którego wyjścia są podłączone do urządzenia zasilanego z zasilacza 7V. W normalnych warunkach pracy poziomy wyjściowe urządzenia 5V będą mieścić się w zakresie napięcia zasilania urządzenia 7V. Jednakże, jeśli podczas włączania zasilanie 5V może przekroczyć zasilanie 7V, wówczas napięcie wyjściowe urządzenia 5V może przekroczyć napięcie zasilania urządzenia 7V (rys. 14). To przepięcie mogłoby spowodować zatrzaśnięcie urządzenia 7V. Podobna sytuacja może wystąpić, gdy urządzenia są zasilane z oddzielnych zasilaczy o równej wartości, takich jak regulowane zasilacze 5V, w przypadku niezależnego zasilania, gdy wyjścia są również podłączone. Takie wyjścia generują wysokie impedancje tylko dla sygnałów leżących w zakresie napięć zasilania. Należy podkreślić, że takie warunki przepięcia wymagają

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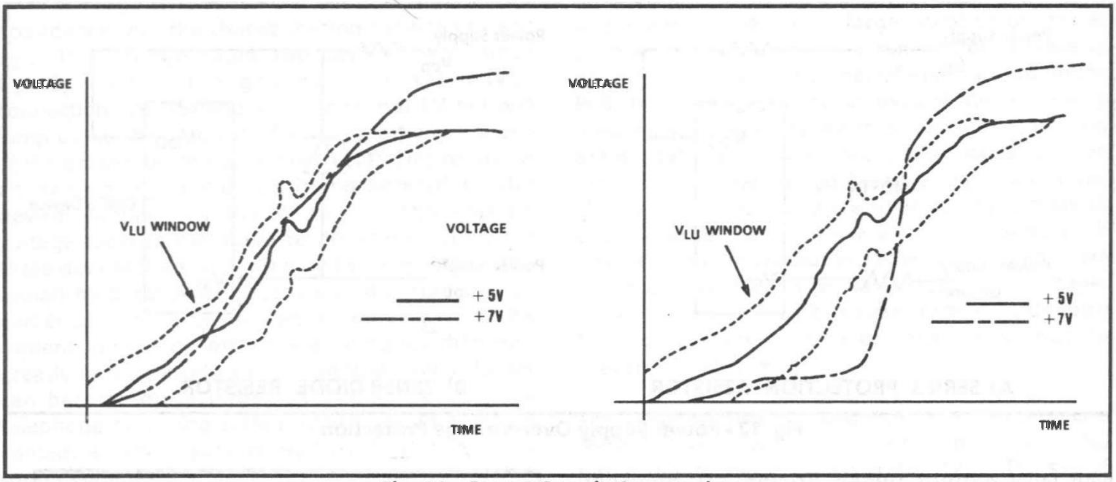


Rys. 14 Sekwencjonowanie zasilania

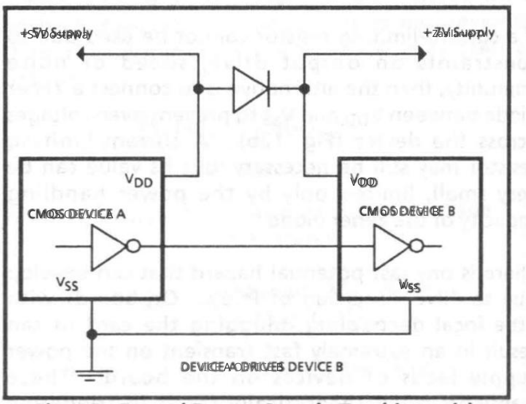
Istnieją tylko przez bardzo krótki okres czasu, aby wywołać blokadę. Tak więc nawet przejściowe przepięcia podczas włączania zasilania mogą stanowić problem.

Aby zapewnić właściwą sekwencję zasilania, należy zwrócić szczególną uwagę na wybór elementów odsprzęgających zarówno na początkowym etapie projektowania, jak i podczas dokonywania zmian w projekcie. Dotyczy to zarówno odsprzęgania głównego zasilania, jak i odsprzęgania lokalnej płyty. Podczas gdy właściwa sekwencja może być widoczna w głównych punktach dystrybucji, lokalne sekwencjonowanie może zostać zmienione przez duże kondensatory na poszczególnych płytach. Płyty o dużym zapotrzebowaniu na prąd stały prawdopodobnie będą miały takie odsprzęganie, dlatego należy je dokładnie rozważyć.

Jednym ze sposobów zapewnienia, że zasilacze śledzą podczas włączania lub wyłączania, jest podłączenie diody z niższego napięcia zasilania do wyższego w przypadku niektórych zasilaczy (rys. 15). Spowoduje to, że zasilacze będą śledziły w granicach jednego spadku napięcia diody, aż osiągną odpowiednie poziomy. W przypadku dwóch równych zasilaczy, dwie diody można podłączyć tyłem do siebie, wymuszając śledzenie zasilaczy, niezależnie od tego, który zasilacz zostanie włączony jako pierwszy.

Urządzenia sterujące innymi na oddzielnych PCB

Gdy układy scalone w systemie sterują innymi urządzeniami na oddzielnych płytkach PCB (np. za pośrednictwem płyty tylnej), wówczas rozważania podane w dwóch poprzednich sekcjach muszą być stosowane globalnie do systemu. Wspomniano o tym już w sekcji dotyczącej podłączania płytek PCB „pod napięciem”. Oznacza to, że gdy płytka PCB jest podłączona do płyty tylnej przy włączonym zasilaniu systemu, istnieje niebezpieczeństwo, że pin wejściowy lub wyjściowy zetknie się z aktywną linią na płycie tylnej przed podłączeniem zasilania



Rys. 15 Śledzenie zasilania Forced Power z zaciskiem Diode

Rozwiązanie tego problemu, jak wspomniano, polega na wcięciu zakończeń krawędzi 1/0 względem zakończeń zasilania na PCB.

Sekwencjonowanie zasilania powinno być traktowane ze szczególną uwagą w systemach z urządzeniami, które sterują poza pokładem. Tutaj obowiązują te same kryteria, które zostały opisane dla systemów z wieloma źródłami zasilania. Należy jednak zachować ostrożność również w systemach z jednym źródłem zasilania. W takim przypadku duże ilości lokalnego odsprzęgania mogą powodować, że napięcia zasilania na niektórych płytach w systemie będą narastać wolniej niż na innych. Devices on płyt, których zasilanie narasta szybko, może wywrzeć przepięcie na urządzeniach na innych płytach. Jeśli to przepięcie jest wystarczająco duże, może zostać wyzwolone zatrzaśnięcie.

Zawsze, gdy jest to możliwe, lokalne odsprzęganie powinno być wyrównane na wszystkich płytach w systemie, aby zminimalizować te efekty. W systemach, w których wszystkie sterowniki poza płytą są urządzeniami trójstanowymi, proste

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solution exists. All outputs should be kept in a high impedance state during power-up and power-down. Thus no current will be available to trigger latch-up even if differential supply voltages develop from board to board. Alternatively, resistors can be connected in series with any inputs or outputs that may be subjected to over-voltages. These resistors are sized to limit current to less than 10mA:

$$R = \frac{(V_{Diff.} - 0.3V)}{10mA}$$

where $V_{Diff.}$ = maximum instantaneous voltage differential between power supplies

The side effects of connecting these resistors are the same as mentioned previously for power supply over voltage protection. There will be reductions in current drive from outputs, increased RC delays and in noise immunity on outputs driving DC loads through these resistors.

Devices Driving Long Address or Data Buses

Long address and data buses can exhibit quite large capacitances. Devices which drive such buses do not have their outputs tied to one another but are subjected to over-voltage conditions. This is especially true for large DC current loads are switched on the same PCB (e.g. a group of LED's during a lamp test). Over-voltages can develop as follows. The change in the power supply current causes a localized voltage drop on the supply pins of the devices near to the device drawing the load current. This is a result of the finite resistance of the power supply tracks and contact resistance of any connectors. At the same time, the bus capacitance tends to hold the voltage on the inputs and outputs connected to the bus at the full supply voltage. If a sufficient voltage differential develops between the bus and the local power supply then the bus capacitance will discharge via the input and output structures. This current can attain a magnitude of tens of milliamps and hence trigger latch-up (Fig. 16).

Various precautions can be taken to reduce the chances of this problem occurring. Reducing the power supply resistance and bus capacitance can be done at the time of initial design. Wide power supply tracks and low contact resistance connectors should be used wherever possible. Bus stubs should be kept as short as possible and have the largest possible spacings between the lines. If this problem still results due to system restraints on PCB layout, then the connection of a decoupling capacitor across the power supply pins of the devices latching-up should help (Fig. 17). The size of the capacitor depends upon the magnitude of the local current and the local resistance of the power supply. Normally a 10nF capacitor will clear such problems and should not interfere with the local power supply sequencing on most PCB's.

There is one other way in which an input/output over voltage can occur on long buses. There exists, on such buses, inherent track capacitance as well as capacitance to ground. When two adjacent tracks are at opposite logic levels (one at 5V, the other at ground), this capacitance charges to the full supply voltage. When the track initially at ground potential suddenly goes high, the signal is coupled through the capacitor to the other track. The voltage on this track increases from its initial value of 5V, impressing over-voltages on any devices connected to this track.

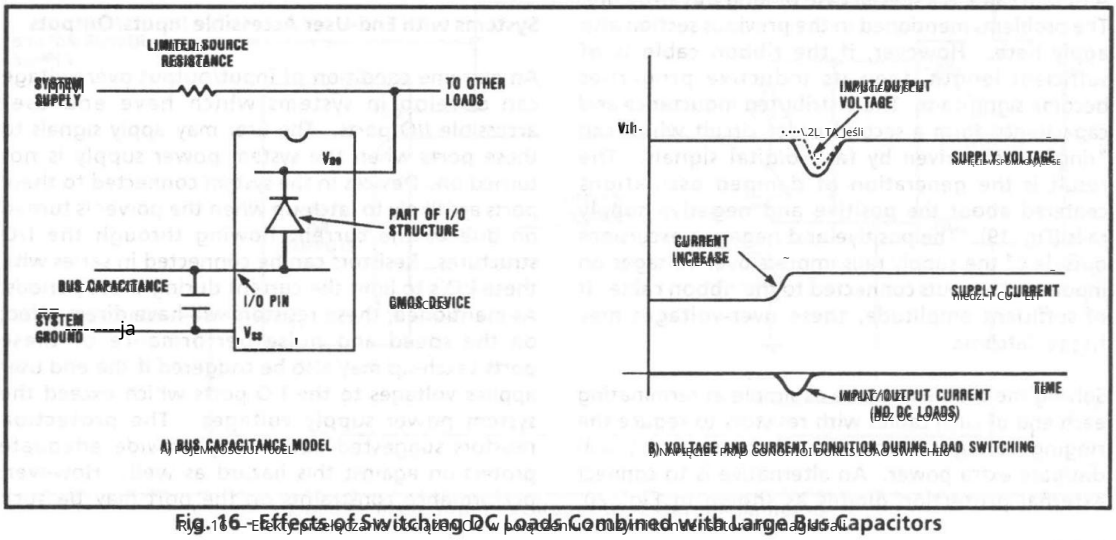

Fig. 16 – Effects of Switching DC Loads Combined with Large Bus Capacitors

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Minimizing interrack capacitance by interleaving signal and ground tracks should be done wherever board space permits. Alternatively, external clamping diodes can be connected on tracks exhibiting these voltage excursions. The diodes may need be Schottky diodes if regular ones do not clamp soon enough toprevent current flow through

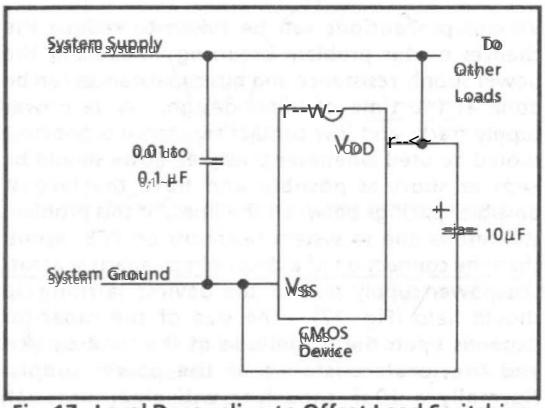


Fig. 17. Local Decoupling to Offset Load Switching Effects

I/O structures. Regular silicon diodes may still be used if they are referenced to voltages inset by 0.7V from the supply rails. The clamping circuit shown in Fig. 18 should be quite effective but can be seen, this circuit will dissipate power. This may or may not be a problem depending on the overall system requirements. The decoupling capacitors help to absorb the high frequency energy. The resistor values shown are selected for a 5V supply and should be scaled for other supply voltages.

Ribbon Cables - A Special Case

A ribbon cable is a special case of long bus structure. The problems mentioned in the previous section also apply here. However, if the ribbon cable is of sufficient length then its inductive properties become significant. The distributed inductance and capacitance form a second order circuit which can "ring" when driven by fast digital signals. The result is the generation of damped oscillations centered about the positive and negative supply rails (Fig. 19). The positive and negative excursions outside of the supply rails impress over-voltages on inputs and outputs connected to the ribbon cable. If of sufficient amplitude, these over-voltages may trigger latch-up.

Solving the problem can be as simple as terminating each end of the cable with a resistor to reduce the ringing voltages. However these resistors will dissipate extra power. An alternative is to connect external protection diodes as shown in Fig. 20.

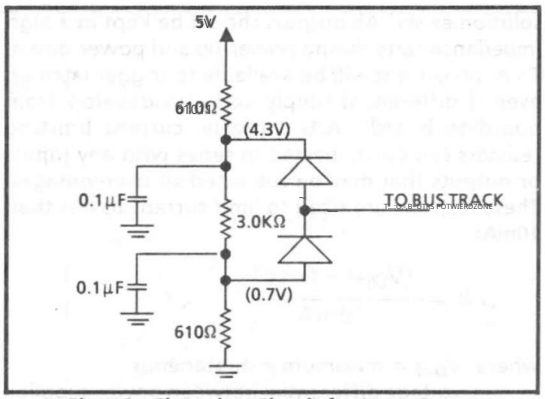


Fig. 18. Clamping Circuit for Long Buses

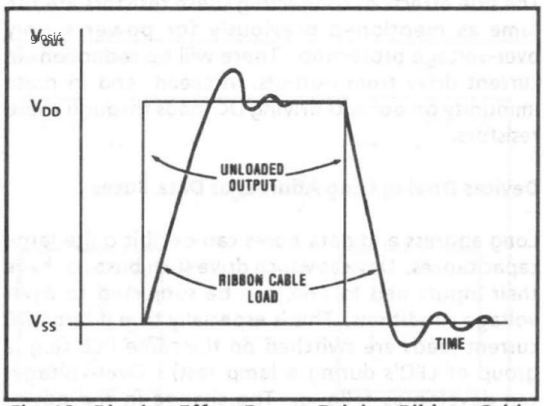
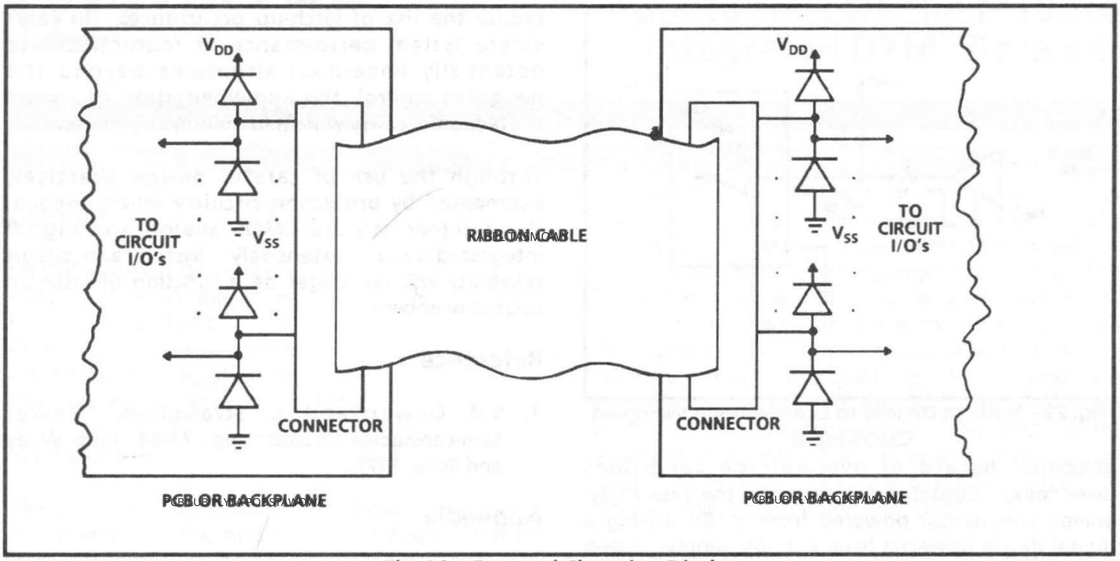


Fig. 19. Ringing Effect Due to Driving Ribbon Cable

These diodes will clamp any generated over-voltages. If the problem persists, it may be necessary to use Schottky diodes to ensure that the external diodes conduct before the input/output structures do.

Systems with End-User Accessible Inputs/Outputs

An extreme condition of input/output over-voltage can develop in systems which have end user accessible I/O ports. The user may apply signals to these ports when the system power supply is not turned on. Devices in the system connected to these ports will latch up when the power is turned on due to the current flowing through the I/O structures. Resistors can be connected in series with these I/O's to limit the current during these periods. As mentioned earlier, these resistors will have a direct effect on the speed and maximum performance of these ports. Latch up may also be triggered if the end user applies voltages to the I/O ports which exceed the system power supply voltages. The protection resistors suggested above may provide adequate protection against this hazard as well. However, performance constraints on the port may be such



Rys. 20 - Zewnętrzne diody zaciskowe

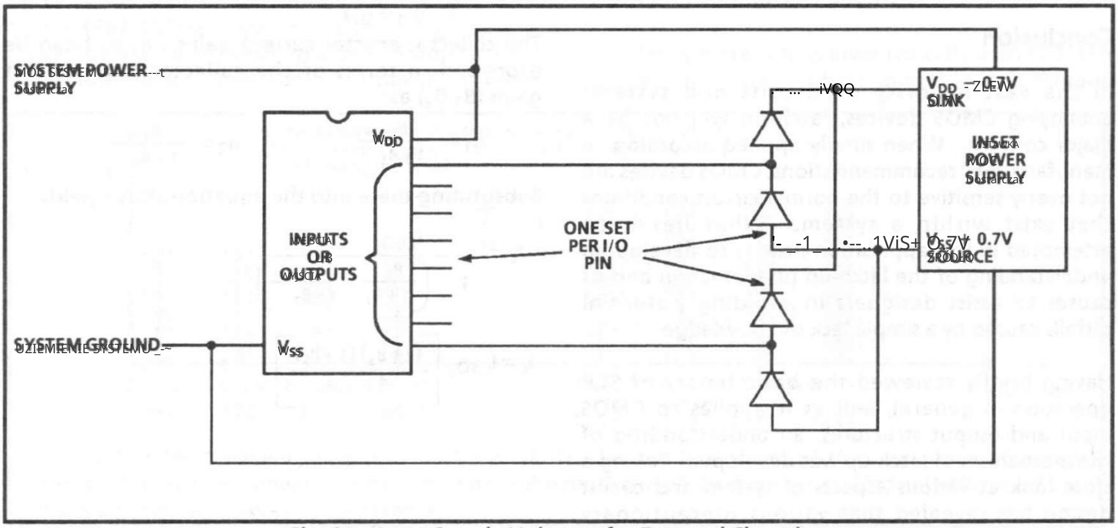
że wybrane rezystory ograniczające prąd są zbyt małe, aby zapewnić ochronę przed poważnymi awariami, np. przypadkowym podłączeniem zasilania sieciowego. Ochronę przed awariami można zapewnić poprzez podłączenie zewnętrznych diod zaciskowych w sposób opisany dla kabli taśmowych. Podobnie, diody Schottky'ego mogą być wymagane.

Jeżeli istnieje prawdopodobieństwo, że w wierszu wejściowym mogą wystąpić tak poważne usterki, może być konieczne zastosowanie zewnętrznych diod zaciskowych do napięcia 0,7 V wprowadzonego przez zasilanie (rys. 21). Diody te będą przewodzić przed strukturami wejścia/wyjścia urządzenia portu

gdy tylko wystąpi przepięcie. Tym samym nie popłynie żaden prąd, który wyzwoliłby zatrzask. Napięcie odniesienia wprowadzone przez 0,7 V, aby umożliwić użycie zwykłych, tanich diod krzemowych. Ponieważ duże prądy płyną przez diody zabezpieczające, obwód zaciskowy wyprowadzony na rys. 18 nie jest wykonalny. Rezystancja wyjściowa w tym przypadku musi być znacznie niższa.

Urządzenia cyfrowe i analogowe w tym samym systemie

W systemach, w których urządzenia cyfrowe i analogowe zasilane są różnymi napięciami zasilania, występuje



Rys. 21 - Wstawienie napięć zasilania dla zewnętrznego zaciskania

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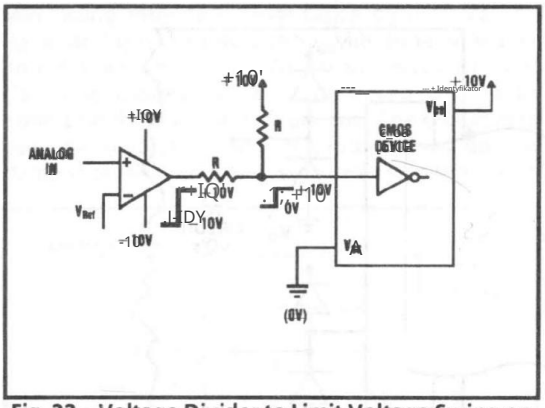

Fig. 22 Voltage Divider to Limit Voltage Swing on CMOS Input

potential hazard of over voltage conditions developing. Consider for example the case of an analog comparator powered from ±10V driving a digital device powered from a +10V supply. When the comparator output goes low it will approach -10V and pull the digital input below V_{SS} (0V). If the comparator can provide enough current, then latch-up may be triggered. Putting a resistor in series with the input will limit the current and prevent latch-up. However it is not a recommended procedure to use the input diodes as clamping circuits. A more advisable solution is to use a resistive divider as shown in Fig. 22. When the comparator output goes low, the divider will have 20V across it. Half of this voltage will be dropped across each resistor so that the digital input sits at 0V. When the comparator output goes high, current flows through the divider so that the digital input sits at V_{DD}. Since the CMOS input has an extremely high input impedance, the value of these resistors can be very large (>100K) to minimize power consumption.

Conclusion

In the vast majority of circuits and systems employing CMOS devices, latch-up will not be a major concern. When simply applied according to manufacturers' recommendations CMOS devices are not overly sensitive to the normal circuit conditions that exist within a system. What has been attempted in this application note is to develop an understanding of the latch-up phenomenon and its causes to assist designers in avoiding potential pitfalls caused by a simple lack of knowledge.

Having briefly reviewed the basic theory of SCR operation in general and as it applies to CMOS input and output structures an understanding of the mechanism of latch-up has been developed. Taking a close look at various aspects of system and circuit design has revealed that various precautionary measures taken at the design stage can greatly reduce the risk of latch-up occurrences. In cases where system performance or features create potentially hazardous situations beyond the designer's control, the implementation of simple protection circuitry will again minimize problems.

Through the use of careful design practices, augmented by protection circuitry when needed, the designer can utilize CMOS analog and digital integrated circuits extensively. System and circuit reliability will no longer be a function of latch-up related problems.

References

1. S.B. Dewan and A. Straughen, "Power Semiconductor Circuits", pp. 77-84, John Wiley and Sons, 1975.

Appendix

The following is a derivation of equation (4) of the main text. Fig. 2 is referenced for this purpose.

The collector and emitter currents of Q_1 and Q_2 are related by:

$$i_{C_1} = \alpha_1 i_{E_1} \qquad i_{C_2} = \alpha_2 i_{E_2}$$

Looking at Fig. 2, it can be seen that the load current and the emitter currents of Q1 and Q2 are all equal. Also the load current is equal to the sum of the collector currents and leakage current from Q_2's collector to its base (I_{CBO_2}). Therefore:

$$\begin{aligned} I_L &= i_{C_1} + i_{C_2} + I_{CBO_2} \\ &= i_{E_1} + i_{E_2} + I_{CBO_2} \\ &= (\alpha_1 + \alpha_2) I_L + I_{CBO_2} \\ &= \frac{I_{CBO_2}}{1 - (\alpha_1 + \alpha_2)} \end{aligned}$$

The collector-emitter current gains (α_1, α_2) can be expressed in terms of the collector-base current gains (B_1, B_2) as:

$$\alpha_1 = \frac{B_1}{1 + B_1} \qquad \alpha_2 = \frac{B_2}{1 + B_2}$$

Substituting these into the equation above yields:

$$I_L = \frac{I_{CBO_2}}{1 - \left(\frac{B_1}{1 + B_1} + \frac{B_2}{1 + B_2} \right)}$$

$$I_L = I_{CBO_2} \left[\frac{(1 + B_1)(1 + B_2)}{1 - B_1 B_2} \right]$$

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Introduction

The purpose of this Application Note is to provide information on the operation and application of Mitel's MT8870 Integrated DTMF Receiver. After a brief discussion of DTMF signalling, the MT8870 will be described in detail and its use illustrated in the application examples which follow.

More than 25 years ago the need for an improved method for transferring dialling information through the telephone network was recognized. The traditional method, Dial pulse signalling was not only slow, suffering severe distortion over long wire loops, but required a DC path through the communications channel. A signalling scheme was developed utilizing tone frequencies and implemented as a relatively reliable alternative to pulse dialling. This scheme is known as DTMF (Dual Tone Multi-Frequency), Touch-Tone™ or tone dialling. As its acronym suggests, a valid DTMF signal is the sum of two tones, one from a low group (697-941 Hz) and one from a high group (1209-1633Hz) with each group containing four individual tones. The tone frequencies were carefully chosen such that they are not harmonically related and that intermodulation products cannot result in minimal signalling impairment (Fig. 1a). This scheme allows for 16 unique combinations. Ten of these codes represent the numerals zero through nine, the remaining six (*, #, A, B, C, D) being reserved for special signalling. Most telephone keypads contain ten numeric push buttons plus the asterisk (*) and octothorpe (#). The buttons are arranged in a matrix, each generating a unique tone from its respective row and its high group tone from its respective column (Fig. 1b).

The DTMF coding scheme ensures that each signal contains one and only one component from each of the high and low groups. This significantly simplifies decoding, because the two components of a DTMF signal may be separated with bandpass filters and its resultant single frequency components each of which may be handled individually. As a result DTMF coding has proven to provide a flexible signalling scheme of excellent reliability, hence motivating innovative and competitive decoder design.

Development

Early DTMF decoders (receivers) utilized banks of bandpass filters, dynamic tuning or some what cumbersome and expensive implementations. This generally restricted their application to central offices (telephone exchanges).

The first generation receivers typically used LC filters, active filters and/or phase locked loop techniques

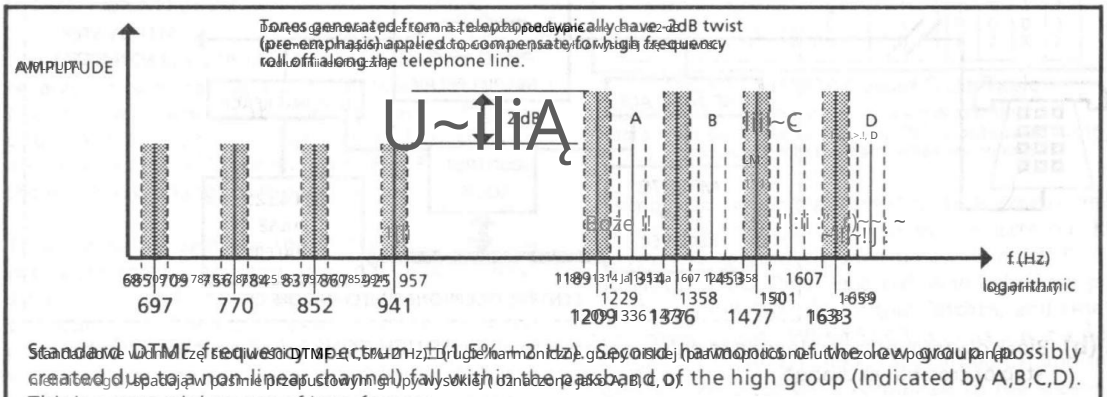

Fig. 1a The Dual Tone Multi-frequency (DTMF) Spectrum

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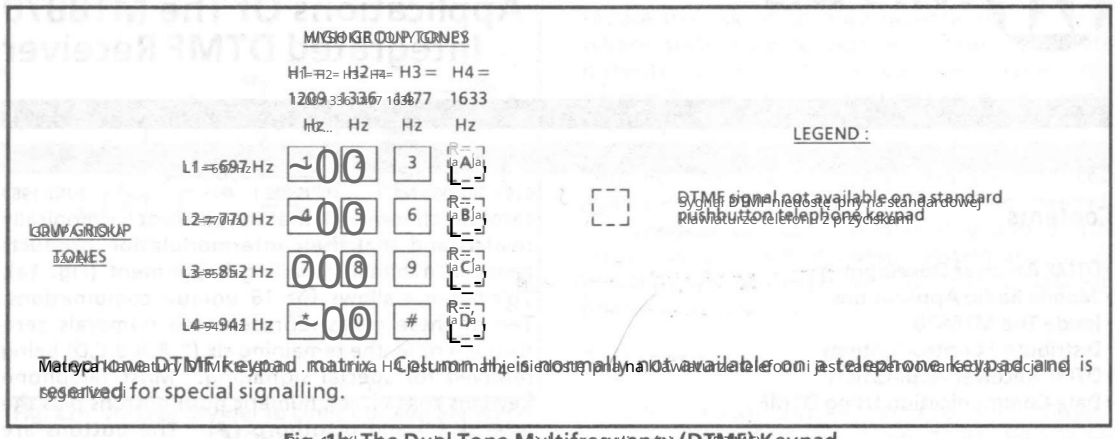
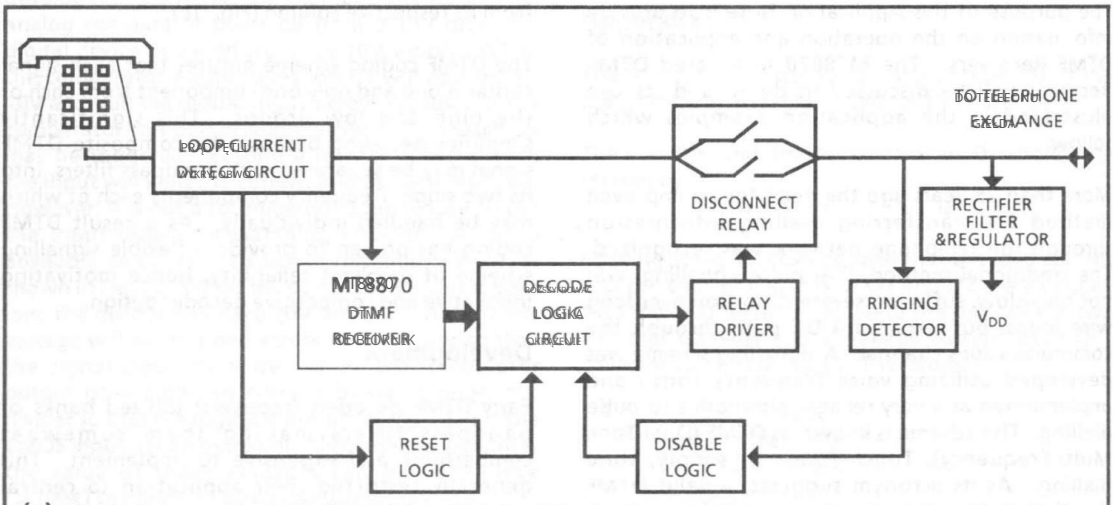
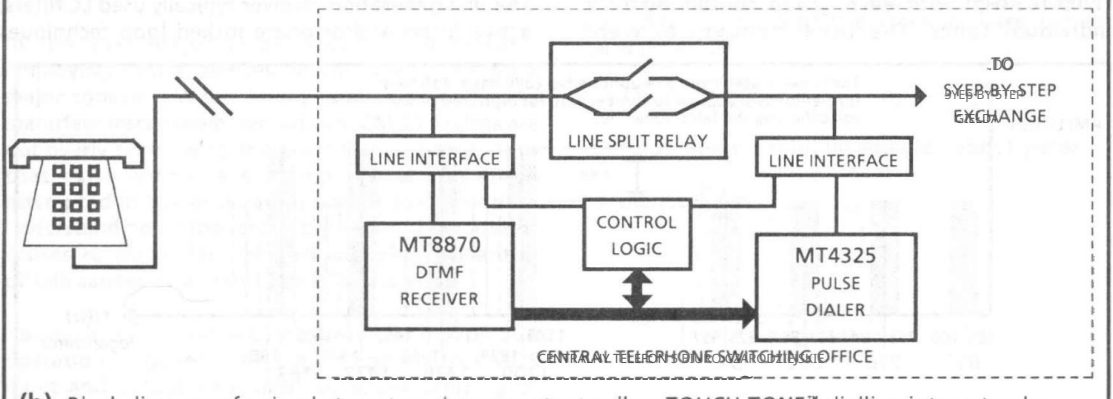


Telephone DTMF Keypad Matrix. Column H4 is normally not available on a telephone keypad and is reserved for special signalling.

Fig. 1b The Dual Tone Multifrequency (DTMF) Keypad



(a) Block diagram of a toll call restrictor. This could be implemented on a small pc board and installed in a telephone wykonywania połączeń międzymiastowych



(b) Block diagram of a simple tone to pulse converter to allow TOUCH-TONE™ dialling into a step-by-step exchange.

Fig. 2 Typical DTMF Receiver Applications

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to receive and decode DTMF tones. Initial functions were commonly phone number decoders and toll call restrictors. A DTMF receiver is also frequently used as a building block in a tone-to-pulse converter which allows Touch-Tone™ dialling access to mechanical step-by-step and crossbar exchanges (Fig. 2).

The introduction of MOS/LSI digital techniques brought about the second generation of tone receiver development. These devices were used to digitally decode the two discrete tones that result from decomposition of the composite signal. Two analog bandpass filters were used to perform the decomposition.

Totally self-contained receivers implemented in thick film hybrid technology depicted the start of third generation devices. Typically they also used analog active filters to bandsplit the composite signal and MOS digital devices to decode the tones.

The development of silicon implemented switched capacitor sampled filters marked the birth of the fourth and current generation of DTMF receiver technology. Initially single chip bandpass filters were combined with currently available decoders enabling a two chip receiver design. A further advance in integration has merged both functions onto a single chip allowing DTMF receivers to be realized in minimal space at a low cost.

The second and third generation technologies saw a tendency to shift complexity away from the analog circuitry towards the digital LSI circuitry in order to reduce the complexity of analog filters and their inherent problems. Now that the filters themselves can be implemented in silicon, the distribution of complexity becomes more a function of performance and silicon real estate.

Inside The MT8870

The MT8870 is a state of the art single chip DTMF receiver incorporating switched capacitor filter technology and an advanced digital counting/averaging algorithm for period measurement. The block diagram (Fig. 3) illustrates the internal workings of this device.

To aid design flexibility, the DTMF input signal is first buffered by an input op-amp which allows adjustment of gain and choice of input configuration. The input stage is followed by a low pass continuous RC active filter which performs an antialiasing function. Dial tone at 350 and 440Hz is then rejected by a third order switched capacitor notch filter. The signal, still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then smoothed by an output filter and squared by a hard limiting comparator.

The two resulting rectangular waves are applied to digital circuitry where a counting algorithm measures and averages their periods. An accurate reference clock is derived from an inexpensive external 3.58MHz color burst crystal.

The timing diagram (Fig. 4) illustrates the sequence of events which follow digital detection of a DTMF tone pair. Upon recognition of a valid frequency from each tone group the Early Steering (ESt) output is raised. The time required to detect the presence of two valid tones, t_{DP}, is a function of the decode algorithm, the tone frequency and the previous state of the decode logic. ESt indicates that two tones of proper frequency have been detected and initiates an RC timing circuit. If both tones are present for the minimum guard time, t_{GTP}, which is determined by the external RC network, the DTMF signal is decoded and the resulting data (Table 1) is latched in the output register. The Delayed Steering (StD) output is raised and indicates that new data is available. The time required to receive a valid DTMF signal, t_{REC}, is equal to the sum of t_{DP} and t_{GTP}.

f_{LOW}	f_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

Table 1. MT8870 Output Truth Table

0=LOGIC LOW 1=LOGIC HIGH Z=HIGH IMPEDANCE

Output truth table. Note that key "0" is output as 1010_2 (i.e. 10_{10}) corresponding to standard telephone coding.

A simplified circuit diagram (Fig. 5) illustrates how the chip's steering circuit drives the external RC network to generate guard times. Pin 17, St/GT (Steering/Guard Time) is a bidirectional signal pin which controls StD, the output latches, and resets the timing circuit. When St/GT is in its input mode (St function) both Q_P and Q_N are turned off and the voltage level at St/GT is compared to the steering threshold voltage V_{TSt}. A transition from below to above V_{TSt} will switch the comparator's output

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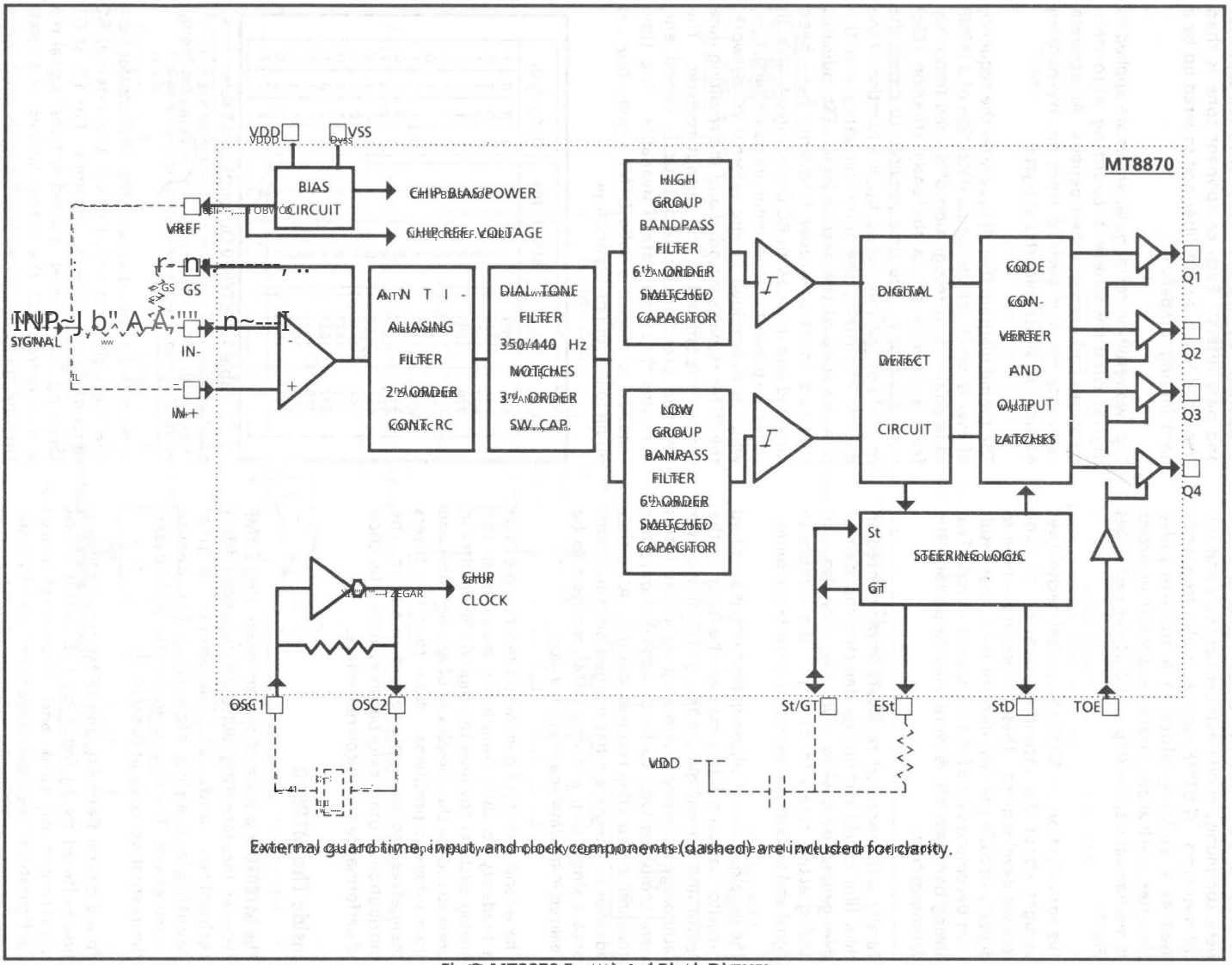

External guard time, input and clock components (dashed) are included for clarity.

Fig. 3 - MT8870 Functional Block Diagram

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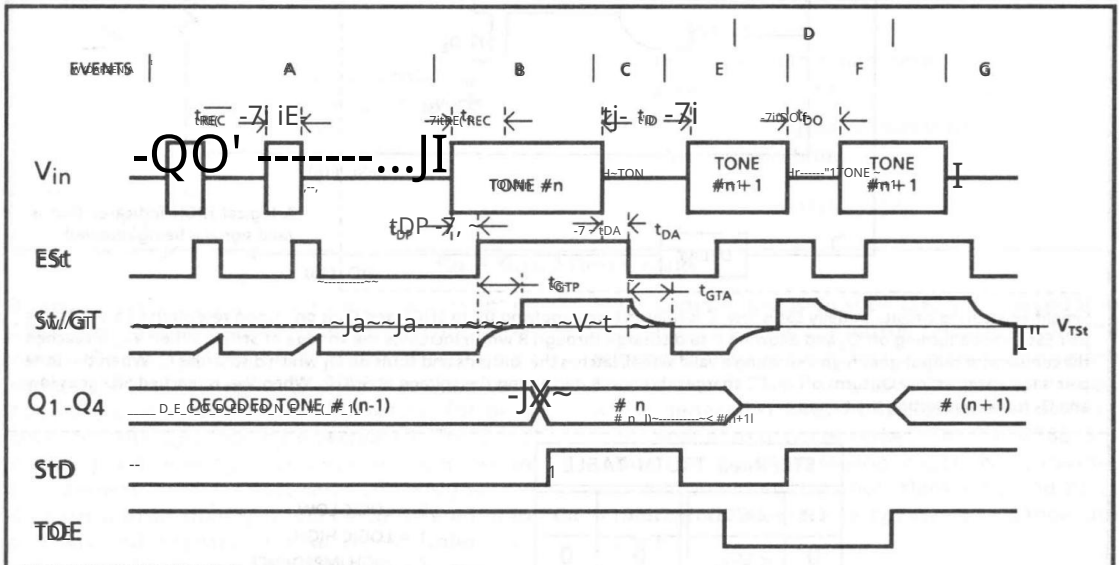
from low to high strobing new data into the output latches and raising the StD output. As long as an input level above V_{TST} is maintained StD will remain high indicating the presence of a valid DTMF signal.

Initially, when no valid tone pairs are present, capacitor C is fully charged applying a low voltage to St/GT. This causes a low at the comparator's output and ensures ESt is also low. Q_2 turns on ensuring that C is completely charged. In this condition St/GT is in its output mode (GT function). When a valid tone pair is received ESt is raised turning off Q_2 which puts St/GT in its high impedance mode and allows C to discharge through R. If this condition persists for the tone-present guard time, t_{GTP}, the voltage at St/GT rises above V_{TST} raising StD which indicates reception of a valid DTMF signal. If the tone pair drops out before the duration of t_{GTP}, ESt is lowered turning on Q_2 which charges C resetting the tone-present guard time.

Once a DTMF signal is recognized as valid both ESt and the comparator output are high. This turns on Q_2 which discharges C and initializes the tone-absent guard time, t_{GTA}. After the DTMF signal is removed, ESt is lowered, Q_2 turns off placing St/GT in its input mode and C begins to charge through R.



EXPLANATION OF EVENTS

A) TONE BURST IS PRESENTED TONE DURATION INVALID, OUTPUTS NOT UPDATED
B) TONE #n DETECTED TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE
E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)
F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED
G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT - INDICATES DETECTION OF CORRECT TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT - DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT - INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME. THIS CONSTITUTES A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT) - A LOW LEVEL SHIFTS Q_1-Q_4 TO THE HIGH IMPEDANCE STATE.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM VALID DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT

Fig. 4 MT8870 Timing Diagram

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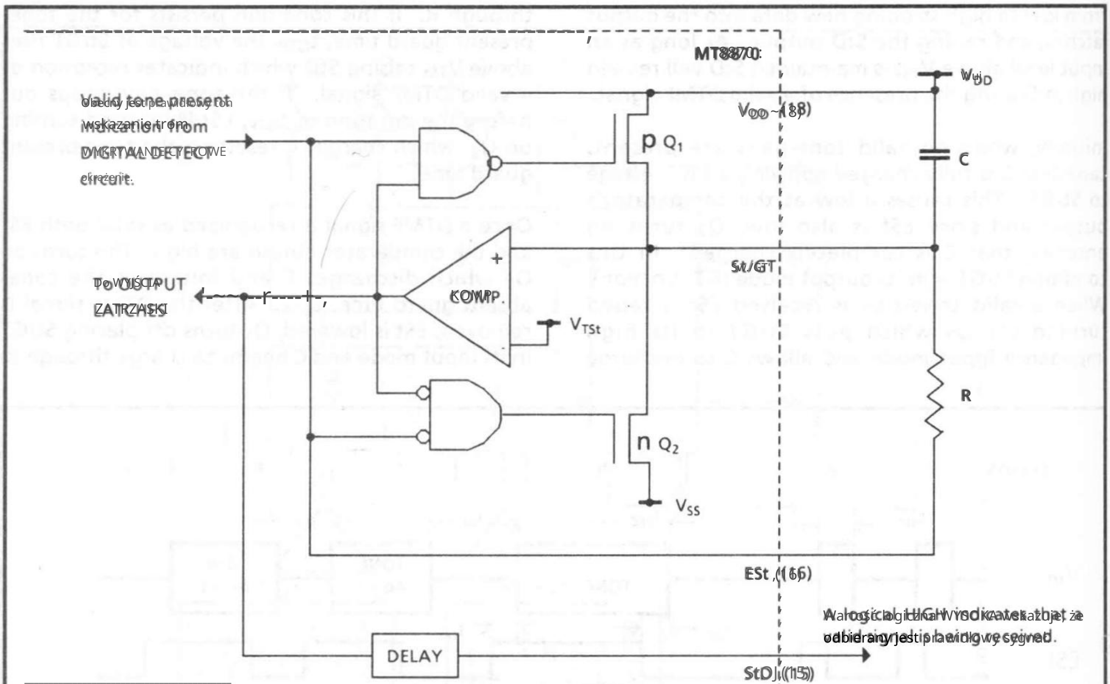

Uproszczony obwód sterowania. Początkowo ESt jest niski, C jest w pełni naładowany, stosując 0 V do St/GT, a Q_2 jest on. Po odebraniu prawidłowego tonu pary ESt jest podniesiony, wyłączając Q_2 i pozwalając C na rozładowanie się przez R, co zwiększa napięcie w St/GT. Gdy V_{TSt} zostanie osiągnięte, wyjście komparatora przechodzi w stan wysoki, wskazując prawidłowy sygnał, blokuje wyjście w dekoderze, i Q_1 rozładowuje C. Gdy para tonów zostanie utracona, ESt zmienia się na niski, Q_1 wyłącza się i C ładuje przez R. Gdy zostanie osiągnięte V_{TSt}, StD zmienia się na niski, a Q_2 resetuje obwód czasowy.

TABELA PRAWDY STEROWANIA

ESt	St(/GT)	(St)/GT	StD
0	$< V_{TSt}$	0	0
0	$> V_{TSt}$	Z	1
1	$< V_{TSt}$	Z	0
1	$> V_{TSt}$	1	1

0 = LOGICZNY LOW
1 = LOGICZNY HIGH
Z = WYSOKA IMPEDANCJA
V_{TSt} = Napięcie progowe (zwykle 1/2 V_{DD})

Tabela prawdy obwodu sterującego. Należy zauważyć, że (St/GT) działa zarówno jako wejście, jak i wyjście, w zależności od względnych stanów ESt i komparatora wyjście.

Rys. 5 Działanie układu sterowania i obwodu czasu ochrony MT8870

Jeżeli ta sama prawidłowa para tonów nie pojawi się ponownie przed t_{GTA}, a następnie napięcie w St/GT spada poniżej V_{TSt}, który resetuje obwód czasowy za pomocą Q_2 i przygotowuje urządzenie do odbioru kolejnego sygnału. Jeśli ta sama ważna para tonów pojawi się ponownie przed t_{GTA}, ESt jest podniesione, włączając Q_1 i rozładowując C, co resetuje t_{GTA}. W tym przypadku StD pozostaje wysokie, a zanik sygnału tonu jest ignorowany jako hałas.

Aby zapewnić środowisko o dobrej niezawodności w typowej telefonii, należy zaprojektować odbiornik DTMF tak, aby rozpoznawał prawidłową parę tonów o czasie trwania większym niż 40 ms i aby zaakceptować jako kolejne cyfry pary tonów, które są oddalone od siebie o więcej niż 40 ms. Jednak w innych środowiskach, takich jak dwukierunkowe radio, optymalny czas trwania tonu i czasy wewnątrzcyfrowe mogą różnić się ze względu na hałas.

Dodając dodatkowy rezystor i diodę sterującą (rys. 6b, 6c) t_{GTP} i t_{GTA} można ustawić na różne wartości. Regulacja czasu ochrony umożliwia dostosowanie odporności na hałas i wydajności odmowy w celu spełnienia określonych potrzeb systemu.

Współczynnik rozmowy jest miarą błędów, które występują, gdy odbiornik fałszywie wykrywa parę tonów z powodu mowy lub szumu tła symulującego sygnał DTMF. Zwiększenie t_{GTP} poprawia wydajność rozmów od

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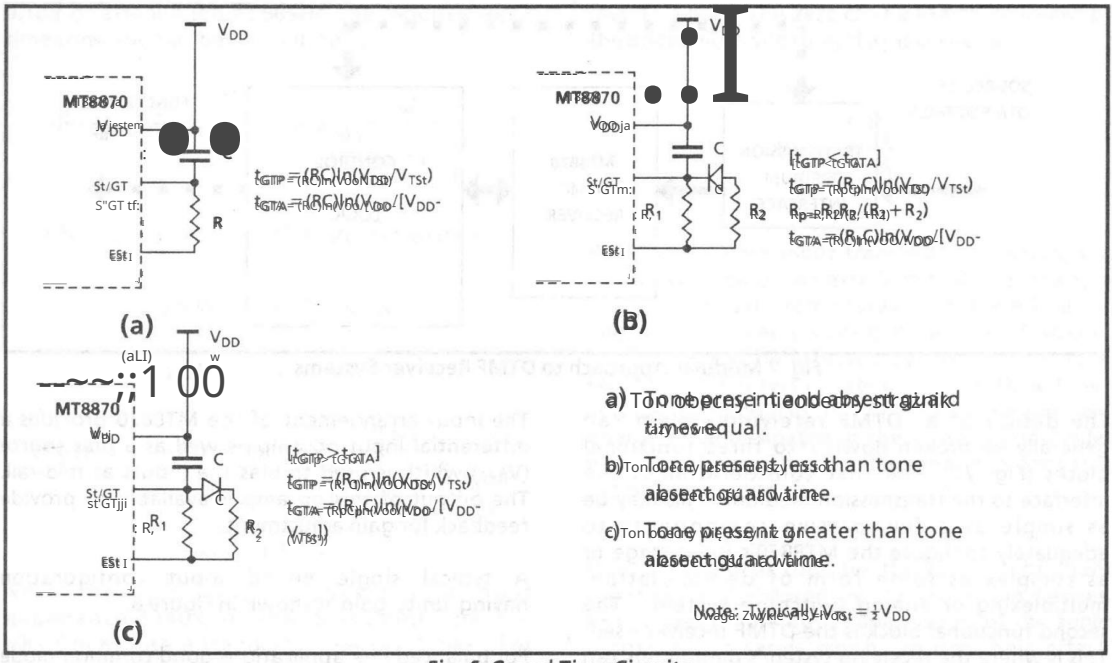

a) Tone present and absent guard times equal.

b) Tone present less than tone absent guard time.

c) Tone present greater than tone absent guard time.

Note: Typically $V_{TSt} = \frac{1}{2}V_{DD}$

Fig. 6 Guard Time Circuits

in reduces the probability that speech will maintain DTMF simulation long enough to be considered valid. The trade-off here is decreased noise immunity because dropout (longer than t_{GTP}) due to noise pulses will restart t_{GTP}. Therefore, for noisy environments, t_{GTP} should be decreased. The signal absent guard time, t_{GTA}, determines the minimum time allowed between successive DTMF signals. A dropout shorter than t_{GTA} will be considered noise and will not register as a successive valid tone detection. This guards against multiple reception of a single character. Therefore, lengthening t_{GTA} will increase noise immunity and tolerance to the presence of an unwanted third tone at the expense of decreasing the maximum signalling rate.

The intricacies of the digital detection algorithm have a significant impact on the overall receiver performance. It is here that the initial decision is made to accept the signal as valid or reject it as speech or noise.

Trade-offs must be made between eliminating talk-off errors and eliminating the effects of unwanted third tone signals and noise. These are mutually conflicting events. On one hand valid DTMF signals presence in noise must be recognized which requires relaxation of the detection criteria. On the other hand, relaxing the detection criteria increases the probability of talk-off errors.

Many considerations must be taken into account in evaluating criteria for noise rejection. In the telephony environment two sources of noise are predominant. These are third tone interference, which generally comes from dial tone harmonics, and band-limited white noise. In the MT8870 a complex digital averaging algorithm provides excellent immunity to voice, third tone and noise signals which prevail in a typical voice bandwidth channel.

The algorithm used in the MT8870 combines the best features from two previous generations of Mitel digital decoders with improvements resulting from years of practical use within the telephone environment. The algorithm has evolved through a combination of statistical calculations and empirical "tweaks" to result in the realization of an extremely reliable decoder.

Applications

The proven reliability of DTMF signalling has created a vast spectrum of possible applications. Until recently, many of these applications were not considered due to cost or size considerations. Now that a complete DTMF receiver can be designed with merely a single chip and a few external passive components one can take full advantage of a highly developed signalling scheme at a small cost effective design solution.

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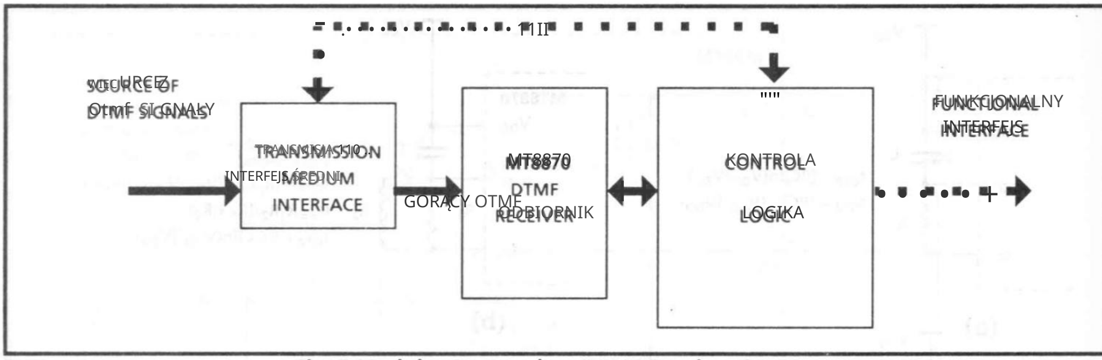


Rys. 7 Podejście modułowe do systemów odbiorników DTMF

Projekt systemu odbioru DTMF można ogólnie podzielić na trzy bloki funkcjonalne (rys. 7). Pierwszym zagadnieniem jest interfejs do medium transmisyjnego. Może to być tak proste, jak kilka pasywnych komponentów, aby odpowiednio skonfigurować stopień wejściowy MT8870 lub tak złożone, jak jakaś forma demodulacji, multipleksowania lub analogowego systemu przełączającego. Drugim blokiem funkcjonalnym jest sam odbiornik DTMF.

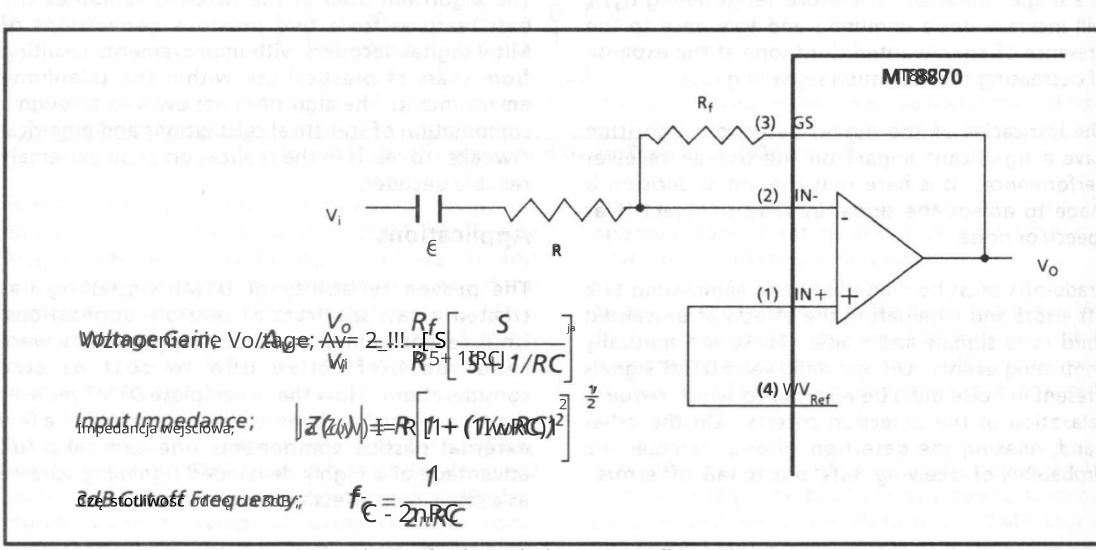
Tutaj parametry systemu odbiorczego mogą być optymalizowane pod kątem konkretnych warunków sygnału dostarczanego z interfejsu „front end". Trzecią i być może najbardziej zmienną funkcją jest logika sterowania wyjściami. Może być ona tak prosta, jak dekoder 4-16-liniowy, kontrolujący określoną funkcję dla każdego kodu DTMF, lub tak złożona, jak w pełni rozwinięty komputer obsługujący protokoły systemu adaptacyjnie zmieniający parametry odbiornika w celu dostosowania do zmieniających się warunków sygnału. Poniżej opisano kilka obecnie stosowanych i koncepcyjnie zaprojektowanych zastosowań, ale najpierw zajmiemy się projektem typowego stopnia wejściowego.

Układ wejściowy MT8870 zapewnia różnicowy wzmacniacz operacyjny wejściowy, a także źródło polaryzacji (V_{REF}), które służy do polaryzacji wejść na szynie środkowej. Wyjście tego wzmacniacza operacyjnego może zapewnić sprzężenie zwrotne w celu regulacji wzmocnienia.

Typowa konfiguracja wejścia single-ended o wzmocnieniu jednostkowym jest pokazana na rysunku 8.

W przypadku zastosowań zbalansowanych linii dobre tłumienie sygnału wspólnego jest oferowane przez konfigurację różnicową (rys. 9). W obu przypadkach wejścia są spolaryzowane do 1/2 V_{DD} przez V_{Ref}. Rozważmy stopień wejściowy, który będzie interfejsował się z linią zbalansowaną 600Ω. Aby odrzucić sygnały szumu wspólnego, rozwiązanie zapewnia zbalansowane wejście wzmacniacza różnicowego.

Przy wejściu skonfigurowanym na wzmocnienie jednostkowe układ MT8870 będzie akceptował maksymalne poziomy sygnału 1 dBm (do 600Ω). Najniższa częstotliwość DTMF, która musi zostać wykryta, wynosi około 685Hz. Pozwalając



Rys. 8 Konfiguracja wejścia single-ended

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0.1dB of attenuation at 685Hz, the required input time constant may be derived from;

0,1 dB tłumienia przy 685 Hz, wymagana stała czasowa wejściowa może być wyprowadzona z;

$$M(\omega)_{dB} = 20\log_{10}\frac{R_f}{R} + 20\log_{10}\frac{\omega\tau}{\left\{(\omega\tau)^2+1\right\}^{\frac{1}{2}}}$$

where $M(\omega)_{dB}$ is the amplifier gain in decibels

gdzie $M(\omega)_{dB}$ to wzmocnienie wzmacniacza w decybelach

ω is the radian frequency

ω jest częstością kołową

τ is the input time constant

τ jest stałą czasową wejściową

$$\text{Therefore} \quad -0.1 = 20\log_{10}\frac{(2\pi)685\tau}{\left\{\left[(2\pi)685\tau\right]^2+1\right\}^{\frac{1}{2}}}$$

Dlatego $-0{,}1 = 20\log_{10}\frac{(2\pi)685\tau}{\left\{\left[(2\pi)685\tau\right]^2+1\right\}^{\frac{1}{2}}}$

$$\text{or } \tau = 1.52mS$$

lub $\tau = 1{,}52mS$

Now choosing R = 220K gives a high input impedance (440K) in the passband) and C = (R = 69nF (use a standard value of 10 nF). For unity gain in the passband we choose $R_a = R_b = R$ and R_b are biasing resistors. The choice of R_b is not critical and could be set at say 68K. Bias resistor R_b adds a zero to the non-inverting path through the differential amplifier but has no affect on the

Teraz, wybierając R = 220K, uzyskujemy wysoką impedancję wejściową (440K w paśmie przenoszenia) i C = (R = 69nF (użyj standardowej wartości 10 nF). Aby uzyskać wzmocnienie jedności w paśmie przenoszenia, wybieramy $R_a = R_b = R$ i R_b rezystory polaryzujące. Wybór R_b nie jest krytyczny i można go ustawić na przykład na ... 68K. Rezystor polaryzujący R_b dodaje zero do nieodwracającej ścieżki przez wzmacniacz różnicowy, ale nie ma wpływu na

inverting path. This zero can be exactly cancelled by the added pole due to R_b if R_b is chosen as;

dodawanego bieguna z powodu R_b if R_b jest wybrane jako;

$$R_b = \frac{R_a R_f}{R_a + R_f}$$

With appropriate input transient protection, this circuit will provide an excellent bridging interface across a properly terminated telephone line for end-to-end or key system applications. Transient protection may be achieved by splitting the input resistors and inserting zener diodes to achieve voltage clamping (Fig. 10). This allows the transient energy to be dissipated in the resistors and diodes and limits the maximum voltage that may appear at the op-amp inputs.

Przy odpowiednim zabezpieczeniu przejściowym wejścia obwód ten zapewni doskonały interfejs mostkowy przez prawidłowo zakończoną linię telefoniczną do zastosowań typu end-to-end lub key system. Ochronę przejściową można uzyskać przez rozdzielenie rezystorów wejściowych i wstawienie diod zenera w celu uzyskania zacisku napięciowego (rys. 10). Pozwala to na rozproszenie energii przejściowej w rezystorach i diodach oraz ogranicza maksymalne napięcie, które może pojawić się na wejściach wzmacniacza operacyjnego.

It is important to consider the amount of shunt capacitance introduced by the protection devices. In this case the parasitic capacitances of the zener diodes are connected in series with R_a which reduces their effect. Relatively large shunt capacitances will attenuate the high group frequencies causing the input signal to "twist" which degrades receiver performance.

Ważne jest, aby wziąć pod uwagę wielkość pojemności bocznikowej wprowadzonej przez urządzenia zabezpieczające. W tym przypadku pojemności pasożytnicze diod Zenera są połączone szeregowo z rezystorami R_a, co zmniejsza ich wpływ. Stosunkowo duże pojemności bocznikowe tłumią wysokie częstotliwości grupy, powodując „skręcanie" sygnału wejściowego, co pogarsza wydajność odbiornika.

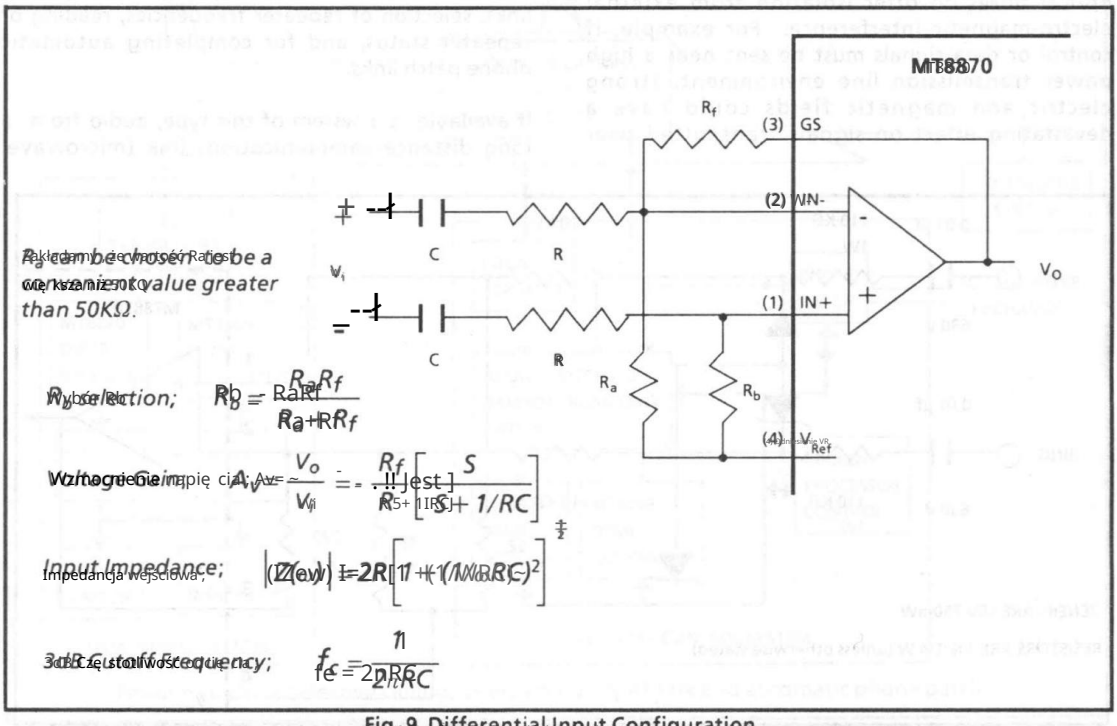

Fig.9 Differential Input Configuration

Rys.9 Konfiguracja wejścia różnicowego

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"Twist" is known as the difference in amplitude between the low and high group tones. It is specified in dB as:

$$TWIST = 20 log \frac{V_L}{V_H}$$

where V_L is the amplitude of the low frequency tone

and V_H is the amplitude of the high frequency tone.

Twist is usually caused by the frequency response characteristic of the communication channel. Along a telephone line higher frequencies tend to roll off faster than the lower ones so the line response is usually compensated for by applying pre-emphasis (negative twist) to the originating DTMF signal. In extreme cases the receiver may require compensation. This could be realized with a filter arrangement utilizing the input op amp.

Any communication path that passes the human voice spectrum is adequate for DTMF signalling. Therefore a variety of "off-the-shelf" interfaces may be applicable in a given control system. More commonly used media are copper wire and RF channels. An optical fibre could carry a light beam modulated by DTMF. Although this would incur a large overhead in terms of bandwidth utilization, optical fibres do offer the possibility of total electro-magnetic interference immunity. For example, if control or data signals must be sent near a high power transmission line environment, strong electric and magnetic fields could have a devastating effect on signals transmitted over wires. DTMF over fibre optics could easily be employed as a highly reliable communications link in a harsh interference infested environment.

In modern digital switching equipment the MT8870 can easily be interfaced to digital PCM line using a codec as an input interface (Fig. 11). Actually all that is required for this interface is a PCM decoder with filter, which is normally associated with PCM decoders. It is not required since the DTMF bandpass filter has an upper cutoff frequency low enough to meet the required roll-off of the PCM filter.

DTMF in Mobile Radio Applications

DTMF signalling plays an important role in distributed communications systems such as multi-user mobile radio (Fig. 12). It is a "natural" in the two-way radio environment since it slips neatly into the centre of the voice spectrum, has excellent noise immunity, and highly integrated methods of implementation are currently available. It is also directly compatible with telephone signalling, simplifying automatic phone patch systems.

Several emergency medical services networks currently use DTMF signals to control radio repeaters. Functions are typically mobile identification, selection of appropriate repeater links, selection of repeater frequencies, reading of repeater status, and for completing automatic phone patch links.

If available in a system of this type, audio from a long distance communications link (microwave,

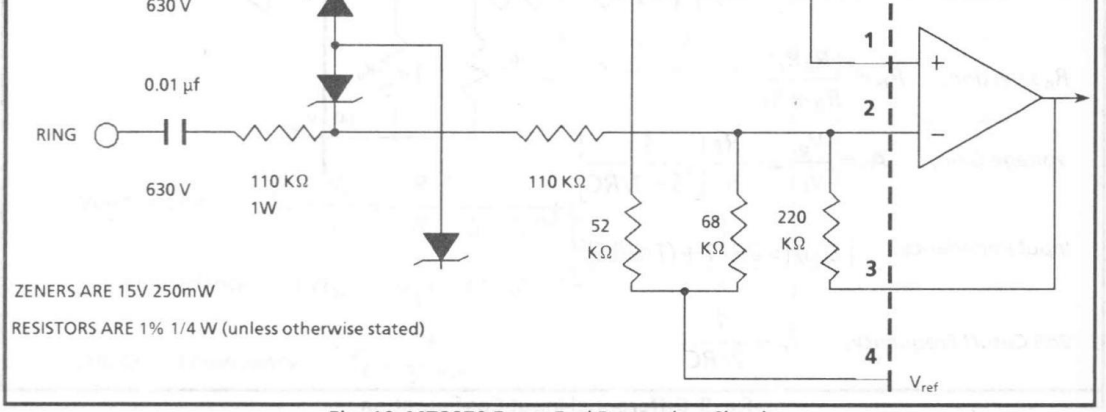

Fig. 10 MT8870 Front End Protection Circuit

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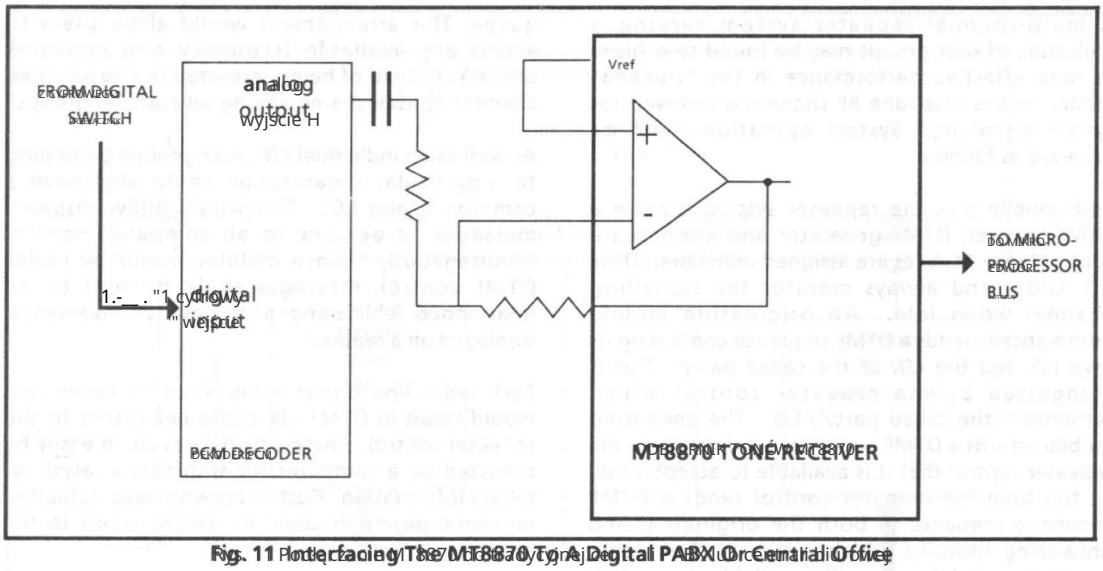
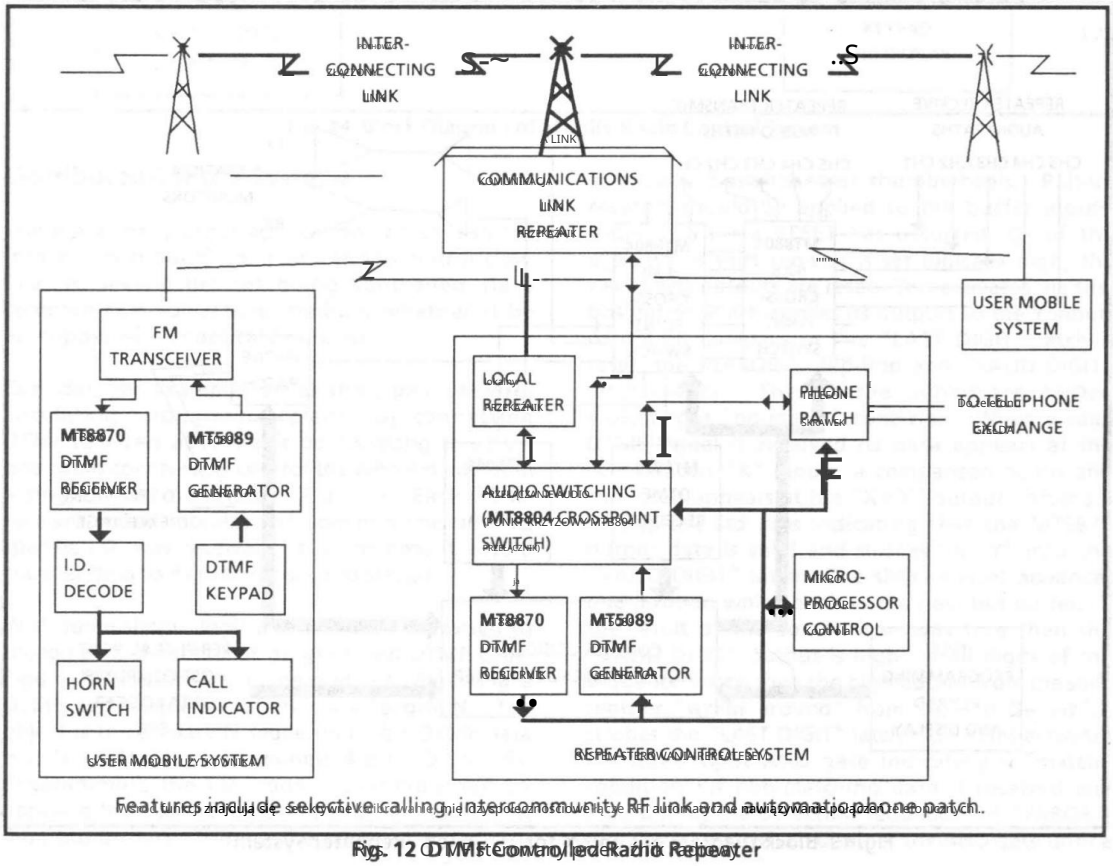


Fig. 11 Interfacing the MT8870 to a Digital PABX or Central Office

satellite, etc.) can be achieved, where commands from the DTMF keypad go to the local repeater. This would offer the mobile user a variety of features including selective calling, inter-community RF link and automatic phone patch.

Interfejsowanie układu MT8870 do cyfrowej centrali abonenckiej lub centrali biurowej

sieci łączności radiowej (satelitarnej, itp.), w której polecenia z klawiatury DTMF są przesyłane do lokalnego przekaźnika. To zapewniłoby użytkownikowi ruchomemu szereg możliwości, takich jak selektywne wywoływanie, międzyosiedlowe łącze radiowe RF oraz automatyczne połączenie z operatorem.



Features include selective calling, inter-community RF link and automatic phone patch.

Możliwości znajdują się: selektywne wywoływanie, międzyosiedlowe łącze RF i automatyczne nawiązywanie połączeń telefonicznych.

Fig. 12 DTMF Controlled Radio Repeater

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A multi-channel repeater system serving a multitude of user groups may be forced to take its most effective use of the available RF channels for system signalling. System operation could be achieved as follows.

Each mobile plus the repeater system contain a DTMF receiver, DTMF generator and appropriate control logic. Mobiles are assigned individual DTMF I.D. codes and always monitor the signalling channel when idle. An originating mobile automatically sends a DTMF sequence containing its own I.D. and the I.D. of the called party. This identifies to the repeater control that it is available to accept a call. At this time the repeater control sends a DTMF command sequence to both the originating and answering mobiles which instructs their logic circuits to switch to specific available channels and where they will be monitored by the repeater control. It then sends DTMF sequences containing both mobiles' I.D.'s to a "channel-request" queue. This arrangement would allow users to access any available frequency and converse privately instead of being restricted to one assigned channel which is shared among several user groups.

As well as an individual I.D. each mobile belonging to a particular organization would also have a common group I.D. This would allow dispatch messages to be sent to all company mobiles simultaneously. Since mobiles would be under DTMF control, messages could be sent to an unattended vehicle and, at the user's convenience, displayed on a readout.

Each radio link established or attempted would result in DTMF I.D. codes being sent to the repeater control. These occurrences could easily be collected by a computer for statistical analysis or billing information. Customers who have defaulted on rental payments could be denied access to the system.

Simplified block diagrams of the control systems for both the repeater and mobiles are shown in Figures 13 and 14 respectively.

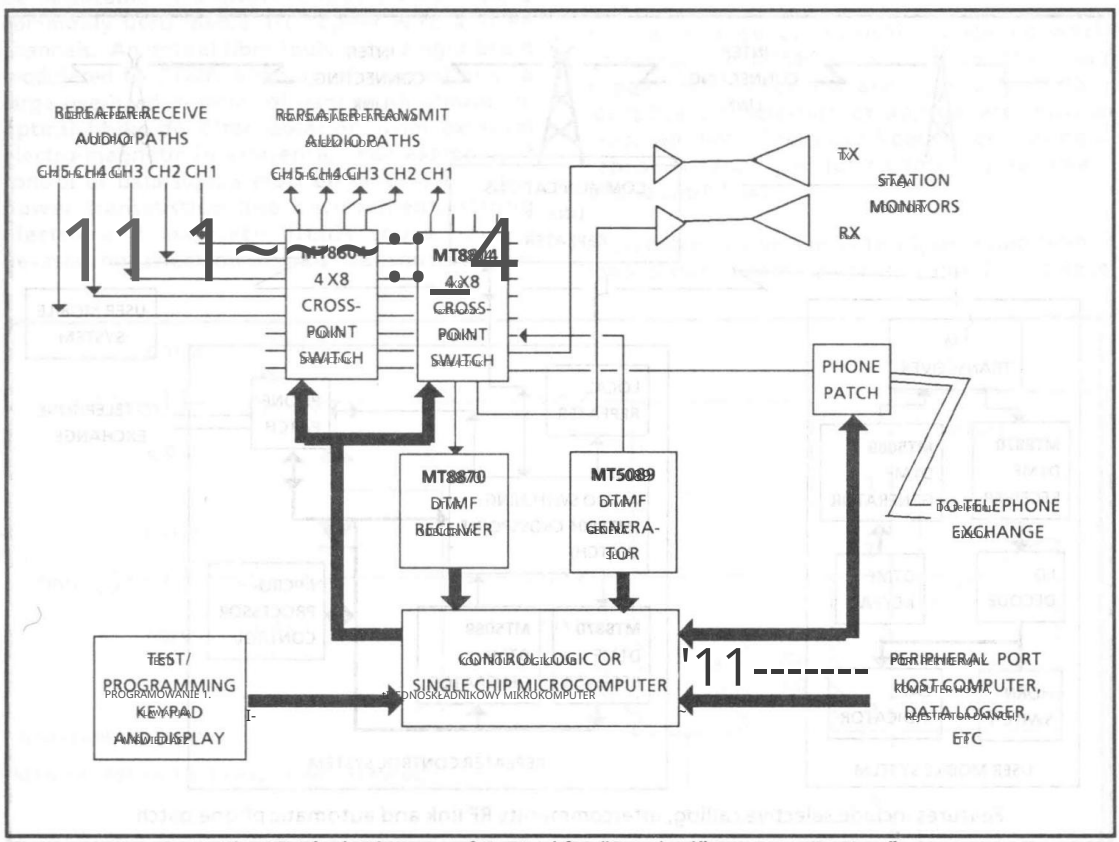

Fig. 13 Block Diagram of Control for "Trunked" Repeater System

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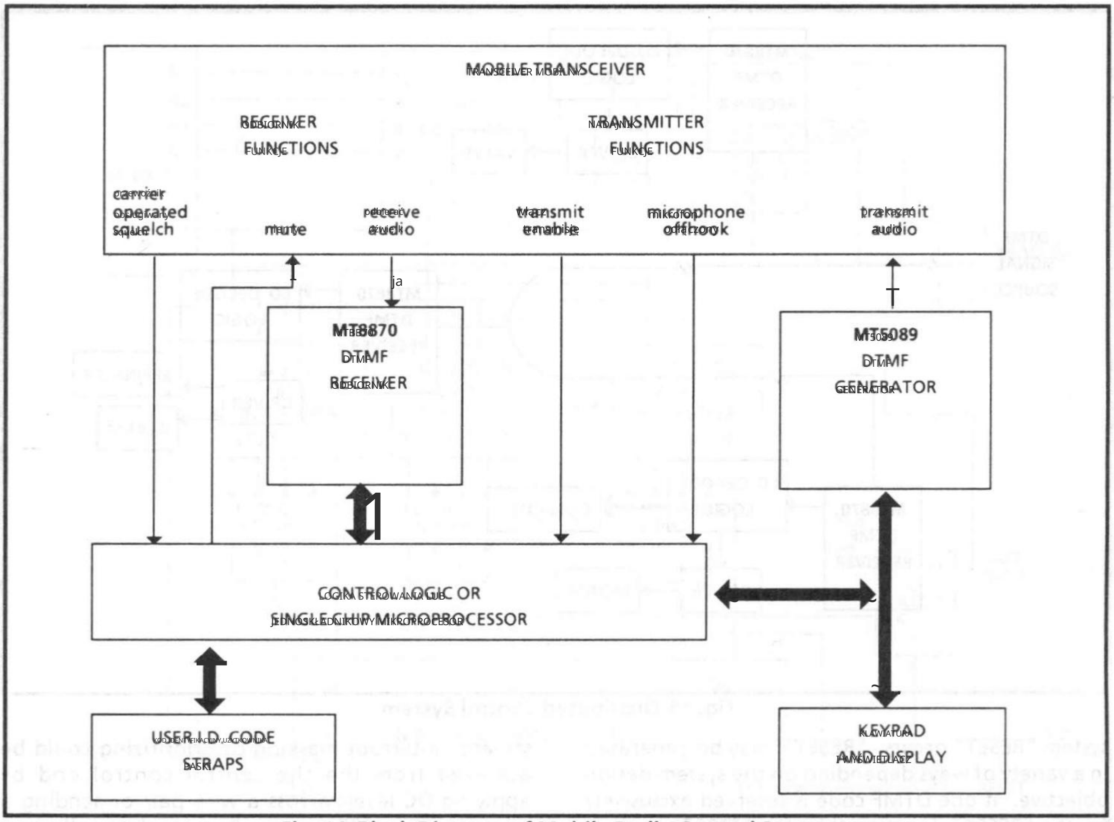

Rys. 14 Schemat blokowy mobilnego systemu sterowania radiowego

Rozproszone systemy sterowania

Istnieje wiele innych zastosowań, które również zaliczają się do rozproszonej klasy komunikacji/kontroli. Oznacza to, że kilka urządzeń jest sterowanych za pomocą wspólne medium komunikacyjne, czy to będzie RF, drut miedziany lub światłowody itp.

Rozważmy na przykład istniejącą parę przewodów krążących w całej roślinie. Łącząc odbiorniki DTMF w strategicznych punktach tej ścieżki można by teoretycznie kontrolować całą roślinę z pojedynczy nadajnik DTMF (rys. 15). Każdy nadajnik DTMF odbiornik będzie monitorować linię wspólną do momentu jej otrzymano określony identyfikator, w którym momencie przesłać dane do jego funkcjonalnego systemu sterowania.

Za pomocą prostej logiki można skonstruować obwód, który rozpoznaje sekwencję zaprogramowanego kodu DTMF. Rysunek 16 ilustruje metodę wykrywania sekwencja kodów DTMF o dowolnej długości, N. Celem jest porównanie N kolejnych 4-bitowych danych DTMF słowa do N zaprogramowanych 4-bitowych słów identyfikacyjnych. Programowanie kodu identyfikacyjnego odbywa się poprzez stosując pożądane poziomy logiczne do wejść N 4-bitowe bufory magistrali. Można to osiągnąć za pomocą pasów h jak pokazano, przełączniki DIP lub pokrętła. Pull-up rezystory należy zastosować do wejść buforowych. Początkowo, po wykonaniu RESETU Q0 z wstępnie ustawialny rejestr przesuwny jest ustawiony logicznie wysoko, pozostałe wyjścia są resetowane. To aktywuje pierwsze bufor magistrali, który stosuje swoje wyjścia do wejść Y komparatora 4-bitowego. Zatrzask „OSTATNIA CYFRA" jest zresetuj, przerzutnik „ERROR-" i „VALID DIGIT" zatrzaski są ustawione. Te trzy sygnały są połączone AND wskazując na stan „no-match". Gdy ważny Po odebraniu sygnału DTMF jego dane pojawiają się na komparatory „X" wejścia, następuje porównanie i wynik pojawia się na wyjściu „X=Y". Po 3.4 µs (typowy) Std wzrasta wskazując, że MT8870 dane wyjściowe są prawidłowe i wysyłają sygnał „X=Y" do Zatrzask „VALID DIGIT". Rejestr przesuwny przesuwa się jedna pozycja, która umożliwia następny bufor magistrali. Jeśli wynik porównania był prawdziwy, wtedy Wyjście "VALID DIGIT" jest wysokie. Wszystkie cyfry sekwencja dopasowania, a następnie wysoki wynik zmiany rejestr „zawija się" od QN do Q0, który miga na wysokim poziomie zatrzasku „OSTATNIA CYFRA". To aktywuje trzy wejścia bramki AND wskazujące na „match" stan. Jeśli otrzymano niezgodne dane, czas trwania sekwencji wykrywania „ERROR-" przerzutnik jest resetowany, co wyłącza bramkę AND do momentu

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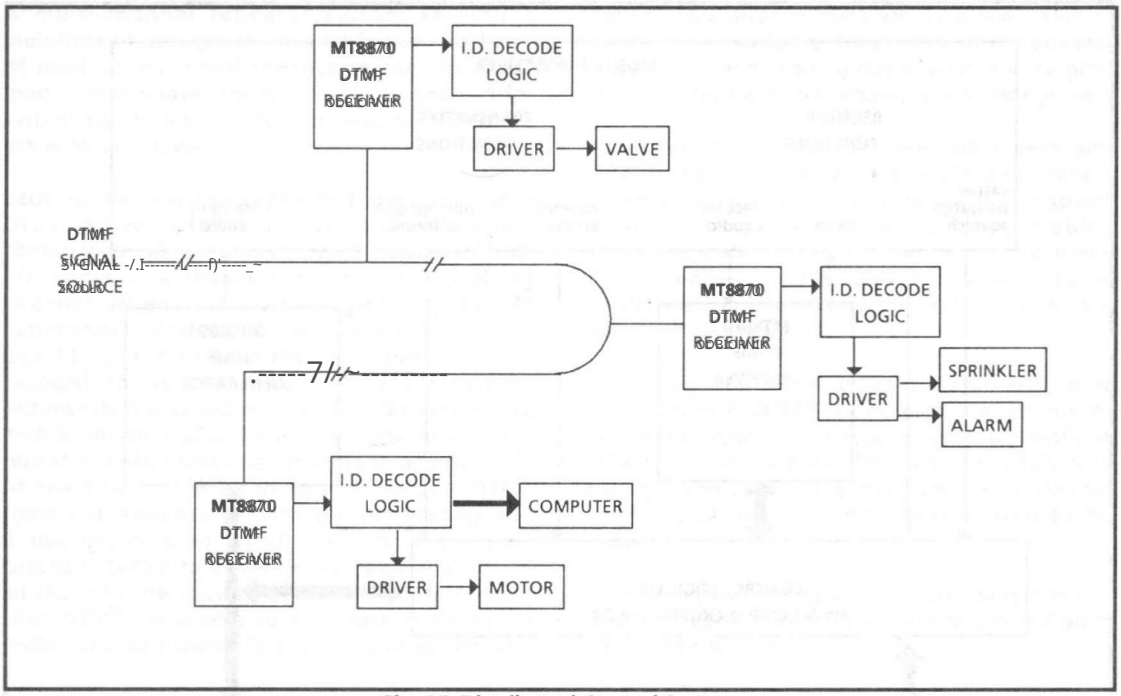

Fig. 15 Distributed Control System

Rys. 15 Rozproszony system sterowania

wystę puje „RESET" systemu „RESET" może zostać wygenerowany

system "RESET" occurs, "RESET" may be generated

in a variety of ways depending on the system design objective. If one DTMF code is reserved exclusively for the "RESET" function then the MT8870 outputs can be decoded directly. This requires that the controller send a "RESET" command prior to sending an I.D. sequence. Alternatively a "time-out" timer, triggered by StD, could serve to generate a system reset if a certain time lapse occurs between received signals. This method places time constraints on the system but eliminates the need to consume a DTMF "RESET" command for the "RESET" function.

The concept of using a common transmission medium for control signalling applies to several possible situations. Plant process control, remote measurement control, selective intercom call systems, institutional intercom systems, two way radio control, pocket pagers and model car or boat remote control, just to mention a few.

Conversely, data could be collected from distributed sources. Implemented on a circulating wire or an RF channel as illustrated in Figure 17, information could be collected by a central unit which individually polls each monitor to ask for data. Alternatively, the system could be interrupt driven (Fig. 18). In this case each monitor, when ready to send data, generates an interrupt request by sending a DTMF "D" sequence followed by a data

wysyłają c sekwencję DTMF "D", po której następ puje sekwencja danych

stream. Interrupt masking or prioritizing could be achieved from the central control end by applying DC levels across a wire pair or sending a pilot tone in an RF system. Remote data collection units would monitor this signal to detect when a higher priority interrupt is being handled or the communications channel is busy.

Data Communication Using DTMF

There is a vast array of potential applications for DTMF signalling using the existing telephone network. Considering that there are millions of ready-made data sets installed in convenient locations (i.e. the Touch Tone™ telephone) remote control and data entry may be performed by users without requiring them to carry around bulky data modems.

Potential applications include:

- home remote control
- remote data entry from any Touch-Tone keypad
- credit card verification and inquiry
- salesman order entry
- catalogue store (stock/price returned via voice synthesis)
- stock broker buy/sell/inquire using stock exchange listing mnemonics
- answering machine message retrieval
- automatic switchboard extension forwarding

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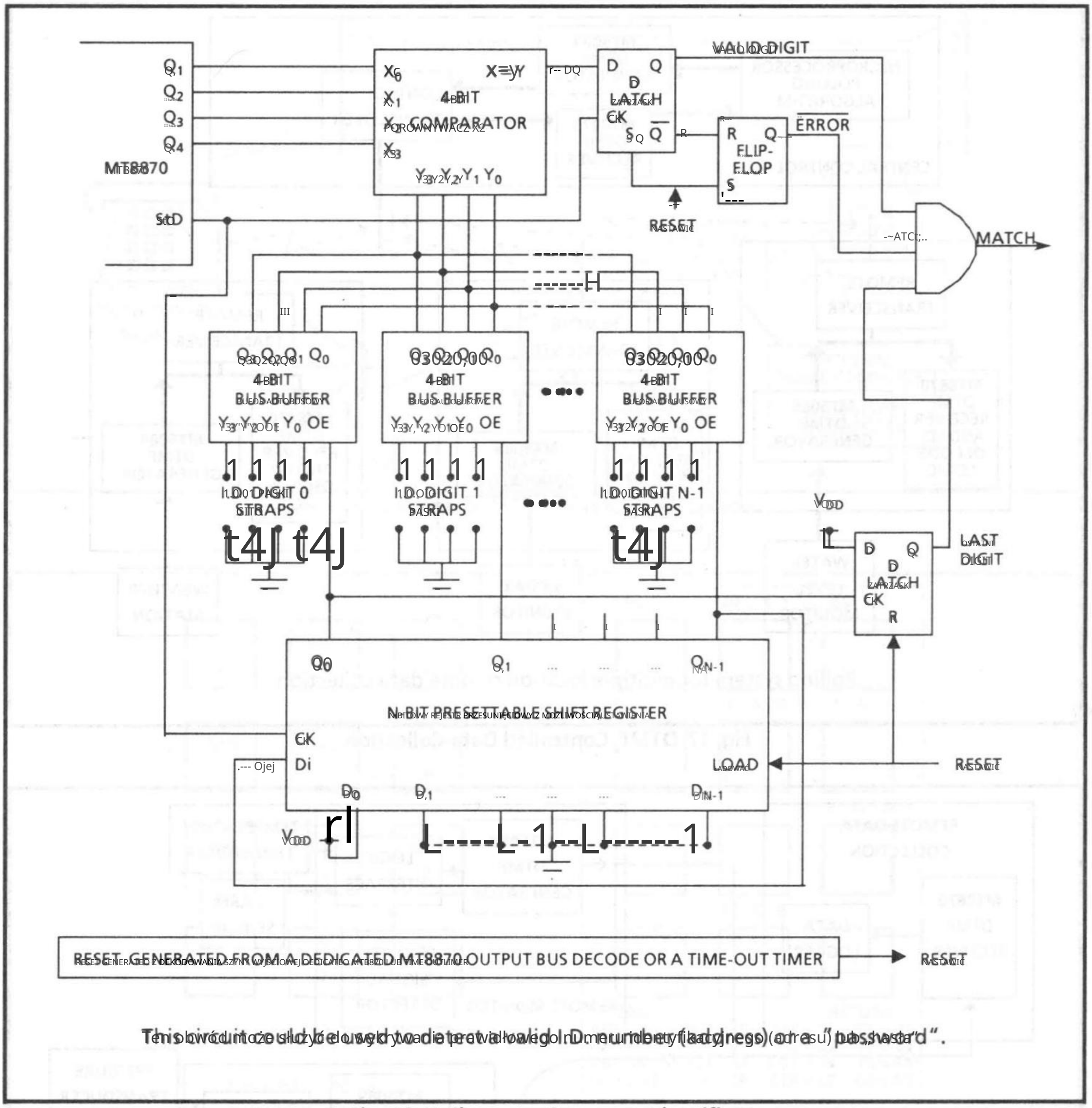

Rys. 16 Identyfikator sekwencji N-znakowej

Domowy system zdalnego sterowania DTMF z opcjonalnym portem danych może pochwalić się różnorodnością wygody (rys. 19). Zdalne sterowanie WŁ./WYŁ. może być podłączony do urządzeń elektrycznych, takich jak wolnowar, kuchenka, oświetlenie zewnętrzne i grzejnik garażowy. Elektromechaniczny zawór elektromagnetyczny umożliwia zdalne sterowanie zraszaczami ogrodowymi. Miłośnicy wideo mogą podłączyć do wejść zdalnego sterowania magnetowidu i nagrywać programy telewizyjne za pomocą kilku naciśnięć klawiszy telefonu przyjaciela. To by poprawiło funkcje timerów, które są obecnie dostępne na większość magnetowidów. Zmiany harmonogramu lub nieoczekiwane transmisje można było przechwytywać z domowego pilota lokalizacja z telefonem Touch-Tone. System bezpieczeństwa może być sterowany mikrofonem, można przełączyć na zdalny monitoring audio. Podłączenie komputera domowego do portu danych stanowi doskonałe centrum wiadomości rodzinnych. W zdalne wiadomości są wprowadzane z klawiatury telefonu. Komputer odpowiada głosem wiadomości generowane przez syntezator mowy. W domu wiadomości, które mają zostać pozostawione, wprowadza się za pomocą klawiatury komputera. Wiadomości do odczytania mogą być wyświetlane na monitorze komputera lub „odtwarzane” z powrotem przez syntezator mowy.

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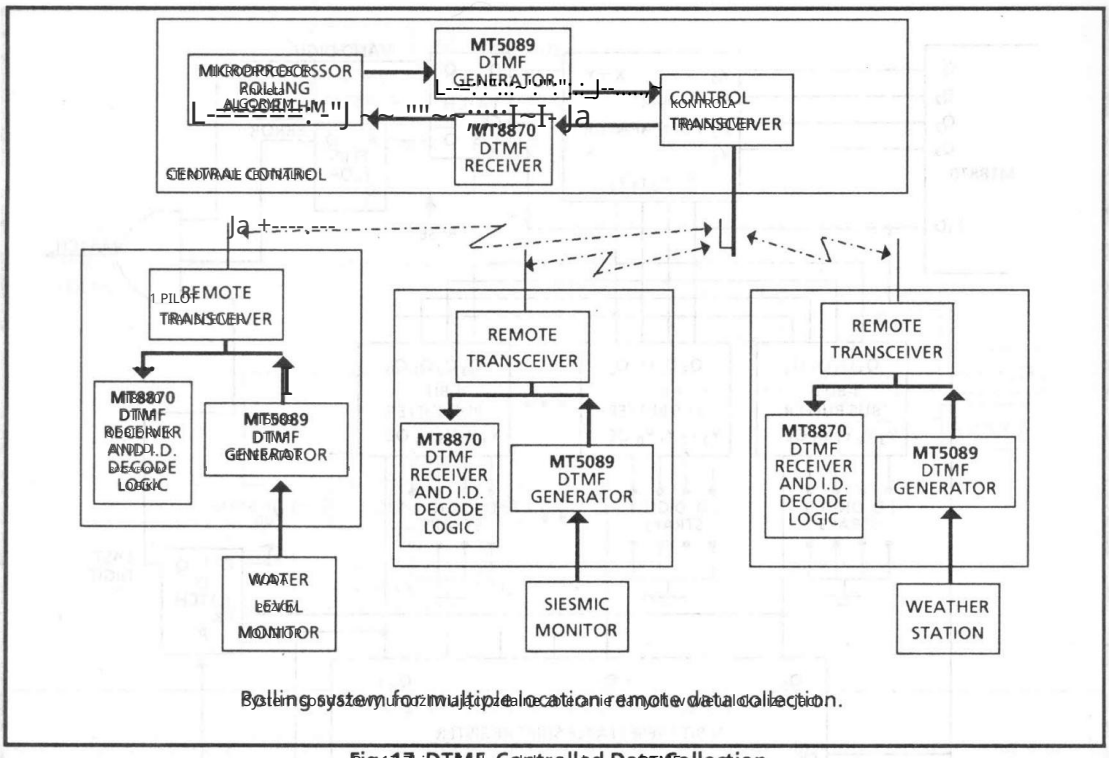

Fig. 17 DTMF Controlled Data Collection

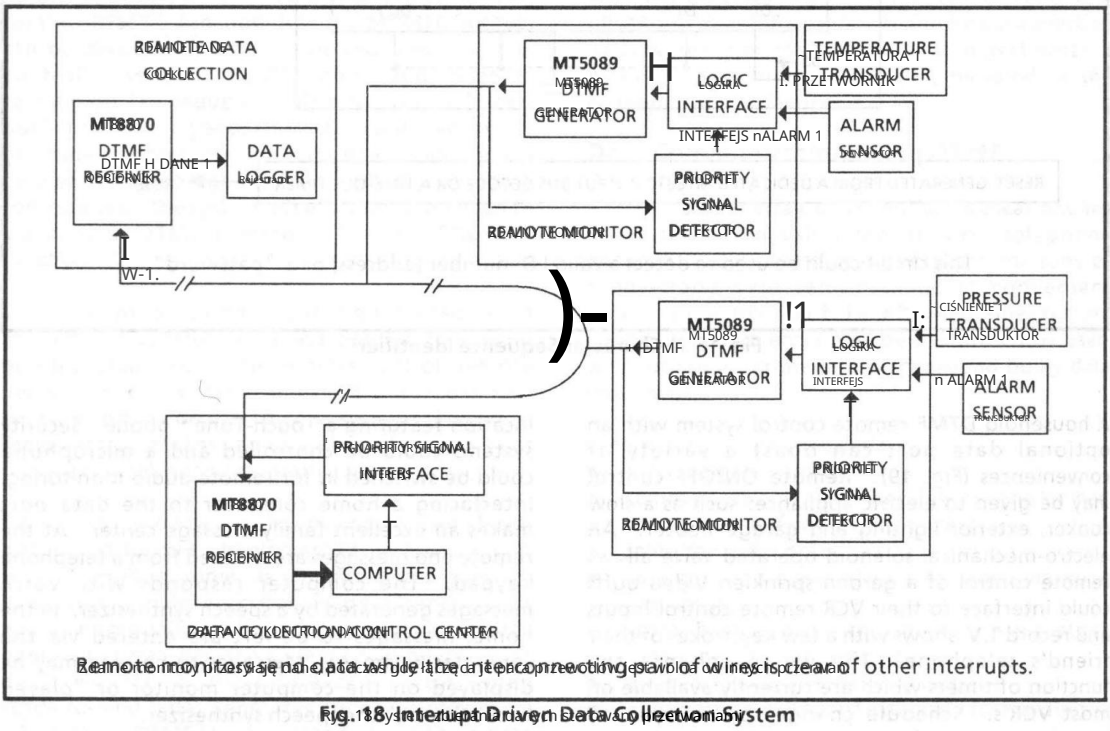

Fig. 18 Interrupt Driven Data Collection System

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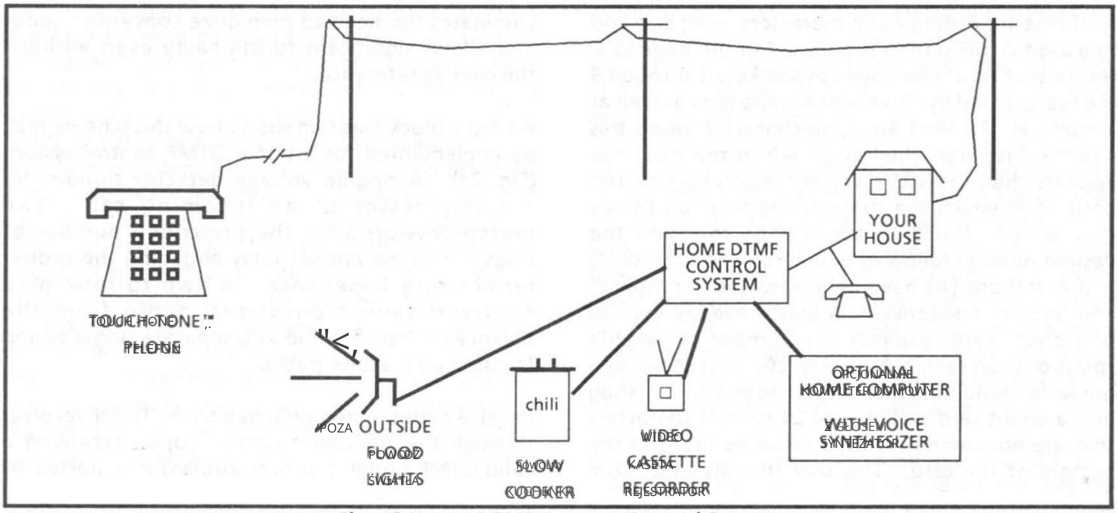
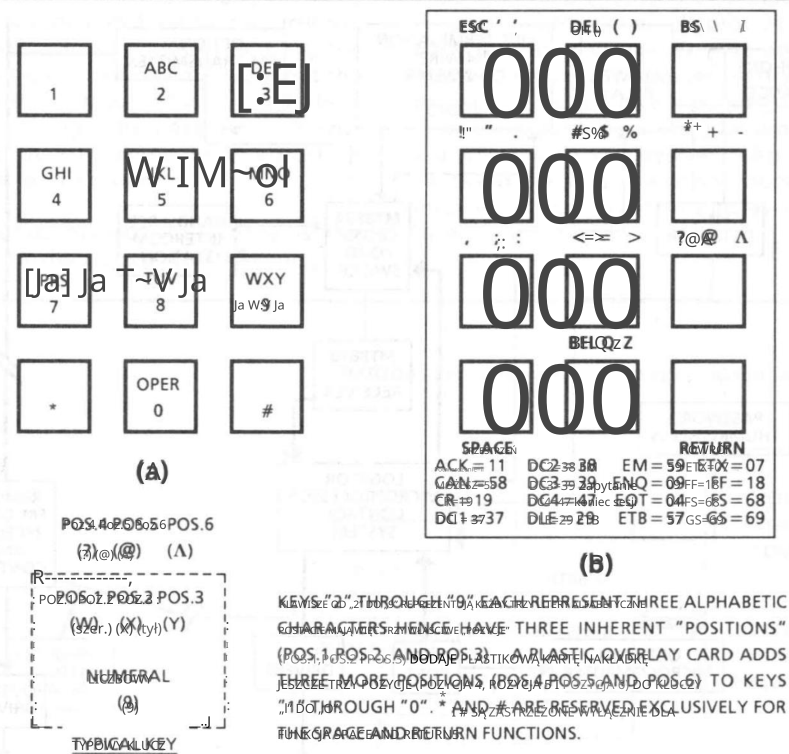


Rys. 19 System zdalnego sterowania DTMF w domu



a) Układ standardowej klawiatury telefonicznej pokazujący pozycje znaków w celu kodowania.
b) Nakładka o rozmiarze karty kredytowej rozszerza funkcję każdego klawisza, dodając trzy dodatkowe pozycje znaków.
Te * i # są zarezerwowane do wysyłania „SPACE” i „RETURN” jako pojedynczych operacji klawiszowych. Każdy znak kod ASCII wymaga dwóch naciśnięć klawiszy. Aby wysłać znak, naciśnij przycisk, na którym się on pojawia, a następnie wciśnij cyfrę odpowiadającą jego pozycji. wyślij "%" wciśnij '5' . Na przykład, aby wysłać „T”, wciśnij „8”, a następnie „1”, a następnie '6'.

Rys. 20 Używanie telefonu z przyciskami jako terminala danych

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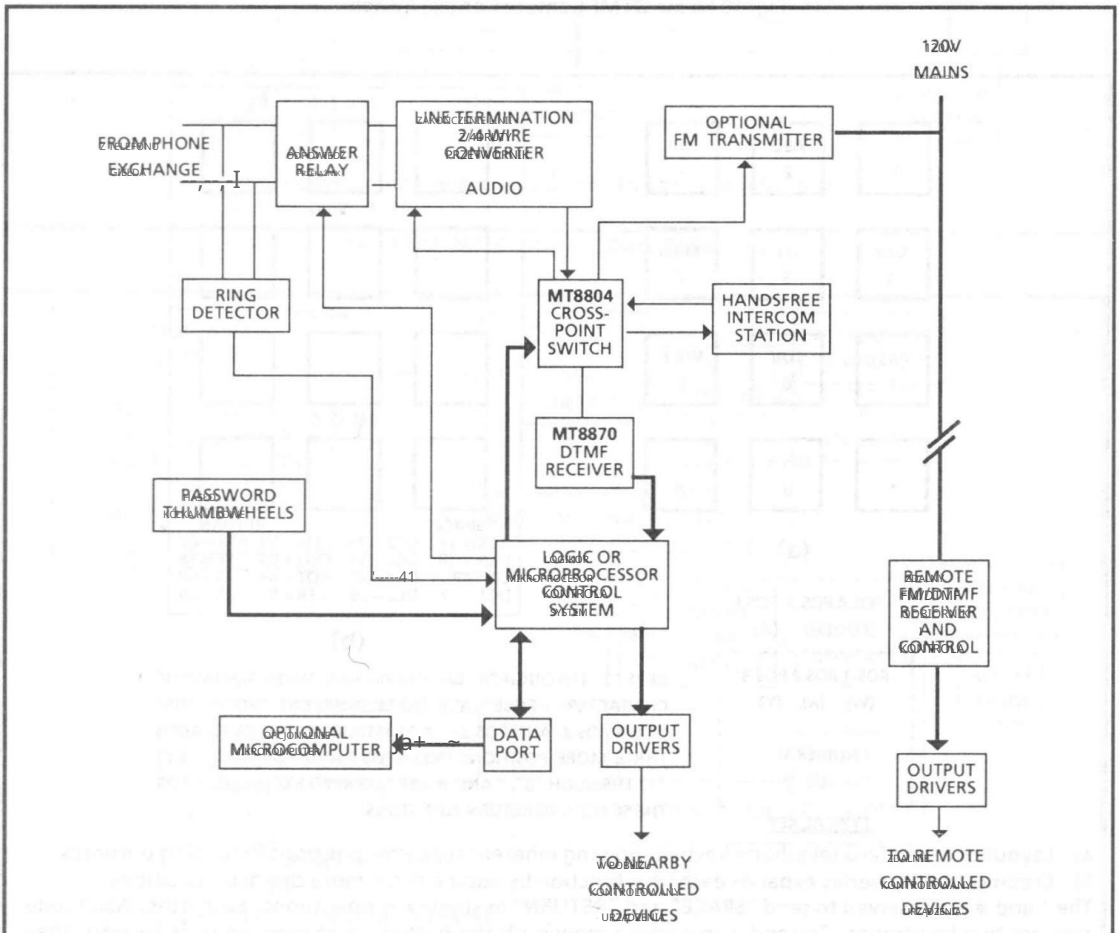
A scheme for coding ASCII characters using one and two digit DTMF signals is outlined in the appendix. Notice that on a telephone keypad keys 2 through 9 are represented by three alpha characters as well as a numeral. To send an alpha character using this scheme, first press the key on which the character appears then press the key corresponding to the position in which the character appears on its key (1, 2 or 3). Numerals are sent by touching the desired number followed by a zero. The asterisk (*) and octothorp (#) have been reserved for "space" and "return" respectively. A plastic overlay the size of a credit card expands the number of useable "positions" on each button (Fig. 20). This serves as a guide for sending other ASCII codes and fits snug into a credit card wallet. ASCII control characters that are not commonly used could be listed at the bottom of the card. This user-friendly algorithm eliminates the need to memorize conversion codes and allows significant functionality even without the overlay reference.

A simple block diagram shows how this scheme may be implemented for a home DTMF control system (Fig. 21). A ringing voltage detector signals the microprocessor of an incoming call. The microprocessor, after the prescribed number of rings, closes the answer relay engaging the proper terminating impedance. A two-to-four wire converter splits bidirectional audio from the balanced telephone line into separate single ended transmit and receive paths.

Receive audio is then switched to the DTMF receiver through the crosspoint switch. Upon receiving a valid DTMF signal, the microprocessor is alerted by



An FM transmitter could be used to couple control signals for distribution over existing power lines. This would eliminate the need for installing wires between the DTMF control unit and remote controlled devices.

Fig. 21 Block Diagram Of Home DTMF Remote Control System

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the rising edge of StD. The microprocessor then checks for a valid password sequence and decodes subsequent commands. A command can be entered to put the system into remote control mode. In this case, the crosspoint switch is configured to route DTMF signals into the FM over-main transmitter as well as the system tone receiver. For warding of control signals is accomplished by applying an FM carrier to the power line. This eliminates the need to string control wires haphazardly about the house. The appropriate device is selected by its unique DTMF I.D. code. The microcomputer keeps track of all device locations and their I.D. codes since it must decide when to supply function outputs to the "nearby" device and when to let the "remote" receivers handle the data. Subsequent data is transmitted to a selected device until a 'reset' command is entered.

Upon receiving any DTMF signal, answer back tones are returned by the microprocessor to acknowledge valid or invalid operations and to indicate the state of an interrogated device. For example, a low to high tone transition could indicate that a particular device is on, high to low transition indicating the off state. A command could be entered to put the system in an 'external' mode which would allow communications through the data port. A host computer could be connected to this port to broaden the scope of the system.

The resident microprocessor contains the software and hardware to control ringing verification, password and command decoding, answer back tone generation, audio routing, output function latches and an optional data port. Output drivers buffer the latches and switch relays or SCRs to control peripheral devices.

An infinite variety of devices could be controlled by such a system, the spectrum of which limited only by the ability to provide appropriate interfacing. This system could also be the heart of a DTMF intercom system allowing intercommunication, "phone patching" and remote control from varied household locations. This type of system concept is, of course, anything but limited to home use. Many applications can provide conveniences to consumers, salespeople and executives.

For example, a merchant could verify credit card accounts quickly utilizing only a telephone keypad for data entry (Fig. 22). Each credit card company could reserve one or more telephone lines to provide this function, reducing the human effort required. The receiving end system would be required to answer the call, provide a short answer back tone or message, receive and decode the credit card account number, verify it, verify the owner's name and give a go/no-go authorization. This return data could easily be provided with the aid of a voice synthesizer. An automatic dialler containing appropriate phone numbers could be installed at the merchant end as an added time saver.

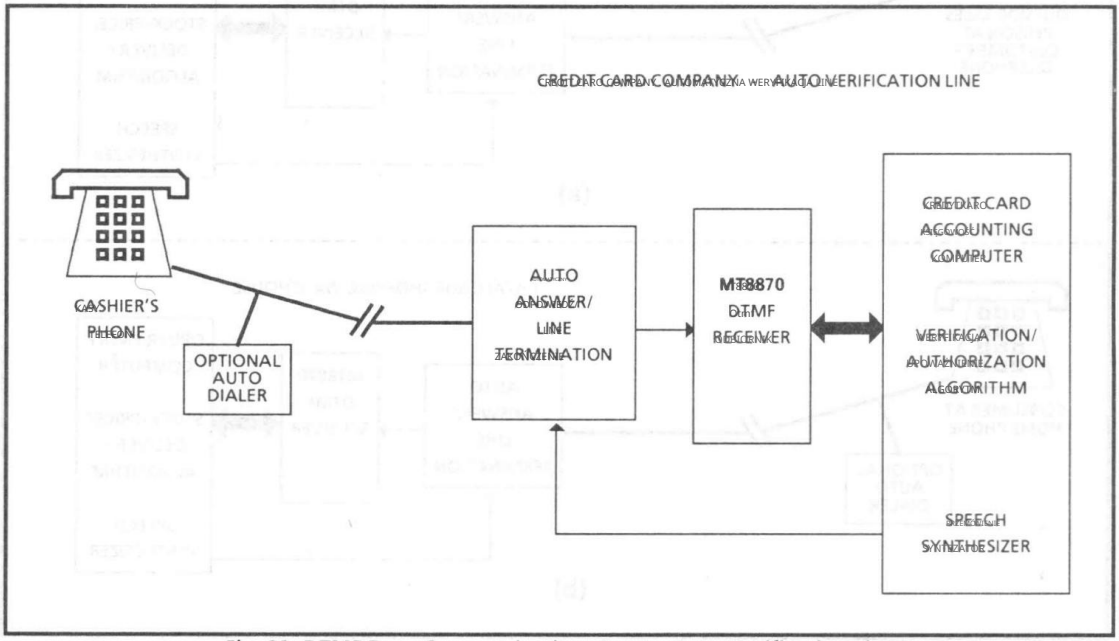

Fig. 22. DTMF Data Communications For An Auto Verification Line

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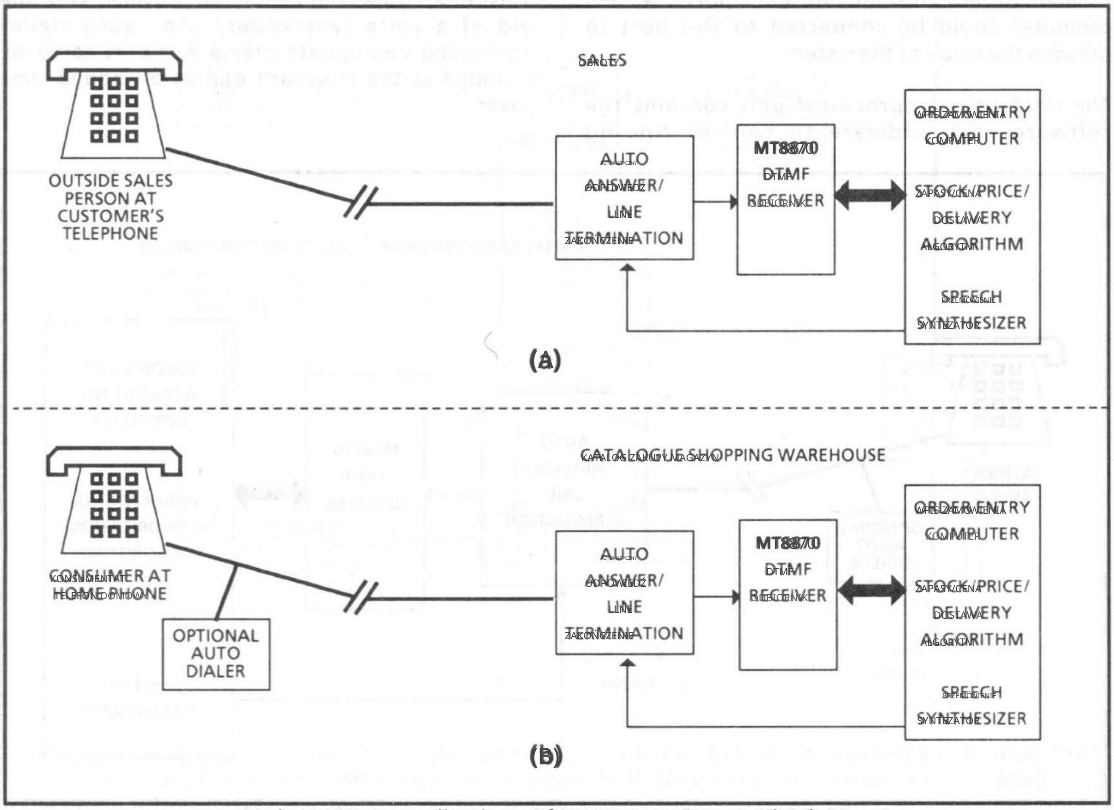
Dzięki podobnemu rozwiązaniu sprzedawca podróżujący mógłby uzyskać dostęp do informacji o cenie, dostawie i statusie klienta, wprowadzać lub usuwać zamówienia towarów i wyszukiwać wiadomości, wszystko z wygody biura klienta (rys. 23a). Dom towarowy mógłby zapewnić swoim klientom usługę zakupów przez telefon, korzystając z wprowadzania danych za pomocą klawiatury telefonu (rys. 23b). Firmy maklerskie wykorzystujące mnemotechniczne notowania giełdowe, mogłyby dostarczać informacji o cenach transakcyjnych i usługi kupna/sprzedaży za pomocą wprowadzania danych za pomocą klawiatury telefonu. Syntezator mowy mógłby dostarczać ceny otwarcia i bieżącej ceny transakcyjnej, wolumen transakcji i inne istotne dane. Producent systemu telefonicznej odpowiedzi mógłby zastosować tę technikę, umożliwiając użytkownikom dostęp do zmianę wiadomości wychodzących i przychodzących z telefonu Touch- Tone ,.

Producent PBX mógłby zaoferować funkcję, która zwalniałaby pracownika centrali telefonicznej z niepotrzebnej interakcji. Połączenie telefoniczne mogłoby zostać odebrane automatycznie, a nagranie mogłoby odpowiedzieć „Dziękujemy za połączenie z Xyz. Wybierz numer wewnętrzny, z którym chcesz się skontaktować, lub zero dla centrali telefonicznej”. Jeżeli dzwoniący zna z góry numer wewnętrzny abonenta, do którego dzwoni, nie trzeba czekać, aż pracownik centrali przekieruje połączenie. Pracownik centrali może zostać powiadomionym o konieczności interwencji, jeśli dzwoniący nie podejmie żadnej akcji dziesięć sekund po zakończeniu nagrywania. Zapewnia to podobną funkcję do łącza „Direct Inward Dialling” (DID), ale bez dodatkowych kosztów związanych z wynajmowaniem bloku numerów telefonicznych, jak w przypadku DID.

Teraz, gdy odbiornik DTMF jest tak łatwy i niedrogi w implementacji, istnieje wiele prostych, dedykowanych zastosowań, które stają się atrakcyjne. Przydatnym zastosowaniem domowym i biurowym dla odbiorników DTMF jest autonomiczny ogranicznik poboru opłat zasilany z linii telefonicznej, podobny do schematu blokowego na rys. 2a. Może on zostać zainstalowany w indywidualnym telefonie lub na przychodzącym zakończeniu głównym, w zależności od tego, który telefon lub telefony mają zostać objęte tym ograniczeniem. Podczas gdy goście nie mogą wykonywać nieautoryzowanych połączeń międzymiastowych, właściciel może nadal chcieć uzyskać dostęp do wybierania numerów za opłatą. Można to zapewnić, dodając obwód logiczny, który wyłącza ogranicznik poboru opłat po otrzymaniu ustalonej sekwencji znaków DTMF (rys. 16). W takim przypadku użytkownik musi wprowadzić swoje hasło przed wybraniem numeru międzymiastowego.



Rys. 23 Dwie aplikacje komunikacji danych DTMF

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Conclusion

The applications for DTMF signalling are tremendous and due to innovative technological advances its use is increasingly widespread. DTMF offers highly reliable, cost effective signalling solutions which require no development effort on the user's part. The advent of single chip receivers has allowed many products that were previously not cost-effective to be manufactured in production quantities.

DTMF signalling was originally designed for telephony signalling over voice quality telephone lines. This signalling technique has been applied to a multitude of control and data communications systems. All that is required is a voice quality communication channel with appropriate interfacing. The applications are limited only by one's imagination.

Zastosowania sygnalizacji DTMF są ogromne i dzięki innowacyjnym postępom technologicznym jej wykorzystanie jest coraz bardziej powszechne. DTMF oferuje wysoce niezawodne, ekonomiczne rozwiązania sygnalizacyjne, które nie wymagają żadnego wysiłku rozwojowego ze strony użytkownika. Pojawienie się jednoukładowych odbiorników spowodowało, że wiele produktów, które wcześniej nie były opłacalne w kosztach produkcyjnych, stało się wykonalnych w produkcji.

Sygnalizacja DTMF została pierwotnie zaprojektowana do sygnalizacji telefonicznej przez linie telefoniczne o jakości głosu. Ta technika sygnalizacji została zastosowana w wielu systemach sterowania i komunikacji danych. Wymagany jest tylko kanał komunikacji o jakości głosu z odpowiednim interfejsem. Zastosowania ograniczone są tylko wyobraźnią użytkownika.

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Appendix

ASCII TO DTMF CONVERSION

Partial ASCII encoding and conversion to 2-sequential DTMF signals

ASCII	HEX	DTMF	ASCII	HEX	DTMF	ASCII	HEX	DTMF	ASCII	HEX	DTMF
ACK	06	11	!	21	44	A	41	21
BEL	07	01	"	22	45	B	42	22
BS	08	34	#	23	54	C	43	23
CAN	18	58	$	24	55	D	44	31
CR	0D	19	%	25	56	E	45	32
DC1	11	37	&	26	79	F	46	33
DC2	12	38	'	27	16	G	47	41
DC3	13	39	(	28	25	H	48	42
DC4	14	47	)	29	26	I	49	43
DEL	7F	24	*	2A	64	J	4A	51
DLE	10	29	+	2B	65	K	4B	52
EM	19	59	,	2C	74	L	4C	53
ENQ	05	09	-	2D	66	M	4D	61
EOT	04	08	.	2E	46	N	4E	62
ESC	1B	14	/	2F	36	O	4F	63
ETB	17	57	0	30	00	P	50	71
ETX	03	07	1	31	10	Q	51	72
FF	0C	18	2	32	20	R	52	73
FS	1C	68	3	33	30	S	53	73
GS	1D	69	4	34	40	T	54	81
HT	09	12	5	35	50	U	55	82
LF	0A	13	6	36	60	V	56	83
NAK	15	48	7	37	70	W	57	91
NUL	00	04	8	38	80	X	58	92
RS	1E	77	9	39	90	Y	59	93
SO	0E	27	:	3A	76	Z	5A	03
SI	0F	28	;	3B	75	[	5B	87
SOH	01	05	<	3C	84	\	5C	35
SP	20	*	=	3D	85	]	5D	88
STX	02	06	>	3E	86	^	5E	96
SUB	1A	67	?	3F	94	_	5F	89
SYN	16	49	@	40	95	`	60	15
US	1F	78				DEL	7F	24
VT	0B	17						

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Applications of the MT3530 300 BPS Single Chip Modem

9761 001 034-NA ISSUE 1 June 1986

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1.0 Introduction

2.0 Inside the MT3530

3.0 Data Communications Systems Using the MT3530

4.0 MT3530 Modem System Configurations

5.0 Diagnostics

6.0 Modem Performance

1.0 Introduction

Modems are used for exchanging information between home computers, personal computers, banks, offices and mainframes, to name just a few possible applications. Computers and other data processing machines work with data in the form of binary pulses, whereas the long distance communication medium, used by the telephone system, requires bandlimited analog signalling. The modem converts digital baseband data to an analog carrier and vice versa so that two devices such as computer and data terminal may communicate over a telephone system.

300 baud modems are among the most common data communications devices in use today. Modem system based on the MT3530, has the advantages of full duplex communication using either Bell 103 or CCITT V.21 Recommendation Standard, a built-in interface to the industry standard RS-232C serial data port, very low system part count, and low power ISO²-CMOS single chip modem I.C.

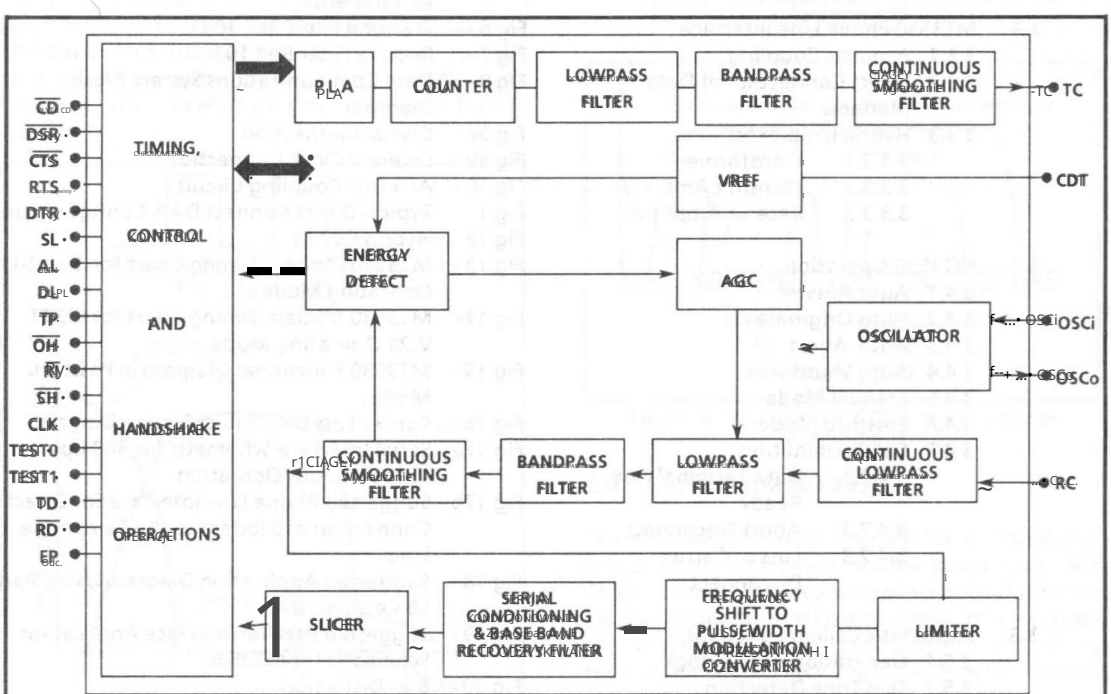

Figure 1. Functional Block Diagram of MT3530 Modem

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1.1 Why are Modems Used?
1.1 Po co używa się modemów?

The digital data signal is typically a random sequence of pulses which has a continuous power spectrum. This spectrum extends to zero frequency, hence transmission via a telephone line is not possible because a phone line is bandlimited. See Figure 2.

Sygnał danych cyfrowych to zazwyczaj losowa sekwencja impulsów, która ma ciągłe widmo mocy. Ponieważ rozciąga się do zerowej częstotliwości, stąd transmisja przez linię telefoniczną nie jest możliwa, ponieważ linia telefoniczna ma ograniczone pasmo. Zobacz rysunek 2.

The purpose of a modem is to translate digital signals into analog signals compatible with the existing telephone network bandwidth of 300 Hz to 3400 Hz. In transmit mode the modem converts binary data into analog signals that the phone line can carry. In the receive mode the modem demodulates the analog signals from the phone line, converting them back to the binary form.

Zadaniem modemu jest tłumaczenie sygnałów cyfrowych na sygnały analogowe, które są kompatybilne z istniejącą pasmową telefoniczną o 300 Hz do 3400 Hz. W trybie transmisji modem konwertuje dane binarne na sygnały analogowe, które może przenosić linia telefoniczna. W trybie odbioru modem demoduluje sygnały analogowe z linii telefonicznej, konwertując je z powrotem do postaci binarnej.

1.2 What is a 300 Baud FSK Modem?
1.2 Czym jest modem FSK 300 Baud?

Bell 103 and CCITT V.21 are both 300 baud modem specifications. They use Frequency Shift Keying (FSK) modulation for data transmission over standard phone lines. FSK encodes binary data into two discrete frequencies within the bandwidth of the media used. A logic "1" in the bit stream places a Mark frequency (Fm) on the phone line. A logic "0" places a Space frequency (Fs) on the line. See Figure 3. Full duplex operation occurs when two-way transmission happens simultaneously between two modems. Since FSK modulation encodes only one bit per baud, it uses approximately 1 Hz of bandwidth for each bit per second of data rate. At 300 bps, two independent channels can be accommodated within the line's bandwidth using Frequency Division Multiplexing (FDM). See Figures 4 and 5.

Bell 103 i CCITT V.21 to obie mają specyfikacje modemu 300 bodów używają modulacji Frequency Shift Keying (FSK) do transmisji danych przez standardowe linie telefoniczne. FSK koduje dane binarne na dwie dyskretne częstotliwości w paśmie używanym przez medium. Logiczna „1" w strumieniu bitów umieszcza częstotliwość Mark (Fm) na linii telefonicznej. Logiczna „0" umieszcza częstotliwość Space (Fs) na linii. Zobacz rysunek 3. Operacja full duplex występuje, gdy transmisja dwukierunkowa odbywa się jednocześnie między dwoma modemami. Ponieważ modulacja FSK koduje tylko jeden bit na bod, wykorzystuje ona około 1 Hz pasma dla każdego bitu na sekundę szybkości transmisji danych. Przy 300 bps, dwa niezależne kanały mogą być umieszczone w paśmie linii przy użyciu Frequency Division Multiplexing (FDM). Zobacz rysunki 4 i 5.

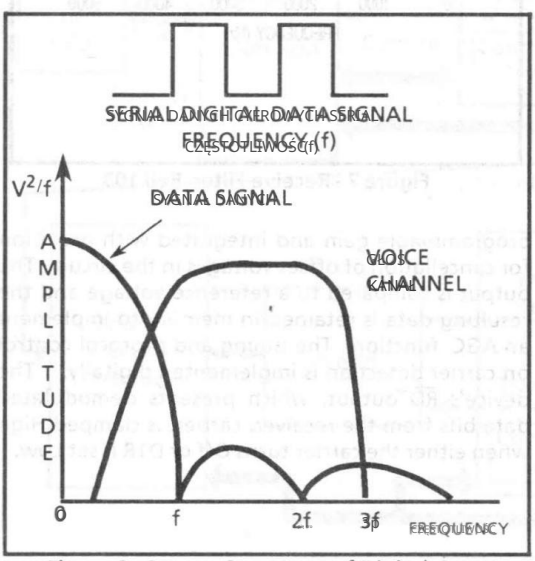

Figure 2 Power Spectrum of Digital Data
Rysunek 2 - Widmo mocy danych cyfrowych

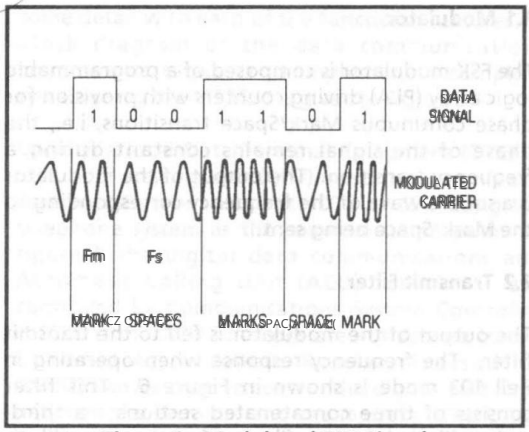

Figure 3 - Modulated FSK Signal
Rysunek 3 - Modulowany sygnał FSK Sygnał

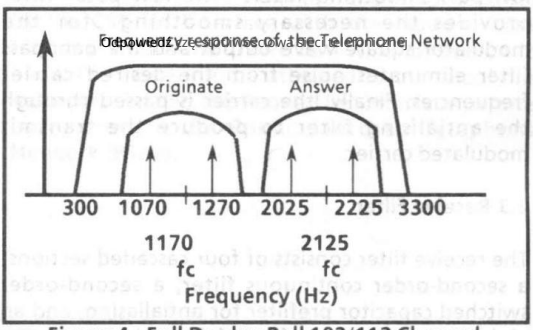

Figure 4 - Full Duplex Bell 103/113 Channel Assignment
Odpowiedź częstotliwości Telefonicznej

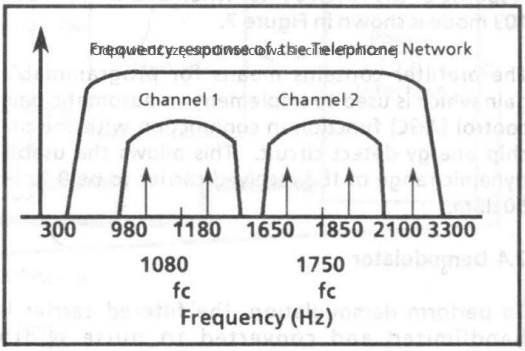

Figure 5 - Full Duplex CCITT V.21 Channel Assignment
Rysunek 5 — Zestaw kanałów Full Duplex CCITT V.21

2.0 Inside the MT3530
Wewnątrz MT3530

The MT3530 is a single chip 300 baud FSK Modem implemented in a 5 volt, double polysilicon, CMOS technology. It consists of six major functional blocks: modulator, transmit filter, receive filter, demodulator, energy detect circuit, and timing, control and handshake logic. A functional block diagram is shown in Figure 1.

MT3530 to jednoprzestrzenny modem FSK 300 bodów zaimplementowany w technologii 5 V, podwójnego polisilikonu ISO2-CMOS. Składa się z sześciu głównych bloków funkcyjnych: modulatora, filtra nadawczego, filtra odbiorczego, demodulatora, obwodu wykrywania energii, logiki pomiaru czasu, sterowania i uzgadniania. Schemat blokowy funkcji pokazano na rysunku 1.

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2.1 Modulator

The FSK modulator is composed of a programmable logic array (PLA) driving counters with provision for phase-continuous Mark/Space transitions, i.e. the phase of the signal remains constant during a frequency transition. The output of the modulator is a square wave of the frequency corresponding to the Mark/Space being sent.

2.2 Transmit Filter

The output of the modulator is fed to the transmit filter. The frequency response when operating in Bell 103 mode is shown in Figure 6. This filter consists of three concatenated sections: a third-order elliptic low pass filter, a fourth-order elliptic bandpass filter and a second-order Sallen and Key low pass smoothing filter. The low pass filter provides the necessary smoothing for the modulator square wave output and the bandpass filter eliminates out-of-band signals at carrier frequencies. Finally, the carrier is passed through the antialising filter to produce the transmit modulated carrier.

2.3 Receive Filter

The receive filter consists of four cascaded sections; a second-order continuous filter, second-order switched capacitor prefilter, antialising and an eighth-order bandpass filter, followed by a second-order continuous smoothing filter. The frequency response of the receive filter when operating in Bell 103 mode is shown in Figure 7.

The prefilter contains means for programmable gain which is used to implement an automatic gain control (AGC) function in conjunction with the on-chip energy detect circuit. This allows the usable dynamic range of the received carrier to be 0 to −50 dBm.

2.4 Demodulator

To perform demodulation, the filtered carrier is bandlimited and converted to pulse width modulation format. This is then introduced to a baseband recovery filter which includes a third-order Bessel low pass filter.

2.5 Carrier Detection

The carrier detect circuit causes the $\overline{CD}$ pin output to turn On and Off at receive carrier levels of −41 and −50 dB, respectively, with appropriate timing. These levels can be modified by applying an external voltage to the device's CDT pin. The filtered receive carrier is rectified with programmable gain and integrated with provision for cancellation of offset voltages in the circuit. The output is compared to a reference voltage and the resulting data is used to implement an AGC function. The timing and protocol control on carrier detection is implemented digitally. The device's $\overline{RD}$ output, which presents demodulated data bits from the received carrier, is clamped High when either the carrier turns Off or DTR is set Low.

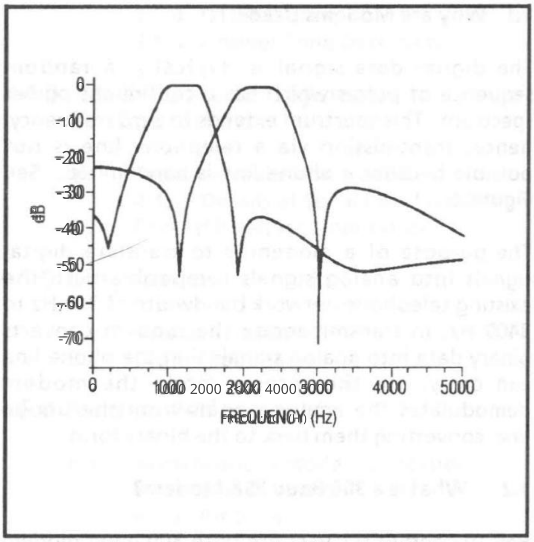

Figure 6 - Transmit Filter Bell 103

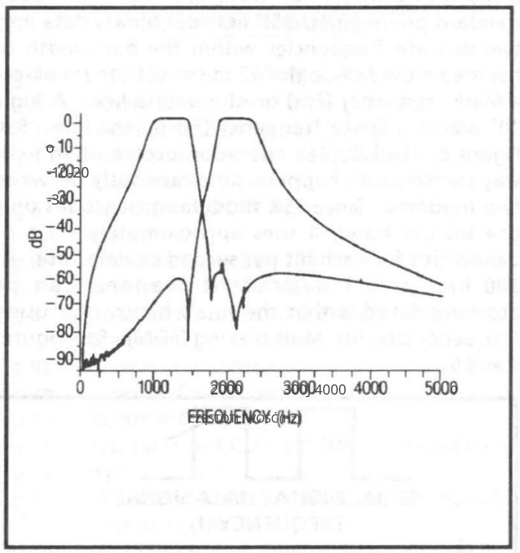

Figure 7 - Receive Filter Bell 103

2.6 Czas, kontrola i uzgadnianie

Ten blok oprócz zapewnienia niezbędnego sygnału taktowania dla różnych części urządzenia, również implementuje interfejs RS232C. Ponadto, sekcja sterowania zapewnia możliwość automatycznego odbierania/wywoływania/wybierania połączeń. Obsługuje interfejs telefoniczny "AP" (Diagnostic ...). Czas i timing operacji wewnętrznej jest sterowany zegarem 3,579545 MHz.

2.7 Inne funkcje

Sekcje nadawania i odbioru są programowalne i mogą być używane w tym samym paśmie częstotliwości, aby umożliwić prawdziwie analogowe możliwości pętli zwrotnej, ułatwiając lokalne testowanie. Zdalne testowanie jest możliwe dzięki włączeniu możliwości cyfrowej pętli zwrotnej.

3.0 System komunikacji danych wykorzystujący MT3530

3.1 Konfiguracja systemu komunikacji danych

Urządzenie MT3530 może zostać skonfigurowane do pracy z bardzo kilkoma zewnętrznymi komponentami. Jednakże, wyrafinowana aplikacja będzie chciała włączyć MT3530 do systemu komunikacji danych składającego się z wielu funkcji funkcjonalnych. Ta sekcja zajmuje się niektórymi szczegółami dotyczącymi każdej z cech funkcjonalnych. Schemat blokowy komponentów komunikacji danych wymaganych do zaimplementowania kompletnego systemu przy użyciu MT3530 pokazano na rysunku 8.

Zwykle lokalny terminal danych (DTE) lub jednostka centralna (CPU) musi przesyłać i odbierać dane z zdalnego DTE lub CPU za pomocą sieci telefonicznej jako ścieżki komunikacji. Rysunek 8 przedstawia cyfrową komunikację danych i funkcje jednostki automatycznego wywoływania (ACU) sterowane przez Kontroler Systemu Komunikacyjnego (CSC). Jeśli funkcja ACU nie jest pożądana, wówczas Uniwersalny Asynchroniczny Odbiornik/Nadajnik (UART) może być używany do sterowania przepływem danych cyfrowych między terminalem a modemem. Typ funkcji sterowania UART jest opisany bardziej szczegółowo w rozdziale 4.2. Informacje kontrolne/dane otrzymane z procesora są warunkowane przez interfejs CSC z modemem. Hybryda zapewnia konwersję z 2-żyłowego na 4-żyłowy, umożliwiając podłączenie modemu do sieci telefonicznej. Na koniec, interfejs linii telefonicznej pozwala na połączenie z publiczną siecią telefoniczną (PSTN).

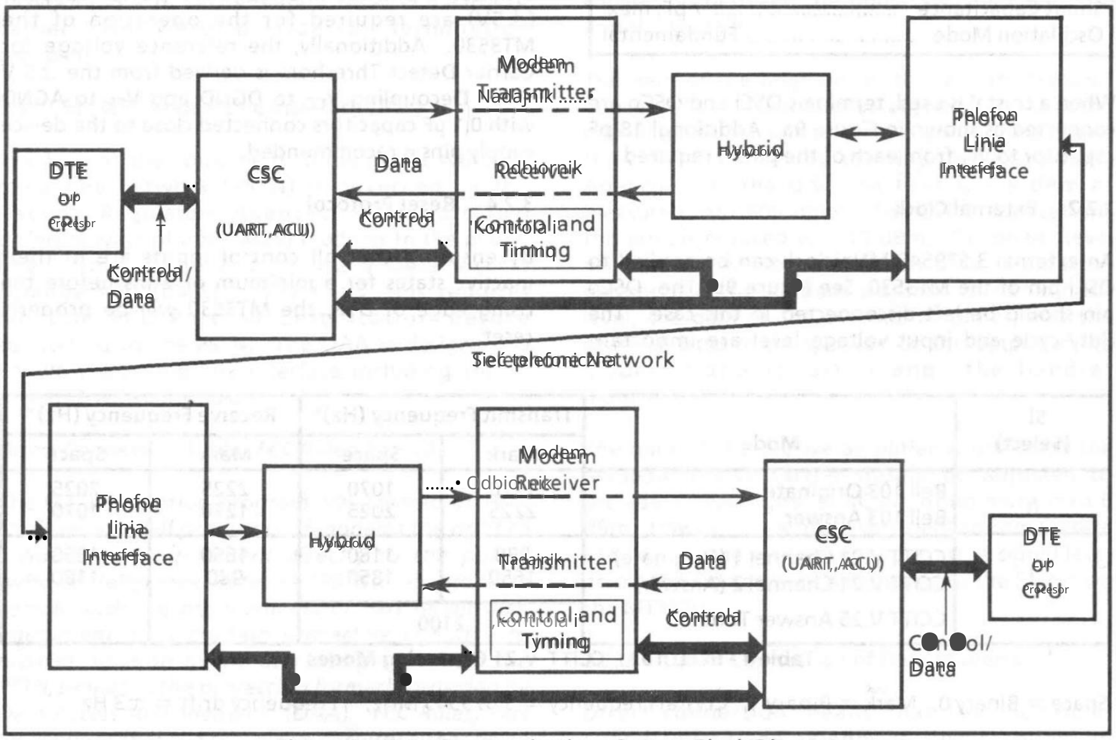

Figure 8 - Schemat blokowy systemu komunikacji danych

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3.2 MT3530 Design In Considerations

In this section, external connections to the MT3530 are defined. Also, special circuit and component considerations for designing the MT3530 based data communications system are explained in detail.

3.2.1 Clock Crystal

The MT3530 has an internal oscillator and clock generator that can be controlled either by an external crystal or external clock. It uses a low-cost 3.579545 MHz crystal as the master clock generator. This crystal is very popular because it is used in all NTSC colour TV's and in many low cost personal computers for interface with TV monitors. The MT3530 can therefore use the same system clock as the display interface. The characteristic of a crystal which is acceptable for use with the MT3530 is given below:

Quartz Crystal Specification (25 °C ± 2 °C)	
Operating Temperature Range	0 °C to 70 °C
Frequency	3.579545 MHz
Frequency Calibration Tolerance	±0.02 %
Load Capacitance	18 pF
Effective Series Resistance	180 ohms max.
Drive Level Correlation/Operating	2 mW
Shunt Capacitance	7 pF max.
Oscillation Mode	Fundamental

When a crystal is used, terminals OSCi and OSCo are connected as shown in Figure 9a. Additional 18 pF capacitor to V_{EE} from each of the pins is required.

3.2.2 External Clock

An external 3.579545 MHz clock can be applied to OSCi pin of the MT3530. See Figure 9b. The OSCo pin should be left disconnected in this case. The duty cycle and input voltage level are important parameters when an external clock is chosen over a crystal. A TTL level, 50% duty cycle, square wave can be applied to OSCi pin through a 0.1 µF decoupling capacitor.

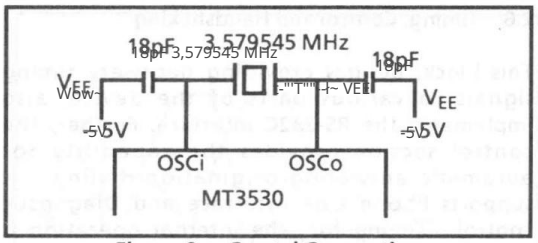

Figure 9a - Crystal Connection

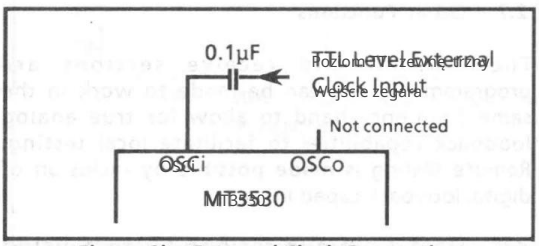

Figure 9b - External Clock Connection

3.2.3 Power Supply Decoupling

Symmetric positive and negative power supplies (±5V) are required for the operation of the MT3530. Additionally, the reference voltage for Carrier Detect Threshold is derived from the ±5 V rails. Decoupling V_{CC} to DGND and V_{EE} to AGND with 0.1 µF capacitors connected close to the device supply pins is recommended.

3.2.4 Reset Protocol

By ensuring that all control inputs are in their inactive states for a minimum of 2 ms before the rising edge of DTR, the MT3530 will be properly reset.

SL (Select)	Mode	Transmit Frequency (Hz)*		Receive Frequency (Hz)*	
		Mark	Space	Mark	Space
0	Bell 103 Originate Bell 103 Answer	1270 2225	1070 2025	2225 1270	2025 1070
1	CCITT V.21 Channel 1 (Originate) CCITT V.21 Channel 2 (Answer) CCITT V.25 Answer Tone	980 1650 2100	1180 1850	1650 980	1850 1180

Table 1 - BELL 103 / CCITT V.21 Operating Modes

Space = Binary 0, Mark = Binary 1, Crystal Frequency = 3.579545 MHz, *Frequency drift = ±3 Hz

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3.2.5 Type Selection

MT3530 is Bell 103/113 and CCITT V.21 compatible. Table 1 illustrates the two types of operating modes. The basic principle is the same but the frequencies and the timings are switched. When in V.21 mode the V.25 Answer Tone of 2100 Hz will be generated upon answering.

3.2.6 Carrier Detect Threshold (CDT)

Applying a voltage between 0 and −5 V dc at this input allows control of the receive carrier detection threshold. This will override the internally determined threshold level of −41 dBm for receive data carrier. Note that when the CDT pin is left open the output voltage level can vary between −1.5 V and −4 V. Therefore, the external voltage level needed to set a required carrier detection threshold will vary from device to device.

3.2.7 Timing Control and Handshake

The RS-232C interface feature facilitates interfacing the modem to a standard RS-232C interface in stand-alone applications or a UART in other applications where the modem is integrated into the Data Terminal Equipment. The control section, in addition, provides the capability for auto answering/origination/pulse dialing. It incorporates a 14 seconds abort timer and a loss of carrier timer which provide call termination capability.

3.3 MT3530 Phone Line Interface (PLI)

Interface of any equipment to the public switched telephone network (PSTN) is governed by the National Regulatory Agencies. There are two different ways of interfacing modems to the phone line. One of these is using a Data Access Arrangement (DAA). In USA this requires meeting FCC Part 68 Certification before connecting to the PSTN. The DAA is designed to handle the phone line interface including the 4-wire to 2-wire conversion.

Direct Connection Under FCC Rules, Part 68

The FCC registration program was created in 1975 to allow non-Bell products the right to connect their equipment directly to the public switched telephone network (PSTN). In order to comply with the requirements of Part 68, all such equipment must contain protective circuitry to provide isolation to the user equipment from the PSTN, similar to the protection formerly provided by Data Access Arrangements (DAA). FCC Rules, Part 68, requires that the protective circuitry either be an integral part of the modem and registered as the terminal device or that the protective circuitry be separate from the modem and registered as protective circuitry. Under FCC Rules, Part 68, this registration class is "Terminal Device" and equipment type is "Data Modems".

The second Public Switched Telephone Network connection scheme uses an acoustic coupler. An acoustic coupler uses the existing telephone handset and is not directly connected to the phone line.

3.3.1 Acoustic Coupling

The MT3530 can be connected to the telephone network using an acoustic coupler. Figure 10 shows how acoustic coupling is accomplished. No component values are given because the speaker and microphone impedance characteristics can vary.

Typically, the modem's transmitted carrier is amplified through a speaker and presented to the mouthpiece of a standard telephone handset. The modem received carrier signal is derived from the earpiece of the same handset by a microphone; the signal is then attenuated and presented to the modem. Note that there is a hybrid in the telephone handset that performs a 2-wire to 4-wire conversion between the public switched network and the MT3530.

The gain of the amplifier at the modem Transmit Carrier output (TC) should be adjusted such that the maximum signal power on the phone line is less than the limits set by the National Regulatory Agencies. In the US, this limit is −9 dBm as measured into 600 ohms. For CCITT applications this limit is reduced to −13 dBm. The power level on the line will be a function of a number of parameters; the modem transmit carrier output level, the gain of the external amplifier, and the characteristics of the speaker on the output of the modem transmit carrier and the handset mouthpiece.

The gain of the receive amplifier which feeds the MT3530 receive carrier should be adjusted to provide a peak signal at RC pin of no more than 0 dBm. However it is often sufficient to compensate the gain of the receive op-amp so that signal level across the Tip and Ring is delivered to the RC pin on the MT3530 .

3.3.2 Direct Connection of Data Modems

Direct connection means that the modem is connected to the telephone line through an

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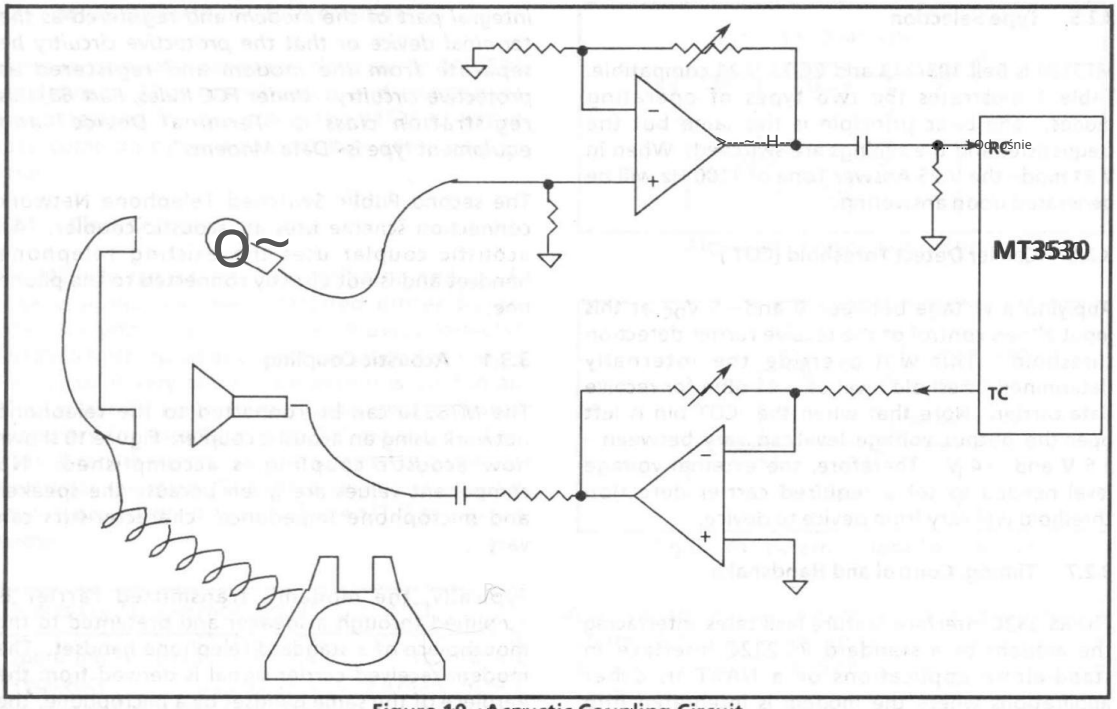

Figure 10. Acoustic Coupling Circuit

approved interface device termed Data Access Arrangement (DAA).

The prime elements of the DAA are transmit signal level, impedance matching, line isolation, transient protection and the billing timing delay. Other functions integral to the DAA include ring detect and switch-hook circuitry.

Any equipment connected to the switched telephone network must meet specifications of "programmable" or "non-programmable" type. The most commonly used is permissive specification. In this arrangement the level must not be greater than −9 dBm as measured into a 600 Ω load averaged over three seconds. For CCITT applications this should be no greater than −13 dBm. The MT3530 transmit carrier output is limited at −8 ± 1 dBm.

Standard termination is defined as 600 Ω and is the reflected impedance required by the primary of the transformer. This impedance matching of the transformer AC impedance (600 Ω) represents the nominal AC impedance of the phone line which changes with frequency and conductor type and size. Off-hook DC resistance of the terminal equipment circuitry is preferred to be less than 200 Ω.

Figure 11 illustrates a typical Direct Connect DAA.

A set of standard requirements for an isolation transformer is as follows:

- Primary Impedance: 600 Ω;
- Secondary Impedance: 600 Ω (nominal);
- Maximum DC Current: 90 mA (*Note 1*);
- Frequency Response: 300 - 3000 Hz ±0.05 dB;
- DC Resistance: Preferably less than 200 Ω. This is in compliance with FCC Rules, Part. 68.31;
- Echo Return Loss: 20 dB (*Note 2*);
- Dielectric Strength: 1500 V AC or greater between primary and secondary. The core is to comply with FCC Rules, Part 68.302 and 68.304.

Note 1: As an alternate design, additional electronic components may be used to shunt DC line current, thus allowing use of a smaller transformer which would only carry an AC signal component. The holding coil then provides the DC path for the holding current provided by the Central Office.

Note 2: Impedance mismatches at the telephone line interface will reflect incoming signals back into the telephone network at a reduced level. This is known as echo return loss.

High voltage transient surge protection is usually performed with bidirectional Zener diodes which limits the potential between Tip and Ring to a specified threshold (1500 V in the U.S.). The series resistor is inserted for short circuit current limiting. Zener protection may also be provided on the secondary side of the isolation transformer.

When answering a telephone, per FCC Part 68 of

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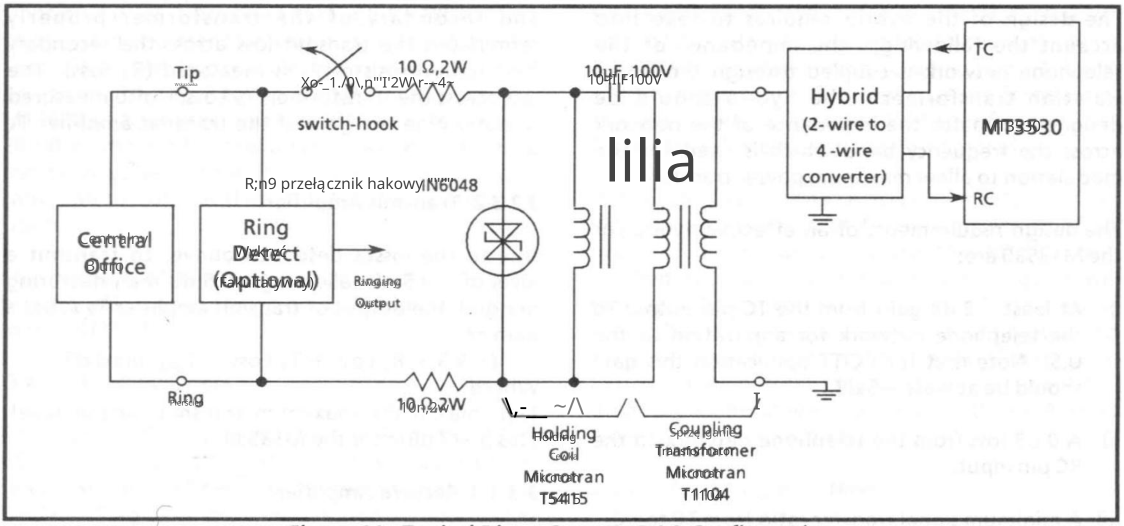

Rysunek 11 – Typowa konfiguracja DAA z bezpośrednim połączeniem

Zasady FCC określają, że użytkownik musi zapewnić ciszę (bez danych) na linii telefonicznej trwającą co najmniej dwie sekundy w celach rozliczeniowych, zanim jakiekolwiek dane lub sygnał odpowiedzi zostaną przesłane. CCITT określa ciszę trwającą od 1,8 do 2,5 sekundy. MT3530 zapewnia ciszę trwającą co najmniej 2,0 sekundy w trybie odpowiedzi.

Obwód DAA może być używany w aplikacjach automatycznej odpowiedzi z dodatkiem obwodu wykrywania dzwonienia. Wymagania obwodu wykrywania dzwonienia są następujące:

i) Spełniać wymagania dotyczące udaru wzdłużnego o napięciu 1500 V lub udaru metalicznego o napięciu 1000 V określone w przepisach FCC Rules, część 68.302;

ii) zapewniać minimalną rezystancję odwieszenia DC wynoszącą 10 MΩ przy napięciu 100 V DC i 3 kΩ przy napięciu 300 V DC oraz impedancję prądu przemiennego przy odwieszeniu mniejszą niż 40 kΩ, ale większą niż 1600 Ω zgodnie z przepisami FCC, część 68.312;

iii) Zapewnia odporność na fałszywe wykrycie wywołania przez impulsy tarczowe generowane przez inne telefony, które łączą tę samą parę metalową w modemie danych;

iv) Reagować na przychodzące napięcie dzwonienia wynoszące od 40 V_{RMS} do 150 V_{RMS} przy częstotliwości od 16 Hz do 68 Hz;

v) Zgodnie z dokumentem Bell System Technical Reference PUB61100 obwód detekcji dzwonka powinien ignorować prawidłowe serie dzwonków o długości 125 ms lub mniejszej.

Interfejs DAA łączy się z PSTN za przewodami Tip i Ring. Przekaźnik zapewnia sterowanie podnoszeniem/odkładaniem słuchawki w celu połączenia lub rozłączenia z

linią. Gdy DAA jest podniesiona, przekaźnik jest zamknięty, a prąd pętli przepływa przez transformator izolacyjny (lub cewkę podtrzymującą), a reszta DAA jest podłączona do linii. Oznacza to chęć wykonania połączenia lub odebrania połączenia. W trybie odpowiedzi po wykryciu sygnału dzwonka modem jest podłączony. Linia sterująca podniesieniem słuchawki może być również używana do wybierania impulsowego zgodnie z Bell Technical Reference PUB 1100, pod warunkiem, że telefon jest podniesiony.

Wymagania dotyczące przekaźnika są następujące:

i) Spełniać lub przekraczać kryteria FCC Rules, część 68.302 i 68.304. Zasady te dotyczą symulacji środowiskowej i prądu upływu;

ii) Dostępny ze stykami ze srebra i palladu pokrytymi złotem, do zastosowań w automatach wybierających numery;

iii) Minimalne możliwe zużycie energii;

iv) Długa żywotność określona w minimalnej liczbie operacji (przesyłek kontaktowych);

v) Oznaczenie 75 Vdc przy prądzie pętli DC 70 mA i napięciu 150 V AC, przy prądzie pierścieniowym AC 130 mA.

3.3.3 Hybrydowy (dupleksor)

Odbiornik i nadajnik modemu wymagają jednej pary przewodów do fizycznego połączenia. W przypadku standardowych połączeń PSTN dostępna jest tylko jedna para przewodów. Dlatego do połączenia modemu z siecią telefoniczną używany jest duplekser lub hybryda elektroniczna (znana również jako konwerter 2-żyłowy na 4-żyłowy).

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The design of the hybrid requires to take into account the following: the impedance of the telephone network coupled through the DAA's isolation transformer. The hybrid should be designed to match the impedance of the network across the frequency band which is used for the modulation and has maximum power transfer.

The design requirements of an effective hybrid for the MT3530 are:

i) At least 2 dB gain from the TC pin output to the telephone network for application in the U.S. Note that for CCITT application this gain should be at least −5 dB.

ii) A 0 dB loss from the telephone network to the RC input.

iii) A minimum signal transfer ratio from TC to RC.

Figure 12 illustrates a hybrid circuit using operational amplifiers. The design calculations include the following: Transformer, Transmit Amplifier and Hybrid Receive Amplifier.

3.3.1 Transformer (T1 in Figure 12)

Standard termination is defined as 600 Ω and is the reflected impedance required by the primary of the transformer. In this design a representative transformer is selected and the secondary termination resistance is determined (equivalent to R_1) for reflected impedance of 600 Ω at the primary.

The receive loss (R_X Loss) from primary to secondary needs to be measured and must be compensated for by the receive amplifier R_XA. With the primary and secondary of the transformer properly terminated, the transmit loss across the secondary termination resistor R_1 is measured (R_1 loss). The loss across the transformer T_X Loss is also measured to determine the gain of the transmit amplifier T_X A.

3.3.2 Transmit Amplifier

Due to the losses described above, to transmit a level of −9.5 dB (allowing a 0.5 dB manufacturing margin), the output of transmit amplifier T_X A has a gain of:

$(-9.5 \text{ dB} + R_1 \text{ Loss} + T_X \text{ Loss} - T_{OUT} \text{ max})$ dB.

Where:

T_{OUT} max is the maximum transmit output level. This is 7 dBm for the MT3530.

3.3.3 Receive Amplifier

The hybrid receive amplifier R_XA requires that the maximum level which can be applied to the RC input of the MT3530 is 0 dB. Therefore, the voltage output of the receive amplifier should not exceed 0 dB. The receive amplifier must, also, make up for transformer receive port insertion loss, R_X Loss. However, this is often sufficient for the receive amplifier gain to be such that the signal across Tip and Ring is delivered to the Receive Carrier pin at the same level. The receive amplifier R_XA, then, has a gain of: R_X Loss dB.

Although the MT3530 provides 55 dB of adjacent channel rejection, the hybrid receive amplifier can be used for additional rejection of transmit signal through use of differential amplifier techniques. Resistor R_2 from the Transmit Carrier pin to the inverting input of the receive amplifier balances the common mode signals.

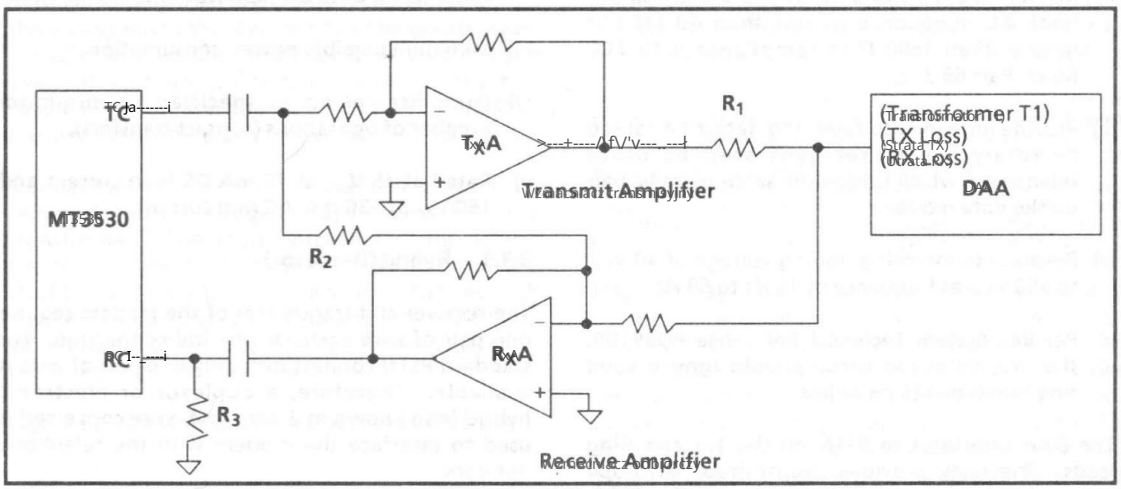

Figure 12 – Hybrid Circuit

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transmit carrier is provided through a 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Receive Carrier input on the MT3530 at a reduced level. Under ideal conditions 20 dB or more of cancellation might be achieved, but because telephone lines vary considerably, cancellation not less than 10 dB is a more realistic figure.

The purpose of the termination resistor, R_T, is to provide a DC bias to the op amp of the receive filter in the MT3530.

3.4 MT3530 Operation

The modem IC may be operated in Bell 103/113 or CCITT V.21 type applications. Logic control on select (SL) pin defines the operating mode. See Table 1. Two diagnostic modes, analog and digital loopback, allow for system tests. Refer to Section 5.0 for details. In addition, Pass-thru mode is available, which the ringing and tone detection and handshake depedence can be suspended.

3.4.1 Auto Answer

In the Answer mode the MT3530 stands idle waiting for an incoming call. To assist in answering incoming calls, the ring indicate signal (RI) from DAA is connected to the $\overline{RI}$ pin of the MT3530. With DTR High and RTS Low, a low on $\overline{RI}$ causes the device to go off-hook and initiate Auto Answer sequence. The MT3530 then initiates Auto Answer sequence by setting $\overline{OH}$ and DSR Low (See Figure 13). $\overline{OH}$ Low enables the hookswitch relay, thereby connecting the modem to the telephone line. The duration of $\overline{RI}$ Low should be greater than 107 ms otherwise the device will ignore it. The modem commences 2.0 seconds (minimum) of silence followed by Answerback Tone. This is a 2225 Hz (Mark) carrier when operating in Bell 103 mode. The generation of Answer Tone continues until:

i) The 1270 Hz (Mark) carrier from the originating modem is detected and the answering modem automatically picks up within 100 ms setting $\overline{CD}$ and $\overline{CTS}$ Low. This completes the handshaking sequence and communication is established;

or

ii) DTR is set Low. See Reset Protocol in Section 3.2.4 for details.

If no Answer Tone is detected within 14 seconds of being put into Answer mode the modem will abort the call. Refer to Auto Abort section 3.4.3 for details.

When operating in V.21 mode the V.25 Answer Tone of 2100 Hz is generated for 3.4 seconds, 80 ms later 1650 Hz (Mark) carrier is generated. The rest is the same as Bell 103 except that the frequencies and timings are switched to V.21 specification. See Figure 14 and Table 1 for additional details.

If the chip is in the Answer mode and an originating modem not following Bell or CCITT protocol sends carrier before the MT3530 has finished the Auto Answer sequence the modem will lock-up. This means that there will be Carrier Detect but handshaking will not be completed and data will not be transferred. This is of particular importance in Mailing application because the duration of the answer sequence with the Answer Tone is almost six seconds.

3.4.2 Auto Originate Mode

With DTR High a call is initiated by applying a High to the RTS input. This will cause $\overline{OH}$ to go Low, enabling the hookswitch relay and connecting the telephone line. This puts the MT3530 in the Auto Originate mode. When dial tone is detected, RTS can be pulsed Low/High to provide dial pulses. The $\overline{OH}$ will follow the RTS pulses, sending the desired digits over the telephone line. The proper timing for dialing must come from the Data Terminal on the RTS line.

When the answering modem comes on line it will wait for 2.0 seconds "silent" (no carrier) and then send the 2225 Hz Answer Tone for Bell 103 operating mode. Refer to Figure 13. Note that if the answering modem sends a carrier within 2.0 seconds, the modem will lock up. The $\overline{CD}$ pin output on the originating modem will go Low 200 ms (max.) later indicating the received carrier. 236 ms (max.) later, the MT3530 will respond with 688 ms (max.) of 1270 Hz carrier. At the end of that time $\overline{CTS}$ (Clear-To-Send) will go Low indicating to the Data Terminal Equipment that the communication link has been established. If no carrier is detected within 14 seconds of being put into Originate mode, the modem will abort the call.

When V.21 mode is selected, the same but the frequencies and timings are switched to V.21 specifications. See Figure 14 and Table 1 for additional details.

3.4.3 Auto Abort

There is an automatic abort feature in the MT3530 to avoid tying up system when there is difficulty in establishing the link. If no carrier is detected within 14 seconds after the device was put into the Answer or Originate mode it will abort the call

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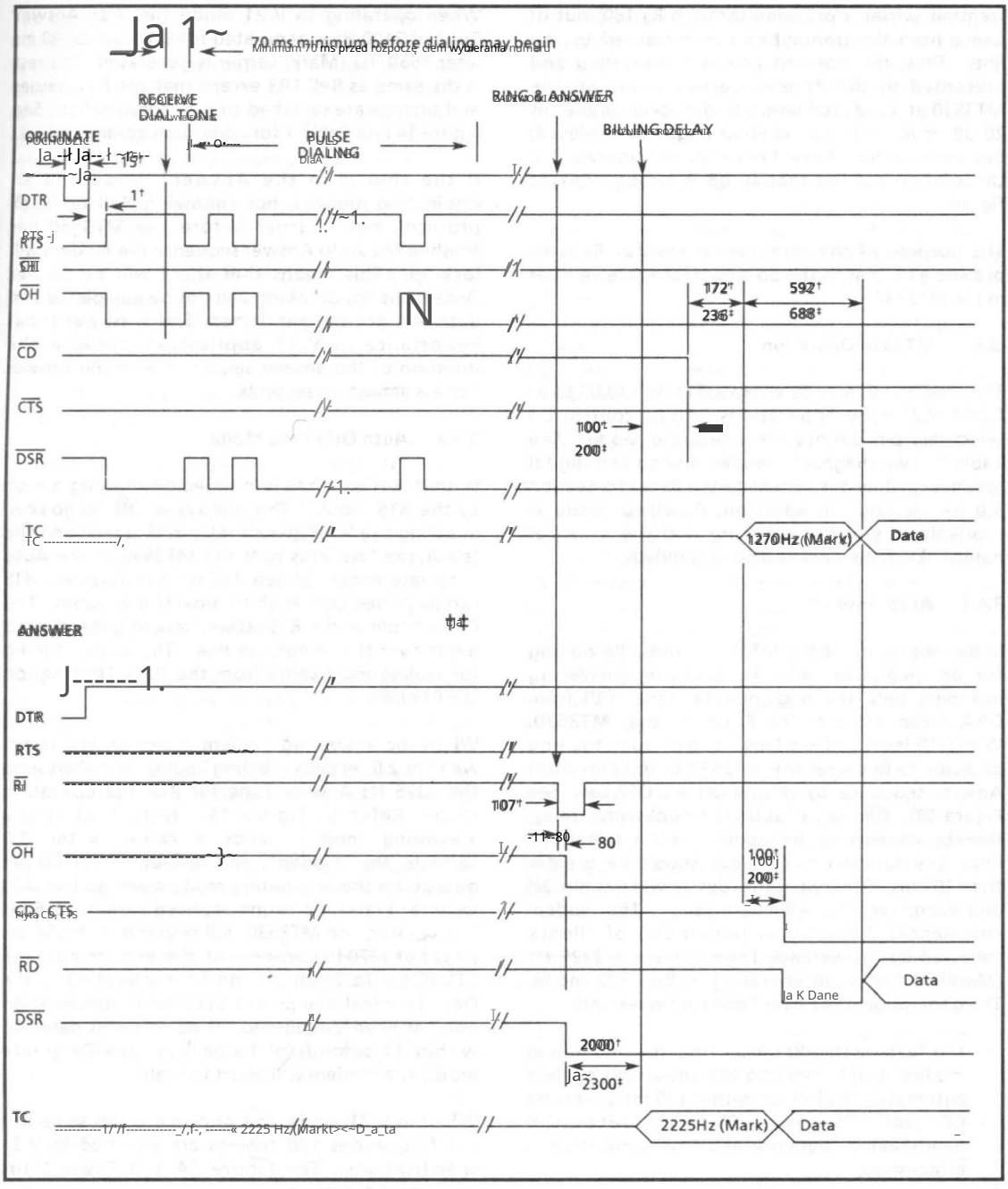

Figure 13 - MT3530 Modem Timing* Chart for Bell 103 Operating Mode

Rysunek 13 - Wykres czasowy modemu MT3530 dla trybu pracy Bell 103

* All timing is in milliseconds and the value is typical unless specified.
Czas mierzony jest w milisekundach, a wartość tajest typowa, chyba że podano inaczej.
† Denotes the minimum value.
Oznacza minimalną wartość.
‡ Denotes the maximum value.
Oznacza maksymalną wartość.

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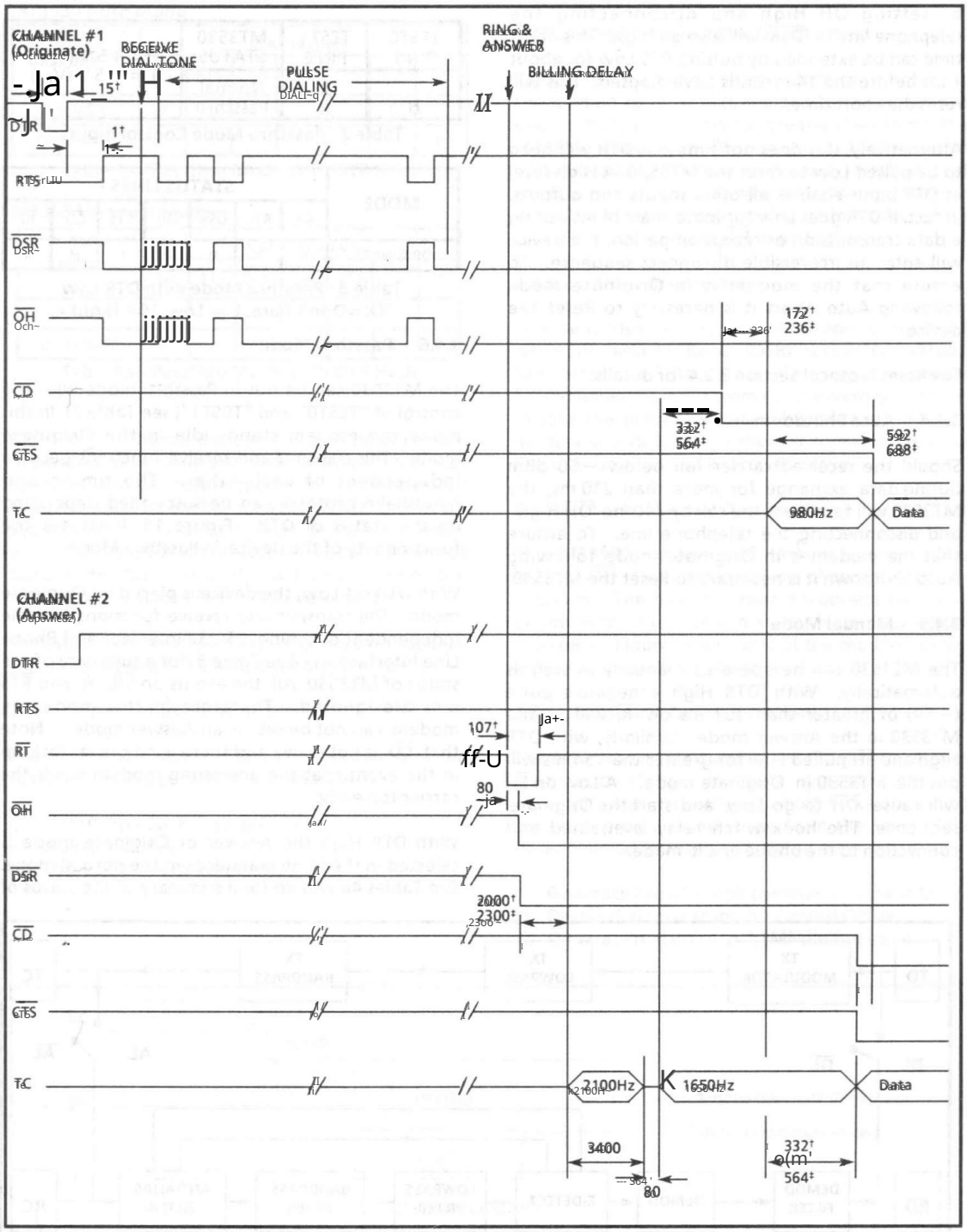

Figure 14 – MT3530 Modem Timing* Chart for CCITT V.21 Operating Mode

Rysunek 14 – Wykres synchronizacji modemu MT3530 dla trybu pracy CCITT V.21

* All timing is in milliseconds and the value is typical unless specified.

* Wszystkie czasy podawane są w milisekundach i są to wartości typowe, chyba że podano inaczej.

† Denotes the minimum value.

‡ Denotes the maximum value.

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by setting $\overline{OH}$ High and disconnecting the telephone line. $\overline{DSR}$ will also go High. This abort time can be extended by pulsing $\overline{RTS}$ Low for about 1 ms before the 14 seconds have elapsed. This will reset the abort timer.

Alternatively, if it does not time out DTR will need to be pulled Low to reset the MT3530. A High level at DTR input enables all other inputs and outputs. In fact, if DTR goes Low for more than 14 ms during a data transmission or reception period the device will enter an irreversible disconnect sequence. To ensure that the modem is in Originate mode following Auto Abort it is necessary to Reset the device.

See Reset Protocol Section 3.2.4 for details.

3.4.4 Auto Shutdown

Should the received carrier fall below -50 dBm during data exchange for more than 210 ms, the MT3530 will terminate the call by setting $\overline{OH}$ High and disconnecting the telephone line. To ensure that the modem is in Originate mode following Auto Shutdown it is necessary to Reset the MT3530.

3.4.5 Manual Mode

The MT3530 can be operated manually as well as automatically. With DTR High a negative pulse (-5V) of greater than 107 ms on $\overline{RI}$ will put the MT3530 in the Answer mode. Similarly, with DTR High and $\overline{SH}$ pulled Low for greater than 54 ms will put the MT3530 in Originate mode. A Low on $\overline{SH}$ will cause $\overline{OH}$ to go Low and start the Originate sequence. The hookswitch relay is enabled and connection to the phone line is made.

TEST0 PIN 7	TEST1 PIN 6	MT3530 STATUS	H = +5 V (V_{DD}) L = -5V (V_{EE})
L	L	Normal	
H	L	Passthru	

Table 2 - Passthru Mode Control Inputs

MODE	STATUS LINES †						
	$\overline{SH}$	$\overline{RTS}$	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ORIGINATE	X	X	H	H	L	H	X

Table 3 - Passthru Mode with DTR Low
†(X = Don't Care, L = Low, H = High)

3.4.6 Passthru Mode

The MT3530 can be put in Passthru mode with the control of "TEST0" and "TEST1" (see Table 2). In this mode the modem stands idle in the Originate mode. The transmit and receive functions become independent of each other. The timing and handshake protocol can be suspended depending on the status of DTR. Figure 15 illustrates the functionality of the device in Passthru Mode.

With DTR set Low, the device is placed in Originate mode. The transmit and receive functions become independent of timing, RS-232 Interface and Phone Line Interface. See Table 3 for summary of the status of MT3530. All the events on $\overline{SH}$, $\overline{RI}$ and $\overline{RTS}$ pins are ignored. Therefore in this mode the modem can not be set in an Answer mode. Note that $\overline{CD}$ is not active and there is no carrier lock-up in the event that the answering modem sends the carrier too early.

With DTR High the Answer or Originate mode is selected in the same manner as in the normal mode. See Tables 4a and 4b for a summary of the status of

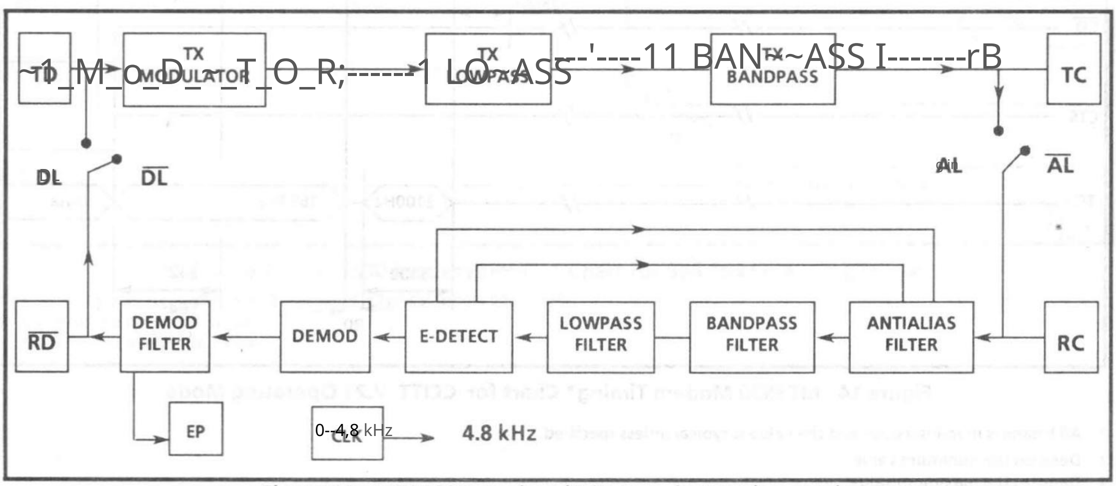

Figure 15 - MT3530 Functional Diagram in Passthru Mode

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MT3530 Auto Mode

MODE	STATUS LINES †						
	$\overline{SH}$	$\overline{RTS}$	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ANSWER	H	L	L	L	L	L	L
ORIGINATE	H	H	L	L	L	L	H

Table 4a - Passthru Mode with DTR High

MT3530 Manual Mode

MODE	STATUS LINES †						
	$\overline{SH}$	$\overline{RTS}$	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ANSWER	H	L	L	L	L	L	L
ORIGINATE	L	L	L	L	L	L	H

Table 4b - Passthru Mode with DTR High

†(L = Low, H = High)

MT3530. The transmit and receive functions are dependent on timing and handshake protocol. $\overline{CD}$ operates as in the normal mode. It should be noted that if a Space is sent before a Mark $\overline{CD}$ will not be active until it sees a Mark first. In Passthru mode with DTR High Auto Shutdown applies where as Auto Abort does not apply. After call termination the modem is placed in the Originate mode.

In Passthru mode the analog and digital loopback functions are available as in the normal mode.

3.4.7 Call Termination Procedures

The MT3530 modem offers the following three features which permits call termination:

i) Data Terminal Ready not active
ii) Abort Disconnect
iii) Loss of Carrier Disconnect

3.4.7.1 Data Terminal Ready not active

The DTR signal must be High (active) in order for the modem to remain connected to the telephone line. If DTR is set Low for greater than 15 ms, the MT3530 resets and $\overline{OH}$ pin goes High. This disconnect procedure is the only method that the DTE has of terminating a call. The exception is when the modem is in Auto Originate mode. In this case RTS Low will cause $\overline{OH}$ to go High.

3.4.7.2 Abort Disconnect

This sequence is not an option and is employed when the Data Set Ready ($\overline{DSR}$) is Low (activated). See Section 3.4.3 for details. This sequence should be implemented on automatic answering modems in case the modem is called by mistake, i.e., the modem will not stay connected to the telephone line in anticipation of a received carrier.

3.4.7.3 Loss of Carrier Disconnect

The MT3530 modem will terminate the call by setting $\overline{OH}$ High when a loss of carrier energy is detected. The loss of carrier disconnect sequence begins when the received signal level goes below −50 dBm. Figure 16 shows the modem carrier loss disconnect timing diagram.

3.5 Automatic Calling Functions

The MT3530 can be used in systems which require automatic calling. In these systems calls are generated automatically by a host processor which has been programmed to perform the tasks. The steps involved in automatic calling are:

i) Generate the off hook command to the DAA
ii) Detect dial tone from the Central Office
iii) Generate dial pulse or DTMF dialing tones

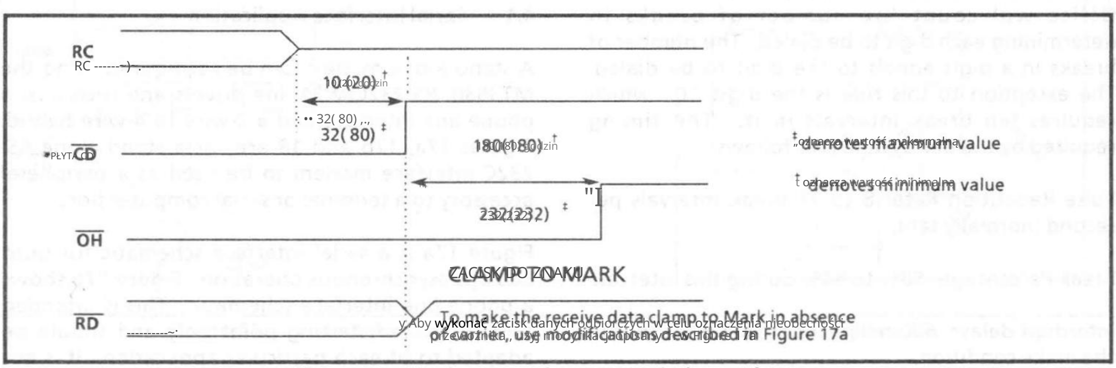

Figure 16 - Carrier Loss Disconnect Timing Diagram

*Bell 103 (CCITT V.21) times in milliseconds

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iv) Wykryj zdalny modem Answer Tone
v) Transmisja danych

3.5.1 Generowanie odłożenia słuchawki

W systemach automatycznego wywoływania połączenie z linią telefoniczną jest zazwyczaj sterowane za pomocą przewodu przekaźnika odłożonego z słuchawką podniesioną do góry. Przy stanie wysokim DTR i przyłożeniu stanu wysokiego do wejścia RTS, pin OH 24 przejdzie w stan niski. Włącza to przekaźnik hook-switch między linią telefoniczną . To przełącza MT3530 w tryb Auto Originate.

3.5.2 Wykrywanie tonu wybierania

Po podniesieniu słuchawki CO poda abonentowi sygnał wybierania . W nowoczesnych biurach centralnych , które akceptują wybieranie DTMF, CO poda „precyzyjny" sygnał wybierania, który jest kompozytem 350 i 440 Hz. W starszych biurach centralnych, które nie akceptują wybierania DTMF, trudno jest dokładnie przewidzieć , jak będzie wyglądało widmo czę stotliwości sygnału wybierania. Nominalnie mieści się ono w zakresie od 300 do 700 Hz. Wymagany jest układ scalony Call Progress Detection.

Zakłada się , że jeśli wykonywane są funkcje automatycznego wywoływania , w systemie znajduje się procesor hosta, który może zapewnić kontrolę. Po wykryciu tonu wybierania przez procesor hosta, wybieranie numeru może się rozpocząć.

3.5.3 Wybieranie impulsowe

Wybieranie impulsowe to proces otwierania (rozłączania) i zamykania (tworzenia połączenia) pętli. W MT3530 odbywa się to poprzez pulsowanie RTS Low/High w celu zapewnienia impulsów wybierania. OH bę dzie podążał za impulsami RTS . Właściwy czas wybierania musi pochodzić z Data Terminal lub Host Processor na linii RTS.

Jeśli tworzenie i zrywanie pętli jest zgodne z wymaganiami określonymi przez Bell System, Central Office policzy liczbę przerw, przy określaniu każdej cyfry, która ma zostać wybrana. Liczba przerw w cyfrze jest równa cyfrze , która ma zostać wybrana. Wyjątkiem od tej reguły jest cyfra „0", która wymaga dziesię ciu przerw. Czas wymagany przez Bell System jest nastę pujący :

Czę stotliwość powtarzania impulsów - od 8 do 11 przerw na sekundę (zwykle dziesięć);

Procent przełamania: 58% do 64% w tym przedziale;

Opóźnienie mię dzycyfrowe - od 600 milisekund do 3,0 sekund w warunku make .

3.5.4 Wybieranie DTMF

Najprostszym sposobem generowania tonów DTMF jest użycie układu scalonego generatora tonów DTMF.

3.5.5 Wykrywanie tonu odpowiedzi

Po wybraniu przez procesor hosta żądanego numeru, może nastąpić szereg zdarzeń. Zakładając, że połączenie zostanie zrealizowane, zdalny modem (odpowiadający) przekaże sygnał odpowiedzi do modemu wywołującego (pierwotnego). Gdy sygnał odpowiedzi zostanie wykryty przez MT3530, wyjście pinu CD przejdzie w stan niski. W trybie Bell 103 sygnał odpowiedzi to nośna 2225 Hz (Mark). Spowoduje to ustawienie wyjścia pinu RD MT3530 w stan wysoki. Po sygnale odpowiedzi 2100 Hz nastę puje nośna 1650 Hz . Spowoduje to przejście wyjścia pinu CD w stan niski, a pinu RD w stan niski. Po wykryciu sygnału odpowiedzi modem wywołujący odpowiada nośną nadawczą. Jest to nośna 1270 Hz (Mark) dla operacji Bell 103 i nośna 980 Hz (Mark) dla operacji V.21. Wymiana danych może rozpocząć się po wykryciu sygnału odpowiedzi przez modem dalekiego końca (odpowiadający). Szczegóły dotyczące czasu przedstawiono na rysunkach 13 i 14.

Jeśli ton odpowiedzi nie zostanie wykryty przez MT3530 po upływie określonego przez użytkownika czasu, procesor hosta może spróbować ponownie wykonać kalibrację później. Więcej szczegółów w sekcji 3.4.3.

4.0 Konfiguracje systemu modemu MT3530

MT3530 można podłączyć do równoległych lub szeregowych portów I/O standardowego sprzętu terminala danych. Połączenie z inteligentnym terminalem lub szeregowym portem komputera odbywa się wyłącznie przy użyciu odbiorników i sterowników linii. Do podłączenia systemu modemu MT3530 do równoległej magistrali mikrokomputera wymagany jest Asynchronous Communications Interface Adapter (ACIA).

4.1 Aplikacja interfejsu szeregowego

Samodzielny modem można skonfigurować przy użyciu MT3530, sterowników i odbiorników linii RS-232C/V.24 , interfejsu linii telefonicznej oraz hybrydy 2- i 4-żyłowej. Rysunki 17a, 17b i 18 przedstawiają samodzielny modem interfejsu RS-232C, który ma służyć jako urządzenie peryferyjne do terminala lub portu szeregowego komputera.

Rysunek 17a przedstawia schemat interfejsu szeregowego dla asynchronicznej pracy do 300 bps. Rysunek 17b przedstawia schemat interfejsu linii telefonicznej. Jest to jedynie sugerowany punkt wyjścia należy go dostosować do każdej konkretnej aplikacji . Nie jest zatwierdzony przez FCC Part 68.

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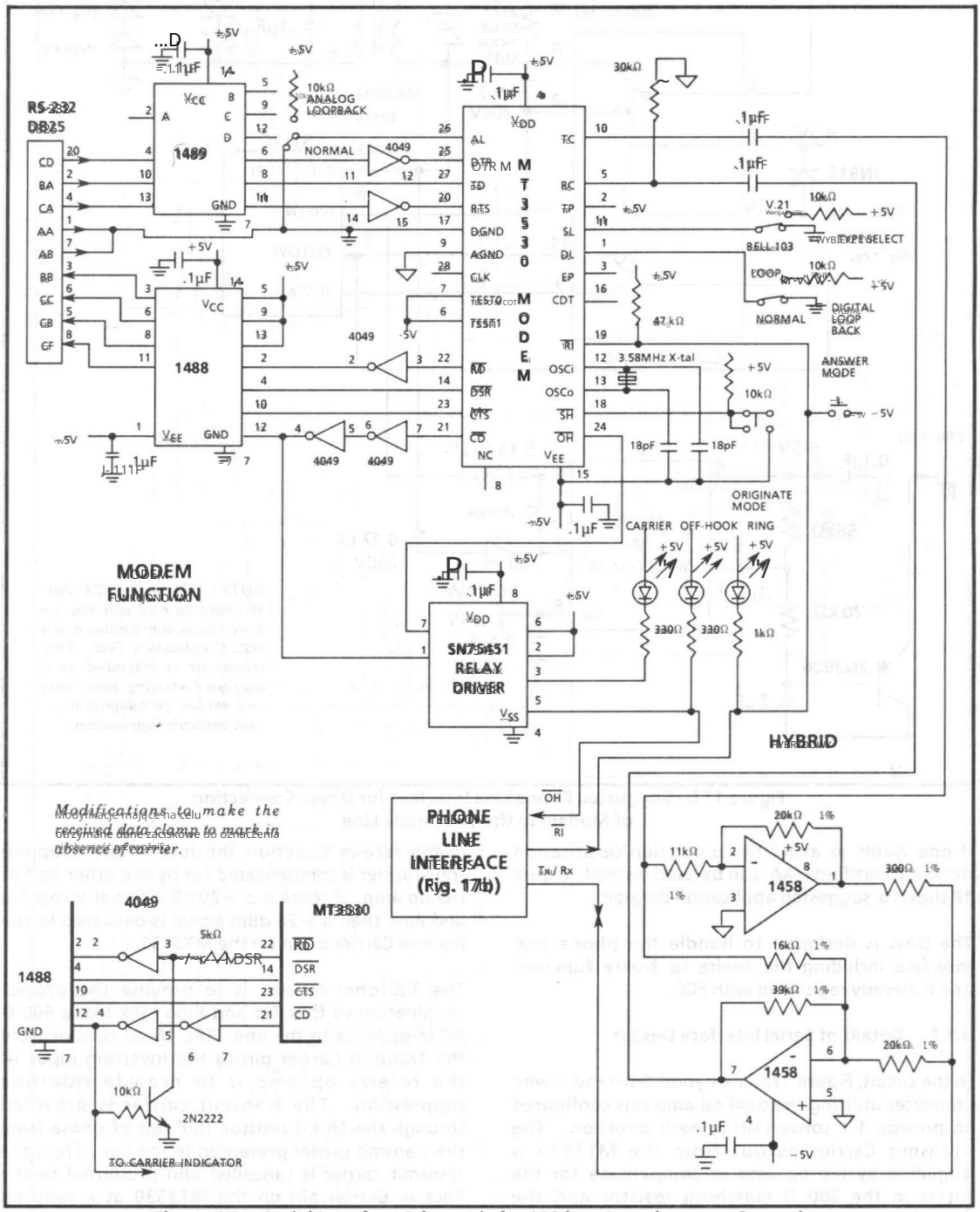

Modifications to make the received data clamp to mark in absence of carrier.

Figure 17a. Serial Interface Schematic for 300 bps Asynchronous Operation

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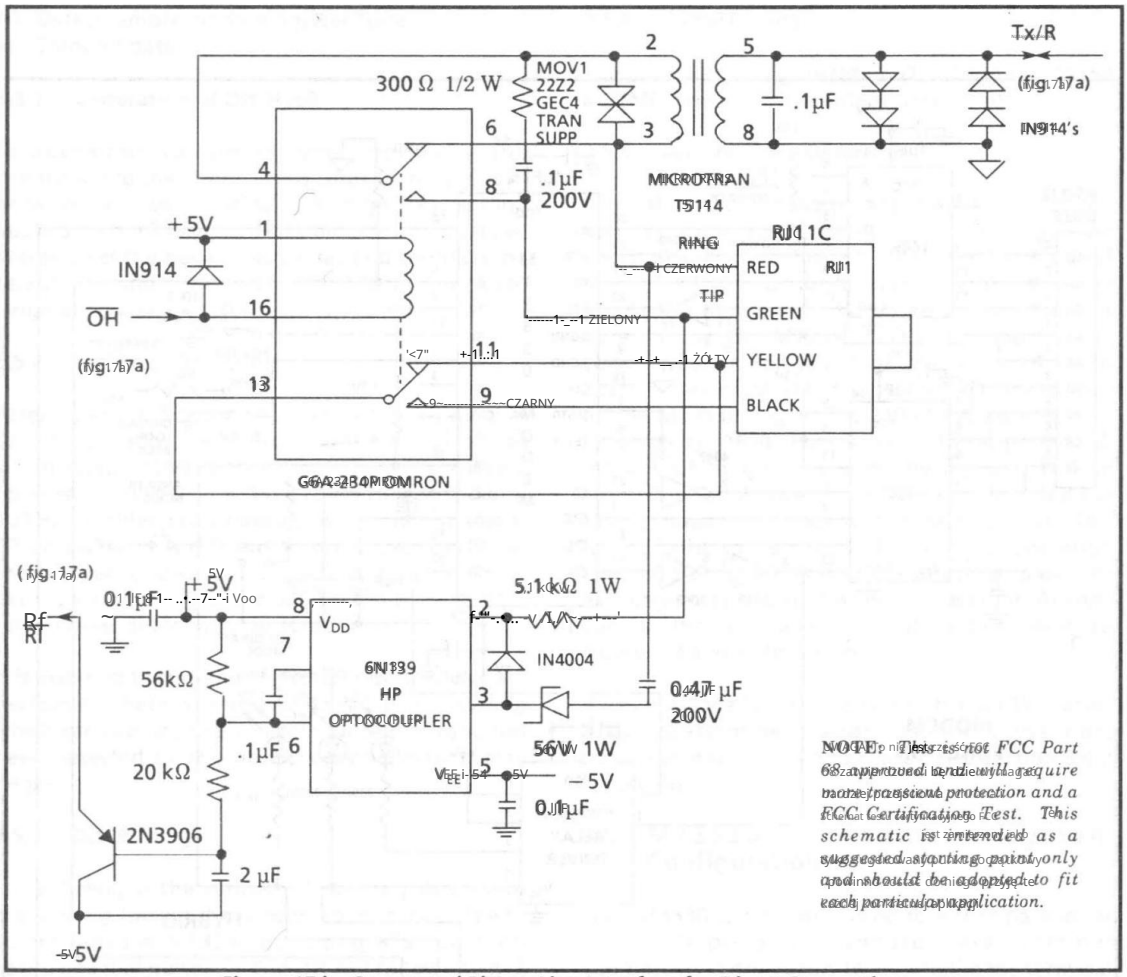

Figure 17b. Suggested Phone Line Interface for Direct Connection of Modem to the Telephone Line

If one wants to avoid the protection/certification details a certified DAA can be used instead. Figure 18 shows a suggested application diagram.

The DAA is designed to handle the phone line interface including the 4 wire to 2-wire function and is already registered with FCC.

4.1.1 Details of Serial Interface Design

In the circuit Figure 17a, the hybrid 4 wire to 2 wire converter utilizing the dual op amps is configured to provide 1:1 conversion in each direction. The Transmit Carrier output from the MT3530 is amplified by the op amp to compensate for the losses in the 300 Ω matching resistor and the coupling transformer. Transmit carrier is detected to within -9 dBm. For CCITT applications this should be reduced to − 13 dBm.

In the receive direction, the loss in the coupling transformer is compensated for by the other half of the op amp. If there is a − 20 dBm signal across Tip and Ring then a − 20 dBm signal is delivered to the Receive Carrier input on the MT3530.

The 300 ohm resistor is to provide the proper termination so that Tip and Ring look like a 600 Ω AC impedance to the line. The 16 kΩ resistor from the Transmit Carrier output to the inverting input of the op amp is to provide sidetone suppression. The transmit carrier is provided through the 16 kΩ resistor 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Receive Carrier pin on the MT3530 at a reduced level.

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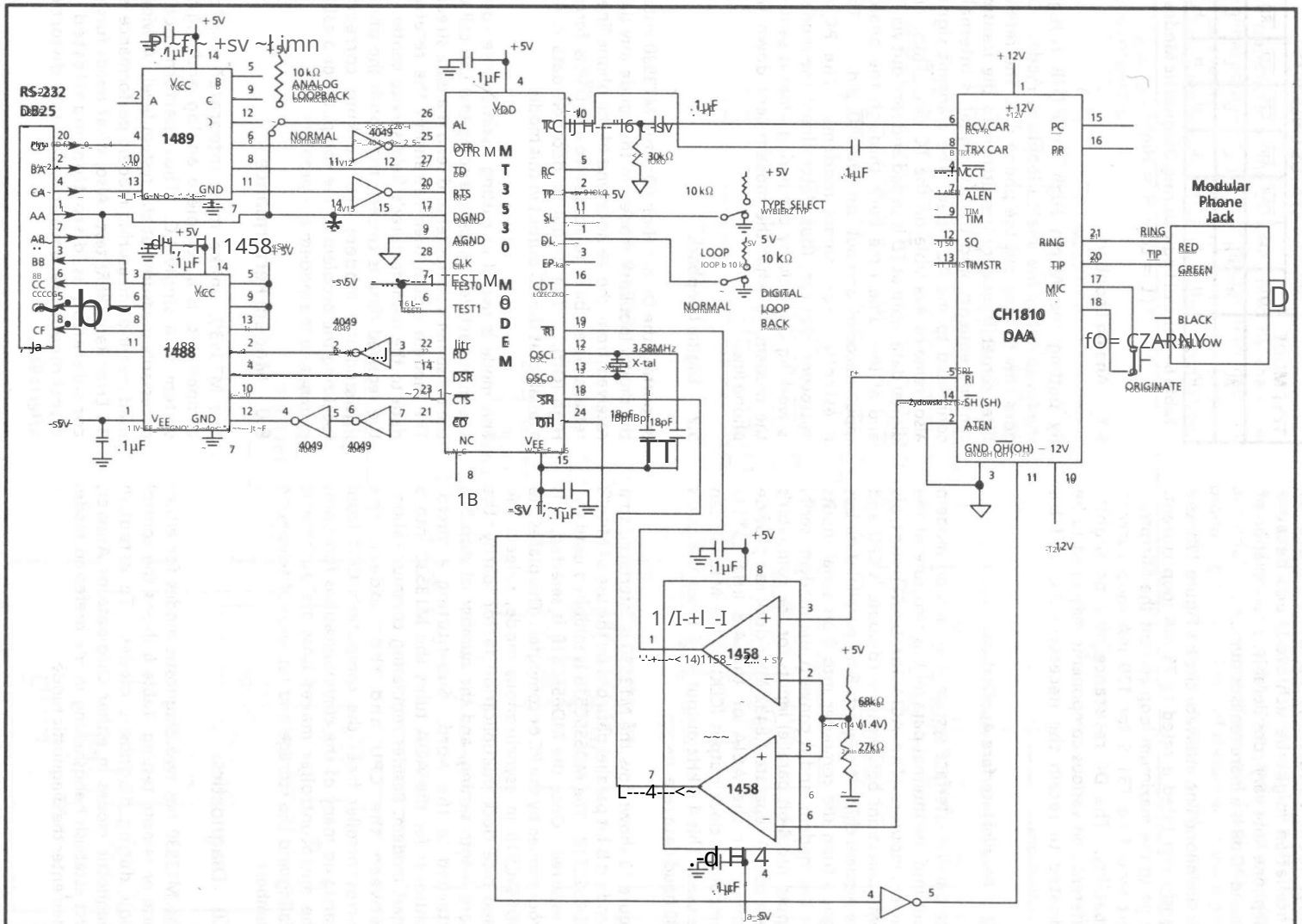

Figure 18. Suggested Application Schematic Using Part 68 Certified DAA

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W idealnych warunkach można by osiągnąć tłumienie rzędu 20 dB lub większe, ale ze względu na znaczną zmienność linii telefonicznych, bardziej realistyczna jest wartość tłumienia rzędu 10 dB.

W przypadku obwodu interfejsu linii telefonicznej, przedstawionego na rysunku 17b, transformator wymieniony w tabeli jest przeznaczony do prądu pętli o natężeniu 75 mA. Aby osiągnąć maksymalny prąd pętli, częścią Microtran będzie T5115 dla możliwości prądu pętli 120 mA. Rezystancja DC może być nieznacznie inna, a różne komponenty mogą wymagać dostosowania, aby zachować niezbędne specyfikacje AC i DC.

4.2 Aplikacja interfejsu równoległego

System interfejsu równoległego to dodatkowy modem wbudowany w wewnętrzną strukturę magistrali równoległej mikrokomputera. ACIA (lub UART) kontroluje komunikację między CPU komputera a chipem modemu. Konwertuje 8-bitowe sygnały magistrali danych równoległych z komputera na 8-bitowe wejścia szeregowe dla modemu i konwertuje wejścia szeregowe modemu na 8-bitowe wejścia równoległe dla magistrali danych komputera. Oddzielny zegar 1,8432 MHz może zapewnić taktowanie dla ACIA lub można użyć wyjścia zegara zgodnego z LSTTL 4,8 kHz (CLK) MT3530. To wyjście 4,8 kHz jest 16 razy szybsze od szybkości transmisji danych 300 bodów chipa.

Rysunek 19 pokazuje, jak MT3530 jest podłączony do standardowej 8-bitowej równoległej magistrali danych za pomocą MD65SC51B firmy Mitel. MD65SC51B jest blokowany do momentu potwierdzenia CS1. Po wybraniu MD65SC51B jest on programowany przez PC lub komputer. Ustawia to MD65SC51B w trybie asynchronicznym, wybiera współczynnik mnożenia zegara szybkości transmisji, parzystość, ustawienie długości słowa i liczbę bitów stopu dołączonych do słowa. Zastąpienie ACIA mikrokontrolerem zmienia MT3530 w inteligentny modem. Oprócz regulowania komunikacji między CPU a modemem, mikrokontroler zwalnia CPU komputera z zarządzania wieloma funkcjami komunikacyjnymi. Mikrokontroler umożliwia automatyczne wybieranie numerów oraz zapisywanie i wyszukiwanie numerów telefonicznych.

5.0 Diagnostyka

MT3530 ma dwa tryby diagnostyczne do testowania lokalnego lub zdalnego. Tabela 6 przedstawia logikę sterowania w trybach diagnostycznych. Aby ustanowić tryby diagnostyczne w trybie Originate lub Answer, najpierw ustanowić uzgadnianie w preferowanym trybie, a następnie przejść do trybu diagnostycznego.

TRYB TESTOWY	STATUS LINII †						
	DTR	RTS	DSR	OH	CTS	CD	RD
AL	H	H	L	L	L	L	L
DL	H	H	H	L	H	H	H

Tabela 6 – Logika sterowania w trybach diagnostycznych † (L = niski, H = wysoki)

5.1 Pętla analogowa

Po ustawieniu pinu AL w stan wysoki, podczas gdy DTR jest w stanie wysokim, urządzenie przechodzi w tryb pętli analogowej. OH przechodzi w stan niski, aby zajęta została linia telefoniczna. Środkowa częstotliwość filtra odbiorczego jest przełączana na środkową częstotliwość nadawczą, a sygnał TC jest wewnętrznie podłączony do wejścia RC. Sygnał nadawczy również pozostaje dostępny na pinie TC. W ten sposób wszelkie dane cyfrowe wprowadzane w TD są kodowane i wysyłane przez TC, a jednocześnie z powrotem przez wejście analogowe, dekodowane i wyprowadzane na pinie RD. Jest to niezbędne w przypadku inteligentnych modemów. Komputer lub mikrokontroler może zatem określić, czy modem działa prawidłowo, porównując to, co jest wysyłane do modemu, z tym, co modem wysyła linią telefoniczną.

5.2 Pętla cyfrowa

Po ustawieniu pinu DL na High (On) MT3530 przechodzi w tryb cyfrowej pętli zwrotnej. W tym trybie wszelkie dane odebrane ze zdalnego końca linii telefonicznej są retransmitowane z powrotem do źródła, a DSR jest wymuszany do High (Off). Cyfrowe lub zdekodowane dane nie są dostępne na wyjściu RD w tym trybie.

Tryb ten jest przydatny w obniżaniu kosztów konserwacji. Producent (lub firma serwisowa) może skalibrować komputer użytkownika i wysłać do niego strumień danych. Następnie modem ponownie prześle otrzymane dane do centrum serwisowego producenta. Jeśli otrzymane dane są poprawne, to zarówno linia telefoniczna, jak i modem działają prawidłowo, lokalizując problem w komputerze lub kablu, eliminując modem jako problem.

6.0 Wydajność modemu

MT3530, w przeciwieństwie do większości zintegrowanych komponentów modemu, jest kompletnym systemem analogowym i cyfrowym w jednym IC. Dlatego wydajność jest koniecznie mierzona na poziomie systemu. Szeroko stosowanym sposobem pomiaru wydajności modemu jest test współczynnika błędów bitowych (BER). Ponadto, co wymaga dalszych rozważań, przejawia się w transmisji asynchronicznej, ponieważ to zniekształcenie wpływa na BER. jest zniekształceniem

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6.1 Asynchronous Modem Distortion
6.1 Zniekształcenie modemu asynchronicznego

The transitions in the data received by the data terminal equipment (DTE, computer, terminal) will not be exactly at the points where they occurred in the original transmission. This is because modulation, network imperfections and demodulation affect the analog carrier alternately. Additionally, transitions in both the modulation and demodulation processes are not instantaneous, producing another form of distortion in the digital waveform. While this distortion is only manifested

Przejścia w danych odbieranych przez dane
sprzęt (komputer, terminal) będą
nie znajdować się dokładnie w punktach, w których miały miejsce
transmisja. To jest spowodowane modulacją,
niedoskonałości sieci i demodulacja wpływają
analogowy nośnik naprzemiennie. Dodatkowo,
przejścia
procesy demodulacji nie są natychmiastowe,
powodując inną formę zniekształcenia w cyfrowym
przebiegu. Chociaż to zniekształcenie jest tylko widoczne

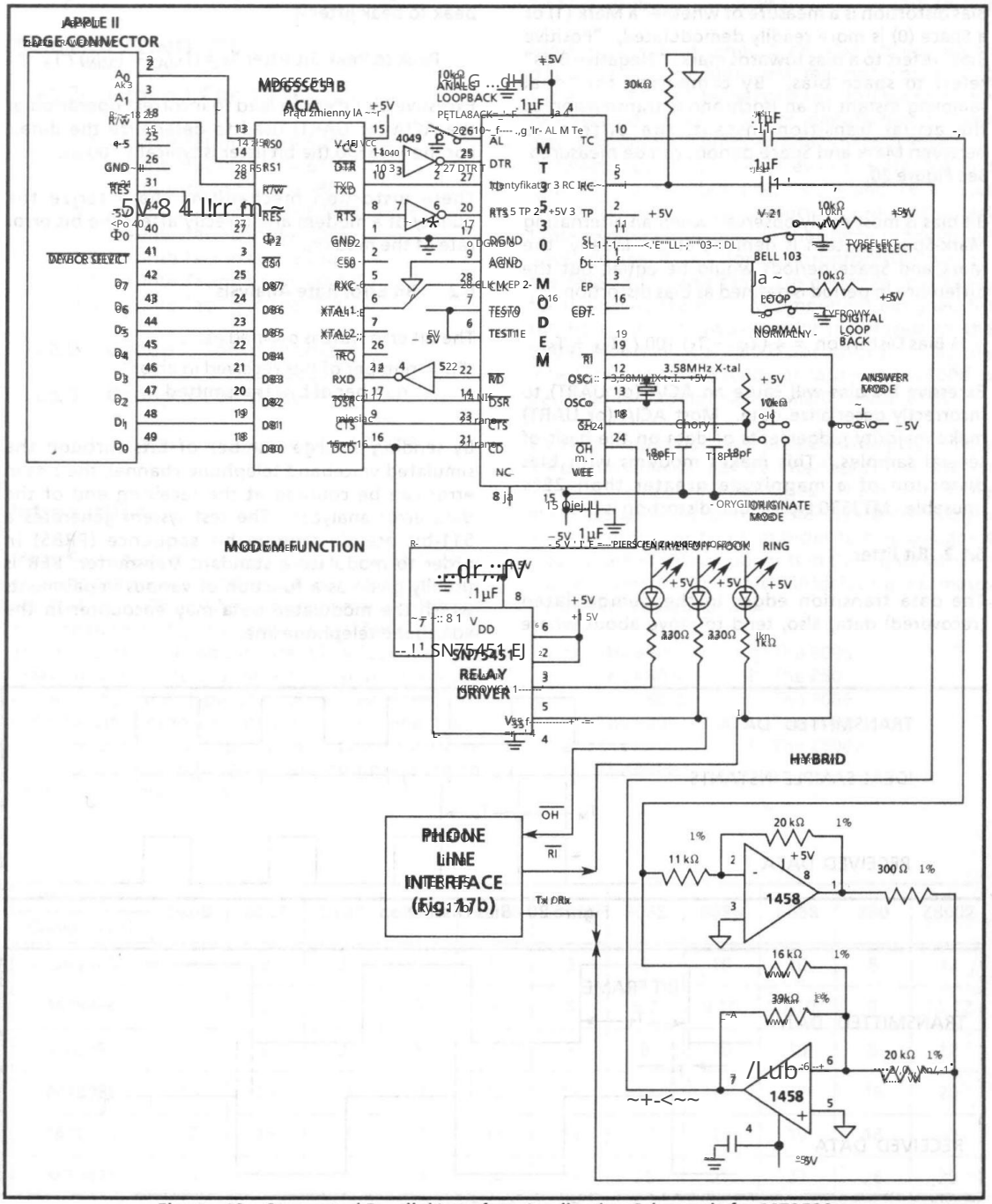

Figure 17. Suggested Parallel Interface Application Schematic for MT5530
Rysunek 17. Sugerowany schemat aplikacji interfejsu równoległego dla MT5530

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W transmisji asynchronicznej występują różne nazwy i definicje danego tego zniekształcenia cyfrowego. Dwie z najbardziej znanych form zniekształceń cyfrowych to zniekształcenia polaryzacji i drgania bitowe.

6.1.1 Dystorsja polaryzacji

Zniekształcenie polaryzacji jest miarą tego, czy Mark (1) czy Space (0) jest łatwiej demodulowany. Dodatnie obciążenie odnosi się do odchylenia w kierunku marko, a ujemne obciążenie odnosi się do odchylenia w przestrzeni. Posługując się idealną chwilą próbkowania w transmisji asynchronicznej z rzeczywistą chwilą przejścia, można zmierzyć różnicę między okresami Mark i Space. Zobacz rysunek 20.

Odchylenie można najłatwiej zaobserwować, gdy stosowany jest naprzemienny wzór Mark-Space. W idealnym przypadku okresy Mark i Space powinny być równe, ale różnica jest definiowana jako zniekształcenie polaryzacji:

$$\% \text{ Zniekształcenie polaryzacji} = \tfrac{1}{2}(T_M - T_S)\,100/(T_M + T_S)$$

Nadmierne odchylenie może spowodować, że ACIA (UART) nieprawidłowo deserializuje dane. ACIA (lub UART) dokonuje większości wyborów danych na podstawie kilku próbek. To sprawia, że modemy ze zniekształceniem odchylenia do 25% są użyteczne. Typowe zniekształcenie odchylenia MT3530 wynosi 3 %.

6.1.2 Drgania bitowe

Krawędzie przejściowe w zdemodulowanych (odzyskanych) danych również mają tendencję do przemieszczania się w kierunku, w którym powinny one idealnie być, co prowadzi do jittera bitowego. Zobacz Rysunek 21.

$$\text{Drgania bitowe} = T_{MAXIMUM} - T_{MINIMUM}$$

Wahania bitowe są zazwyczaj określane w procentach, wskazując, jaki procent ramki bitowej stanowią wahania między szczytami.

$$\text{Szczytowe drgania bitów } \% = (T_{MAX} - T_{MIN}) / T_B$$

Nadmierne drgania bitowe mogą prowadzić do nieprawidłowego działania układu ACIA (lub UART) używanego do deserializacji danych. W przypadku MT3530 jitter bitowy wynosi zazwyczaj 100 mikrosekund.

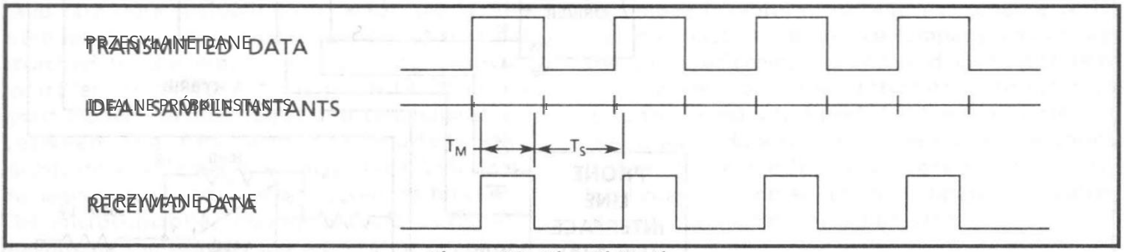
Mechanizmy zniekształceń charakteryzują jakość modemu i bezpośrednio wpływają na współczynnik błędów bitowych modemu.

6.2 Analiza współczynnika błędów bitowych

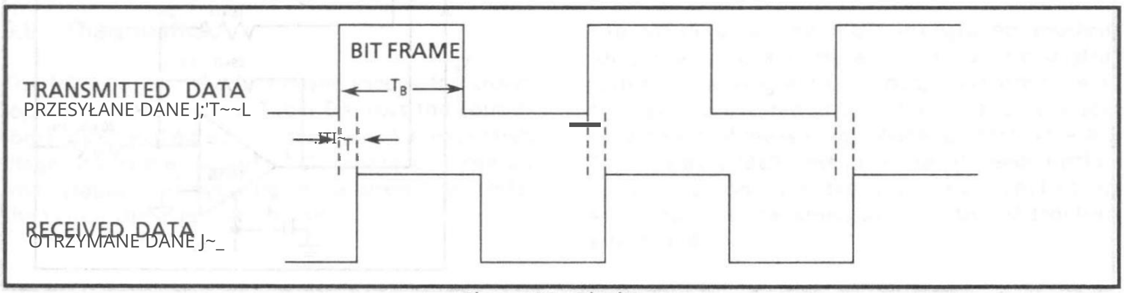
Współczynnik błędów bitowych definiuje się jako:

$$P_e = \frac{\text{liczba bitów odebranych błędnie}}{\text{liczba przesłanych bitów}}$$

Wysyłając dużą liczbę bitów przez symulowany kanał telefoniczny pasma głosowego, błędne bity mogą być zliczane na końcu odbiorczym. Analizator błędów danych testowych generuje 511-bitową pseudolosową sekwencję bitów (PRBS) w celu modulacji standardowego nadajnika. BER jest zwykle podawany jako funkcja różnych uszkodzeń, na które mogą natrafić zmodulowane dane w linii telefonicznej pasma głosowego.



Rysunek 20 - Dystorsja polaryzacji



Rysunek 21 - Drgania bitowe

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Application Note MSAN-119
How to Interface Mitel Components to Microprocessors

91G1000-028NA ISSUE 1 January 1986

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2.0 Group 2 Components

3.0 Group 3 Components

3.1 Interfacing to the 68000/10/08

Introduction

Most of Mitel Semiconductor's products have been designed around Motorola microprocessors, so extra circuitry may be needed to interface to microprocessors designed by other manufacturers. Even across Motorola's product line, there are several different bus structures (segmented primarily by data bus size, i.e., 8 and 16 bit bus structures). Mitel Semiconductor's products reflect these two bus structures, in that some products are designed specifically for a microprocessor such as the 6809 (8 bit) and some are designed specifically for the 68000 (16 bit). A component designed for the 68000 is not always easily interfaced to the 6809, however, a 6809 peripheral is easily interfaced to the 68000, because the 68000 is designed to accommodate 6802/09 peripherals.

Most Mitel Semiconductor components are designed around Motorola microprocessor architectures. This allows unique designs to be developed that interface a component directly to more than one type of microprocessor without requiring additional circuitry. The purpose of this application note is to provide assistance in interfacing Mitel components to various microprocessors.

This application note will provide examples of how Mitel components may be interfaced to several of the major microprocessor types. The intent of the examples is to categorize interface architectures by microprocessor types in order to help designers incorporate Mitel components in their systems. The microprocessors for which interfacing examples have been created for are:

a/ The 68000
b/ The 68010
c/ The 68008
d/ The 6809
e/ The 6802
f/ The 6800
g/ The 8085
h/ The Z80
i/ The 8086
j/ The 8088
k/ The Z8002

Processor / Component	6800	6802	6809	68000	68010	68008	8085	8086	8088	Z80	Z8002
MD6655C51	4	2	3	5	5	5	6	10	10	8	12
MT8880	4	2	3	5	5	5	6,7	9,10	9,10	8	11,12
MT8952	4	2	3	5	5	5	6	10	10	8	12
MT8980	15	14	13	16	16	16	17	19	19	18	20
MT8981	15	14	13	16	16	16	17	19	19	18	20
MT8920	23	22	21	24	24	24	25	27	27	26	28

Table 1 – Table of Circuits Cross Referenced by Microprocessor and Mitel Part Number

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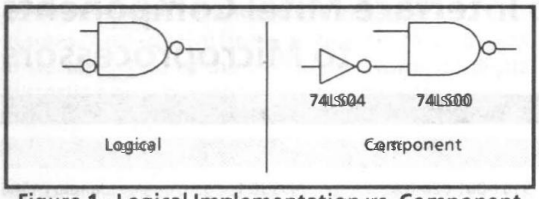

Figure 1 – Logical implementation vs. Component implementation

These microprocessors are believed to be the industry's most popular. In most cases, microprocessors not included in the list will have architectures similar to one of those mentioned.

To minimize the number of interfaces that have to be dealt with, it is possible to segment the listed microprocessors into groups. Members of a group are related by similar bus structures. The microprocessors that can be grouped together are:

a/ 6800, 6801, 6802, 6808
b/ 8085, 8086

The remaining microprocessors have subtle differences between systems that cause a need for individual interface circuits.

Grouping Mitel components on the basis of similar interfacing requirements also minimizes the total number of interface circuits. Mitel devices with similar bus architectures are grouped as follows:

Group 1

a/ MD65C51 Asynchronous Communications Interface Adapter (ACIA)
b/ MT8952 HDLC Controller
c/ MT8880 DTMF Transceiver

Group 2

a/ MT8980 Digital Switch
b/ MT8981 Digital Switch

Group 3

MT8920 ST-BUS Parallel Device (STPA)

The majority of the application note is dedicated to describing the interface circuits and explaining their operation. Each interface shall have an accompanying block diagram to enhance understanding of the circuit. To keep the interfaces independent of particular microprocessor systems, only "glue" components will be shown in the diagrams. Instead of showing commercially available components, only the logical symbol representing the desired operation shall be shown. This will leave the actual implementation to the designer (see Figure 1).

Table 1 is a directory of the schematic diagrams referenced by microprocessor and Mitel Semiconductor device part number. To find the appropriate interface circuit, select the column corresponding to the microprocessor being used, and select the row corresponding to the Mitel component being used. The figure number of the required circuit diagram(s) is indicated in the table element common to the row and the column.

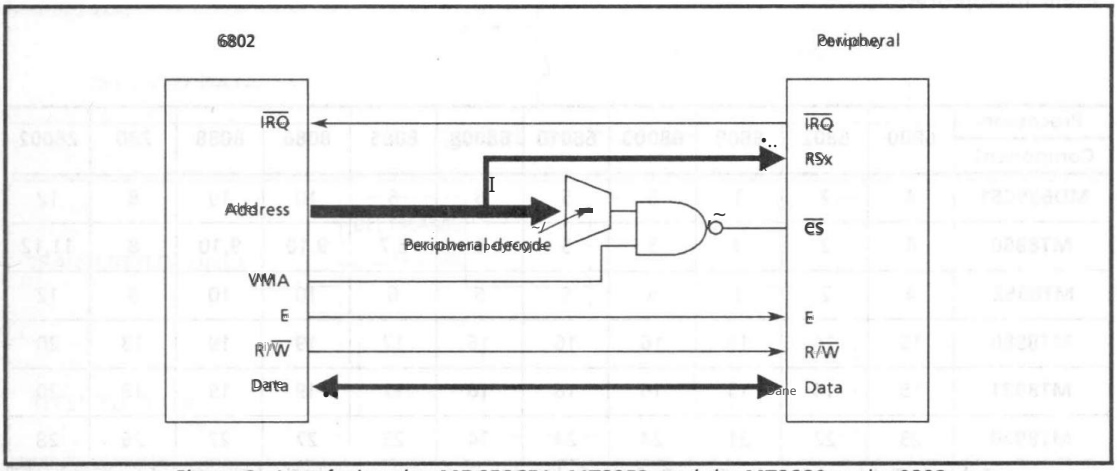

Figure 2 – Interfacing the MD65C51, MT8952 and the MT8880 to the 6802

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1.0 Group 1 Components

Group 1 consists of the MD65SC51, the MT8952 and the MT8880. All of these components have the same basic interface, but a subtle requirement causes several of the parts to use a separate and more complex circuit design (depending on the microprocessor interfaced to).

The Group 1 interface consists of:

a/ an 8 bit data port,

b/ several inputs to used for selecting internal registers (register selects),

c/ chip select input(s),

d/ a read/write control that specifies the direction of data flow (to or from the component),

e/ an enable strobe that synchronizes component timing to the microprocessor's timing,

f/ an interrupt output that is used to alert the microprocessor that a specific event has occurred at the component.

The subtle difference mentioned above divides Group 1 components into two sub-groups: those components that require a constantly active Enable clock and those components that do not. The MT8880 is the component that requires a constant clock on the E input (in some of their operating modes). This may cause a more complicated circuit design when interfacing to microprocessors that have more than one clock cycle per bus cycle, i.e., 8085, 8086, 8088, Z80 and the Z8000. When interfacing to the 6802/09, 6800, and the 68000, the circuit design is the same for both sub-groups.

1.1 Interfacing to the 6802

Interfacing Group 1 components to the 6802 is the simplest interfacing task. The 6802 has the following interface:

a/ an 8 bit data port,

b/ 16 bit address bus for addressing 64 kbytes of memory or I/O,

c/ a read/write output that specifies the direction of data flow (to or from the microprocessor),

d/ an enable strobe output that synchronizes component timing to microprocessor timing. (This signal strobes with a constant frequency unless the microprocessor is in the reset condition. Cycles may be stretched but should only be stretched for several normal E cycles. Note that because E is constant, all group 1 devices may use the same circuit when interfacing to the 6802. Also note that one bus cycle is equivalent to one E cycle.)

e/ an interrupt input that is used to alert the microprocessor that a specific event has occurred at the component.

The 6802's signals relate to Group 1 signals almost directly. The data port of the 6802 may be connected directly to the data port of any of the Group 1 components. Information is transferred between microprocessor and the component on this bus. The address bus of the microprocessor must be decoded to produce the chip select(s) needed by a component before it will participate actively on the data bus. In decode of the address bus the validity of the address bus state must be qualified by the VMA (Valid Memory Address) signal. Any of the address bits may be connected directly to the register select inputs of the component (the least significant bits are the bits most commonly used).

When the chip select is active, and the enable signal is active the data bus will be carrying either information from the microprocessor, or information from the component. The source of the information is dependent on the state of the $R/\overline{W}$ signal from the 6802. If the $R/\overline{W}$ is high (read), the selected Group 1 component will turn on its data bus drivers and the contents of the selected register will be transferred to the data bus. If the $R/\overline{W}$ signal is low (write), the Group 1 device's data port will be high impedance and the microprocessor will transfer information to the data bus. The bus cycle is terminated by the falling edge of the E clock (strobe is a more appropriate term). When a write bus cycle is ended, the Group 1 component will latch the state of the data bus into the selected register. When a read bus cycle is ended, the component holds the data bus in the same state for a short period of time (hold time) before relinquishing control of the bus. Note that some of the components "acquire" the data from the bus on the rising edge of E. Appropriate set up time before this rising edge must be observed. Set up time is applicable to control signals, data and address information.

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The interrupt output of Group 1 devices is an open drain configuration (analogous to open collector in TTL devices), therefore it must be pulled up to V_{CC} by a resistor. This output can be connected directly to the 6802 or to a priority encoder which is then connected to the 6802. Group 1 components signify the presence of an interrupt condition by pulling this line low. The microprocessor must clear this interrupt through an established procedure that is dependent on the type of component that initiated the interrupt. The resistor used to pull up any open drain outputs is not shown in any of the diagrams in this note.

Figure 2 shows the connection of data bus as a straight connection in reality there will probably be a buffer intervening to give the microprocessor more driving capability. R/$\overline{W}$ and E are also shown to be a straight connection. These signals are also usually buffered. In further figures, details such as buffers will be omitted as they are dependent on the design of the target system.

The address bits are shown connected to a box labelled "peripheral decode". This can refer to any circuitry that produces an active high signal when the correct address is on the bus. The active signal is 'NAND'ed with VMA to produce an active low chip select. Most Group 1 components have at least two chip select inputs usually of opposite active logical states, so the active low signal in Figure 2 could have been a high signal depending on the device

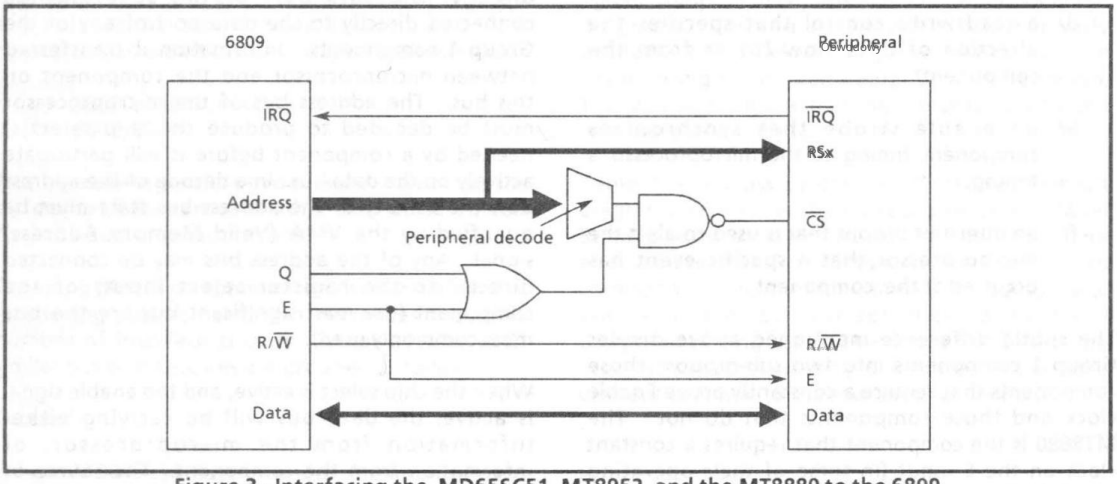

Figure 3. Interfacing the MD65SC51, MT8952, and the MT8880 to the 6809

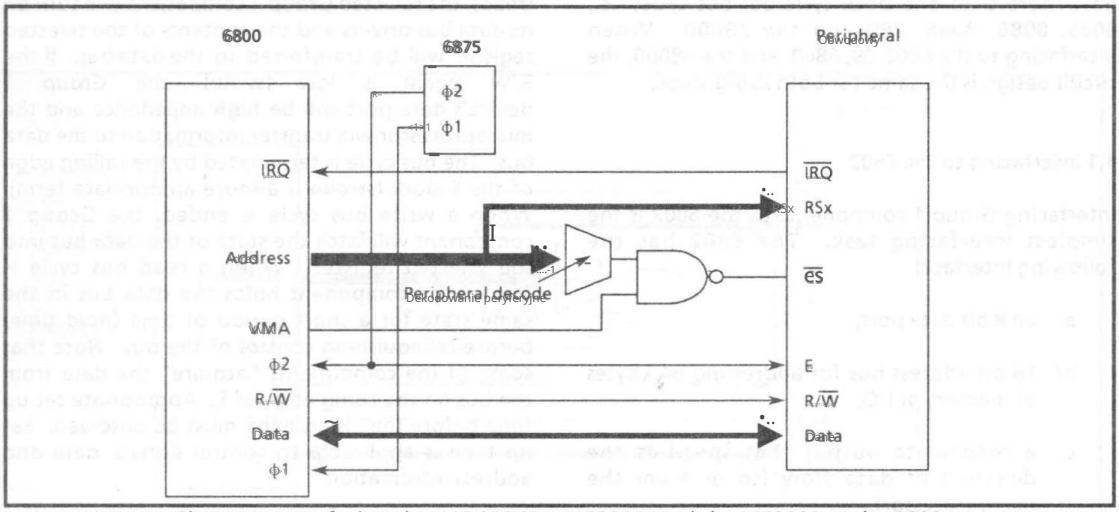

Figure 4. Interfacing the MD65SC51, MT8952, and the MT8880 to the 6800

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i użytego wyboru (pozostałe niewykorzystane chip selecty mogą być użyte do dalszego dekodowania magistrali adresowej lub mogą być powiązane z ich aktywnymi poziomami napięcia). Najważniejszym punktem sugerowanym przez obecność bramki NAND jest to, że sygnał VMA 6802 musi kwalifikować każde dekodowanie komponentów Grupy 1 (VMA mogło być powiązane z aktywnym wysokim wejściem chip select, aby zapisać zewnętrzną bramkę).

1.2 Interfejs do 6809

Układ potrzebny do połączenia 6809 z urządzeniami grupy 1 (rysunek 3) jest niemal taki sam, jak układ używany do połączenia z 6802, ze względu na podobieństwo architektur magistrali obu mikroprocesorów. Jedyną różnicą między tymi dwoma układami jest to, że 6809 nie ma sygnału VMA, więc równoważny sygnał musi zostać wygenerowany przez 'OR'owanie sygnałów E i Q układu 6809.

1.3 Interfejs do 6800

Do połączenia układu 6800 z urządzeniami Grupy 1 wymagany jest ten sam obwód, który jest używany do połączenia podzespołów Grupy 1 z układem 6802. Jedyną różnicą między obwodami jest to, że na rysunku 4 przedstawiono układ IC generatora zegara 6875 podłączony do układu 6800.

1.4 Interfejsowanie z 6800/10/08

16-bitowy mikroprocesor Motoroli 68000 wykorzystuje szeroką gamę interfejsów zaprojektowanych dla 8-bitowych mikroprocesorów tej firmy. Zwykle transfer informacji między 68000 a urządzeniem peryferyjnym odbywa się asynchronicznie, w przeciwieństwie do metody synchronicznej stosowanej przez 8-bitowe mikroprocesory (6800, 6802, 6809 itd.). 68000 można jednak zmusić do wykonania transferu synchronicznego.

Transfery synchroniczne uzyskuje się poprzez odwoływanie się wszystkich zdarzeń magistrali do krawędzi stroboskopu E. Transfery asynchroniczne obejmują uzgadnianie między 68000 a komponentem zaangażowanym w transfer danych. Gdy 68000 chce odczytać lub zapisać urządzenie, 68000 potwierdza LDS lub UDS (DS w 68008), a gdy komponent zaakceptuje dane (zapis) lub umieści prawidłowe dane na magistrali danych (odczyt), komponent potwierdza otwarty sygnał drenażowy DTACK (Data Acknowledge). Ten sygnał powoduje, że 68000 kończy cykl magistrali, usuwając sygnał stroboskopowy danych. Po negacji DS, odczyt zatrzaskuje dane w mikroprocesorze, urządzenie peryferyjne zwalnia magistralę danych i neguje DTACK. W przypadku zapisu dane są zatrzaskiwane w urządzeniu peryferyjnym, które następnie neguje DTACK.

Firma Motorola zaprojektowała mechanizm umożliwiający obsługę urządzeń peryferyjnych, które nie mają możliwości wykonywania asynchronicznego transferu danych za pomocą układu 68000. Układ 68000 dostarcza Eclock, sygnał VMA i wejście zwane VPA. Jeśli adres dostarczony przez układ 68000 (kwalifikowany przez AS) powoduje potwierdzenie sygnału VPA, układ 68000 synchronizuje transfer danych z zegarem E (szczegóły dotyczące synchronizacji znajdują się w karcie danych układu 68000).

Aby zsynchronizować, 68000 czeka, aż Eclock przejdzie w stan niski (czas Eclock nie ma związku z normalnymi cyklami magistrali 68000), następnie 68000 potwierdza VMA i kończy cykl magistrali jak 8-bitowy mikroprocesor. Sekwencja końcowa wygląda następująco: E go jest wysokie, dane są przesyłane, cykl magistrali kończy się opadającym E, VMA jest negowane, AS i stroboskopy danych są negowane).

Obsługa wyjątków w procesorze 68000 znacznie różni się od obsługi 8-bitowych procesorów. Urządzenia peryferyjne mogą odgrywać aktywną rolę w określeniu wektora wyjątku. Każdy stan na wejściach poziomu priorytetu przerwania (IPLO-2) inny niż wszystkie jedynki (poziom 0) oznacza przerwanie. Jeśli przerwanie jest oznaczone, stan wejść IPLO-2 koduje poziom priorytetu przerwania. Informacje zakodowane na tych wejściach są odwracane w procesorze 68000, aby reprezentować poziom priorytetu na 3-bitowej masce przerwania w wewnętrznym rejestrze stanu.

Gdy instrukcja wykonywana w momencie przerwania zostanie zakończona, 68000 wykonuje cykl potwierdzenia przerwania. Podczas cyklu potwierdzenia przerwania 20 najbardziej znaczących bitów adresu jest ustawianych na wysoki, trzy najmniej znaczące bity odzwierciedlają poziom przerwania, a wszystkie piny FCO-2 w 68000 są ustawione (rzeczywisty wskaźnik, że cykl potwierdzenia przerwania występuje). AS jest potwierdzany, a następnie LDS jest potwierdzany (wektor przerwania może być przesłany tylko na dolnej połowie magistrali danych w 68000). Pin R/W będzie wysoki, ponieważ 68000 oczekuje, że urządzenie peryferyjne umieści informacje wektorowe na magistrali danych, tak jakby 68000 odczytywał jeden z wewnętrznych rejestrów urządzenia peryferyjnego. Urządzenie peryferyjne zaprojektowane dla 68000 zakończy uzgadnianie z wymaganymi danymi i zwróci DTACK tak jak normalna wymiana.

Komponenty grupy 1 nie mają powyższej możliwości zapewnienia układowi 68000 wektora przerwań, tak samo jak nie mogą wykonywać transferu asynchronicznego. Jednakże Motorola przewidziała 6800 urządzeń peryferyjnych w przetwarzaniu wyjątków 68000, tak jak przewidziano transfery danych za pomocą urządzeń peryferyjnych 6800. Jeśli informacje dostarczane przez 68000 w celu wskazania cyklu potwierdzenia przerwania i poziomu przerwania mogą spowodować, że VPA

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be asserted, the 68000 will automatically fetch an exception vector at an address determined by the level of the interrupt (Motorola calls this autovectoring). There are seven autovector locations (7 interrupt priority levels) and they are located at addresses 000064$_H$ to 00007C$_H$.

The circuit to interface Group 1 components to the 68000 (Figure 5) must be able to assert VPA not only when the component is directly addressed but also when the 68000 is indicating that the component was the source of the interrupt. Figure 5 shows a block symbol to represent the decode of a group 1 device. The input of this block is the address bus and AS, the output is a signal that has two destinations: the in put to the circuit that asserts VPA and the input to the circuit that asserts the group 1 components chip select.

To select the component for data transfer, the output of the peripheral decode circuitry is further decoded by VMA. To generate VPA, the peripheral decode ouput is 'NOR'ed with an interrupt acknowledge (IACK) signal. The IACK signal is formed by 'AND'ing the FC0-2 outputs, asserting AS, and placing the correct priority level information on the 3 least significant address pins. All this information is 'AND'ed to produce IACK. Figure 5 shows a possible interrupt encoding scheme implemented with the Group 1 component's IRQ line driving a 74LS348 eight to three encoder. The 74LS348 in turn drives the IPL inputs (remember that the logic level is inverted to form the internal priority level).

The remaining signals that Group 1 components require are derived in a more standard manner. R/W from the 68000 can be connected directly to the component as can E and one half of the 16 bit data bus (the component will be found at either odd or even addresses from the base address). The 68008 has only two interrupt inputs with IPL0/IPL2 being functionally equivalent to tying IPL0 and IPL2 together on the 68000 (only priority levels 0, 2, 5 and 7 are available on the 68008).

1.5 Interfacing to the 8085

There are two circuits needed to interface group 1 components to the 8085, depending on the requirement for a continuous E clock on the MT8880. The circuit in Figure 6 assumes that the application can accommodate the lack of a continuous E clock; in some applications the MT8880 can do so.

The circuit is different from the interface to the Motorola 8 bit microprocessors in many respects. The first difference is that the 8085 has a multiplexed address/data bus, the Motorola parts do not. The first step in decoding an address

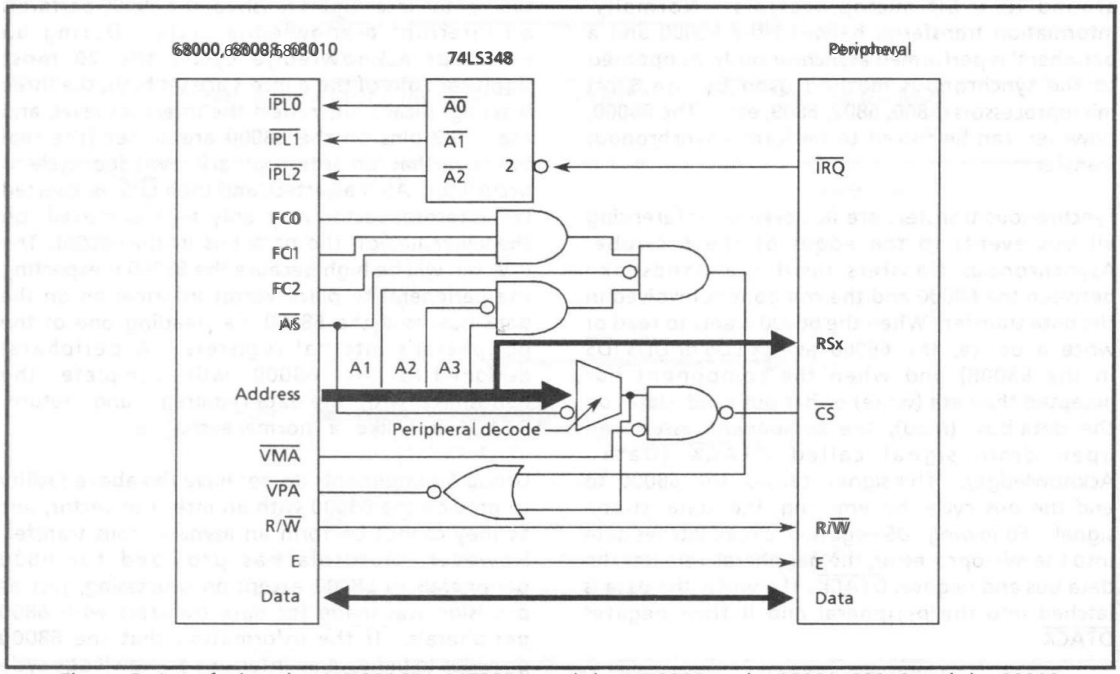

Figure 5 - Interfacing the MD65SC51, MT8952, and the MT8880 to the 68000, 68010 and the 68008

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generated by the 8085 is to demultiplex the least significant half of the address from the data. Intel provides a latch, the 8212, that does this. It is strobed by the ALE (Address Latch Enable) signal from the 8085, when the address is present on the bus. The demultiplexed address may then be decoded as in the Motorola system.

The second difference is that rather than using the combination of a R/$\overline{W}$ direction pin and an E strobe, the 8085 uses a $\overline{Read}$ strobe and a $\overline{Write}$ strobe. When either of these strobes are active, the active period is equivalent to the period in a Motorola bus cycle where the E strobe is active. The direction of the data transfer is determined by which strobe, $\overline{RD}$ or $\overline{WR}$, is present. For correct operation of Group 1 components, R/$\overline{W}$ and E must be generated from $\overline{RD}$ and $\overline{WR}$. To generate E, $\overline{RD}$ and $\overline{WR}$ are 'NAND'ed together. The generation of the R/W signal is done by driving the Set input and the Reset input of a $\overline{RS}$ flip flop with $\overline{RD}$ and $\overline{WR}$ respectively. The Q output may be connected directly to R/$\overline{W}$. R/$\overline{W}$ will maintain the same state until the opposite operation occurs, but it will only affect the Group 1 components when the device is selected, and then it will have the correct state with ample set up and hold times. It is important to note that R/$\overline{W}$ has a minimum set up time with respect to the rising edge of E. This must be accounted for in the circuit design, therefore E may have to be delayed.

The final difference is that the 8085 circuit is that the interrupt input, RST is active high, so the $\overline{IRQ}$ output of the Group 1 component must be inverted.

As stated before, the reason that different interface is required for several Group 1 components is various applications may require these components require a regular E strobe. The MT8880 uses the E strobe to update the status of the $\overline{IRQ}$ pin and a bit in the status register that shows a valid DTMF (Dual Tone Multiple Frequency) tone has been received. These signals will only become active if E is strobed during a period when a DTMF tone is actually present (the device retains no memory of such an event if it has already passed when E is strobed), so the period between E strobes should not be quite as long as the minimum time a DTMF tone must be present. The clock need not be present if no tones are expected.

Given the above requirements, their circuit in Figure 6 must be modified to provide an E strobe with some regularity. The clock of the 8085 cannot be used directly because this clock has several cycles per bus cycle (four cycles for opcode fetches, and three for data reads/writes to memory and I/O). It would be possible to keep using the signal derived by 'NAND'ing the $\overline{RD}$ and $\overline{WR}$ that is used in Figure 6, if it could be guaranteed that the microprocessor would not be placed in a hold state ($\overline{RD}$ and $\overline{WR}$ will cease to toggle until the microprocessor is released). If this cannot be guaranteed, then the circuit in Figure 7 may be required.

The circuit in Figure 7 is only different from the circuit of Figure 6 in the way E is generated. To generate a constant E strobe, the circuit takes advantage of the fact that ALE and the system clock (CLK) never get placed into a high impedance state (even in hold conditions). Also events involving the $\overline{RD}$ strobe, $\overline{WR}$ strobe, ALE and CLK have a constant relationship that allows ALE to initiate an "event sequence" that is sustained by CLK and results in an E strobe synchronized with the termination of the $\overline{WR}$ and $\overline{RD}$ strobes (See Timing Diagram 1).

ALE occurs a minimum of 15 nS before the falling edge of clock cycle 1 in any 8085 bus cycle. The next falling edge of clock cycle 1 will clock the output of the first flip flop through the second flip flop to drive the E input of the Group 1 component. This output is input into a third flip flop that is clocked by the rising edge of CLK, so on the rising edge of the clock cycle 2 the output of the third flip flop will be clocked low. This output drives the D input of a fourth flip flop, which will propagate this signal on the next rising edge of CLK (clock cycle 3). Also on the fourth flip flop's output will clear the first two flip flops and coincidentally clear the signal driving the E input of the Group 1 component. This is the point where data may be removed from the bus by the component if a read is occurring and where data is still valid from the microprocessor if a write is occurring, so the proper relationship between the microprocessor and the Group 1 component is maintained. Flip flops 3 and 4 are preset by ALE going high, so all flip flops are initialized for the next bus cycle.

1.6 Interfacing to the Z80

The circuit in Figure 8 is very similar to the circuit in Figure 6 in that the Z80 must transform a $\overline{RD}$ strobe and a $\overline{WR}$ strobe into an E strobe and a R/$\overline{W}$ signal (recall the set up time for the R/$\overline{W}$ signal with respect to the E signal). The operation of the circuit is exactly the same as the circuit used for the 8085, i.e., 'NAND'ing $\overline{RD}$ and $\overline{WR}$ to form E and the RS flip flop-used to create R/$\overline{W}$. However the Z80 circuit the peripheral decode has been arbitrarily chosen to include $\overline{IORQ}$ (I/O request) active. By doing this, the 8 most significant address bits need

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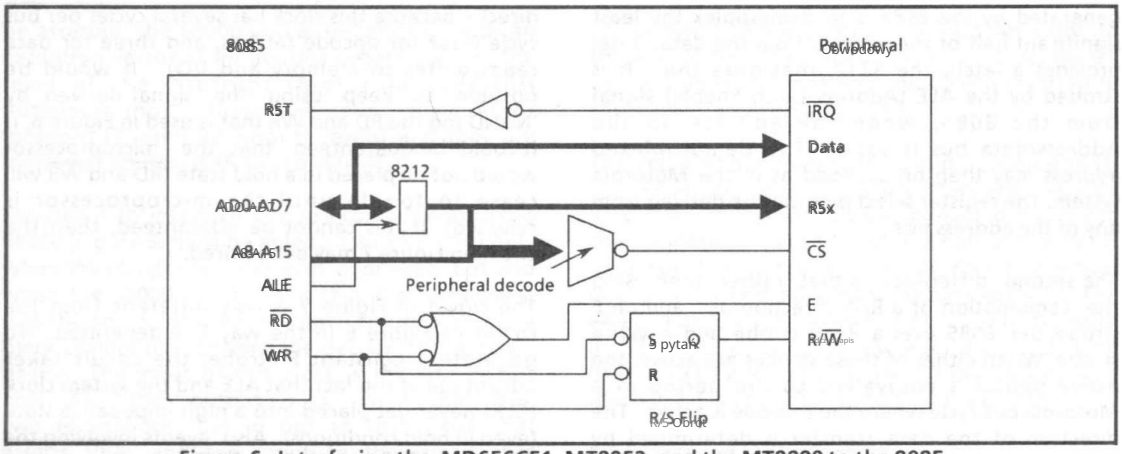

Figure 6. Interfacing the MD65SC51, MT8952, and the MT8880 to the 8085

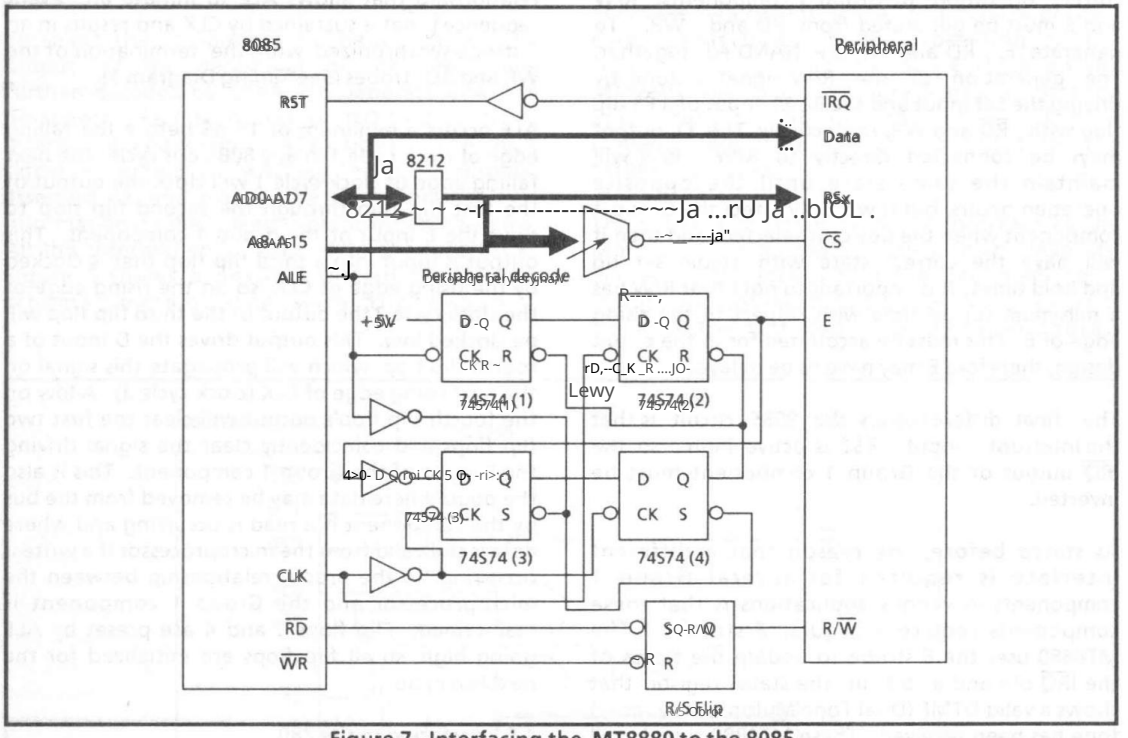

Figure 7. Interfacing the MT8880 to the 8085

not be decoded as an I/O access doesn't allow specification of more than an 8-bit address.

Another difference between this circuit and the 8085 circuit is that the address bus of the Z80 is not multiplexed so no latch is needed for a portion of the address. INT, the interrupt input does not need an inverter between the Z80 and the Group 1 component. Both the 8085 and the Z80 have autovectored interrupts or vector acquisition modes (like the 68000). The autovectored interrupts should be used.

It is impossible to generate a regular E strobe, that is not based on the RD and WR signals from the Z80. This is because the Z80 does not have a signal like ALE to unconditionally indicate the start of a bus cycle when RD and WR are not present. This may make it difficult to use the MT8880 with the Z80, given the constraints on E mentioned earlier.

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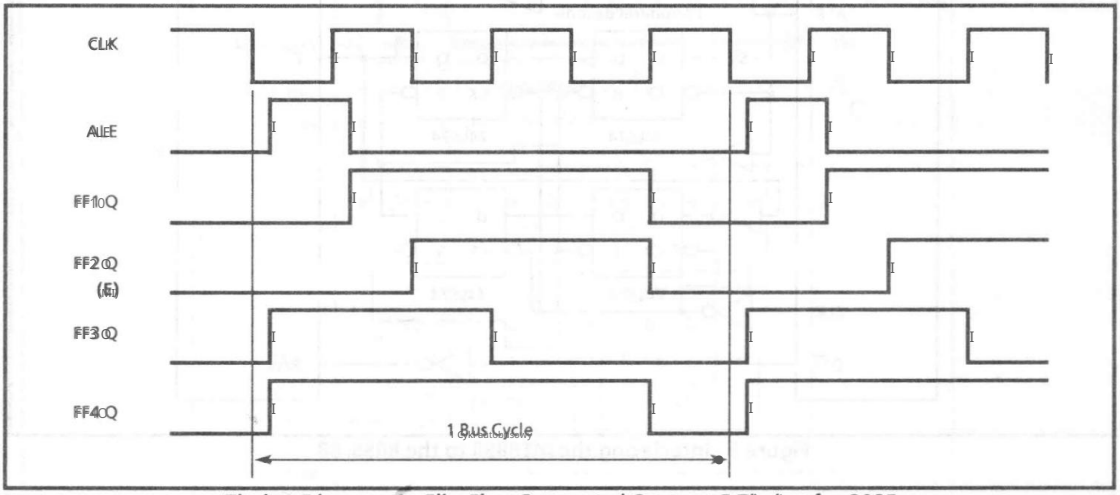
1.7 Interfacing to the 8086/88

The 8086/88 can interface to Group 1 components in very similar manner to the way the 8085 does. The 8086/88 has a multiplexed address/data bus (AD0-15 for the 8086 and AD0-8 for the 8088), ALE strobe, $\overline{RD}$ and $\overline{WR}$ strobes. Conveniently, there is a signal that can be inverted and connected directly to the R/$\overline{W}$ inputs of Group 1 components, DT/$\overline{R}$ (Data Transmit/Receive).

$\overline{BHE}$ (Bus High Enable) is an output used to indicate that information is on the high portion of the data bus (8086 only). This signal is used to qualify chip selects. To generate the E signal in applications where E is need constant, $\overline{RD}$ and $\overline{WR}$ may be 'NAND'ed together (Figure 10). The difference in the interrupt circuitry is that an 8259 Programmable Interrupt Controller may be used to handle the 8086/88's need for acquiring an interrupt vector (the 8086/88 does not provide autovectoring).

Note that although the 8086/88 has a minimum and maximum mode, the only difference in the signals required by Group 1 components is that when in maximum mode the signals may be generated by an 8288 bus controller rather than the 8086/88 itself. This is not shown in Figure 9 and Figure 10.

To generate the constant E strobe for the MT8880, a slightly altered 4 flip-flop circuit that uses ALE and CLK as its inputs is shown in Figure 9. This circuit accommodates differences in the sequence of events between the 8086/88 and the 8085.



Timing Diagram for Flip Flop Generated Constant E Timing for 8085

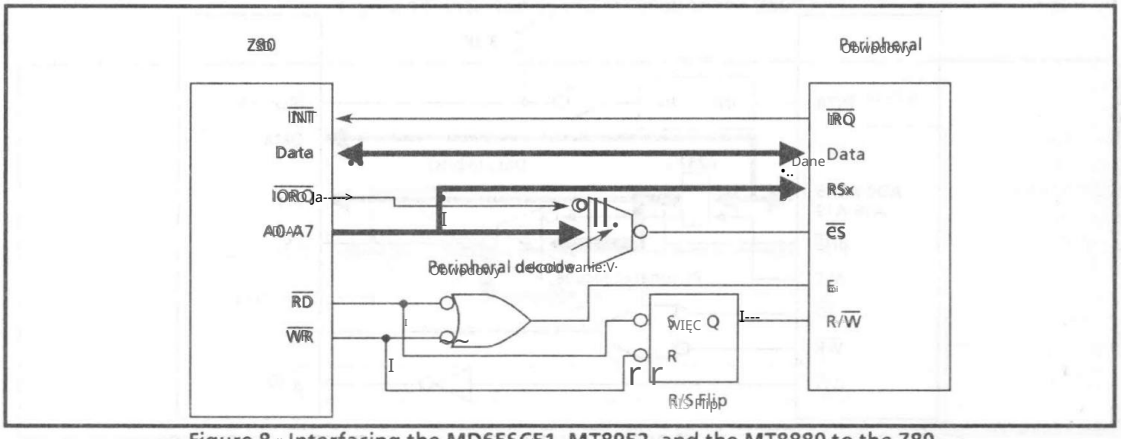


Figure 8. Interfacing the MD65SC51, MT8952, and the MT8880 to the Z80

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1.8 Interfacing to the Z8002

The circuits for interfacing the Z8002 to Group 1 components (Figures 11 and 12) are similar to the circuits for the 8086/88. The differences are:

a) The Z8002 has an active low "autovector" input (the 8259 PIC is not required).

b) AS, the Z-bus version of ALE, is active low and must be used to strobe the multiplexed address from the Address/Data bus into a 16-bit latch.

c) The Z8002 supplies a R/$\overline{W}$ signal.

d) The Z8002 $\overline{DS}$ signal is the equivalent of the 8086/88 $\overline{RD}$ and $\overline{WR}$ strobes. This signal can be inverted to form $\overline{E}$ (Figure 12) for Group 1 components.

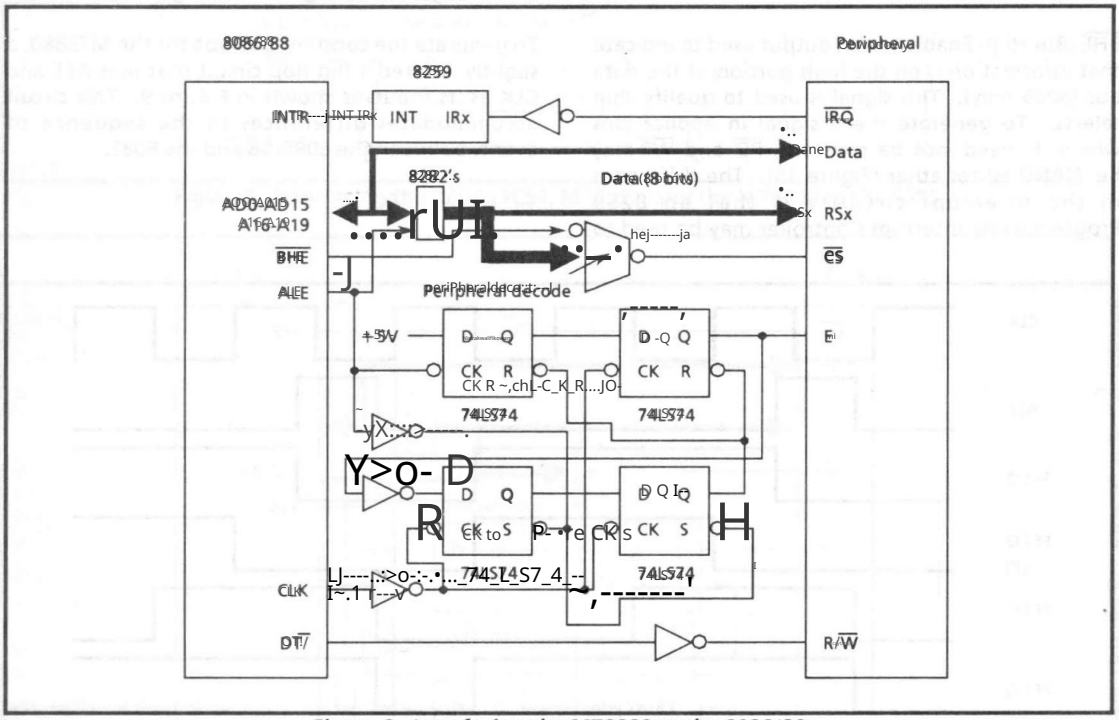

Figure 9 - Interfacing the MT8880 to the 8086/88

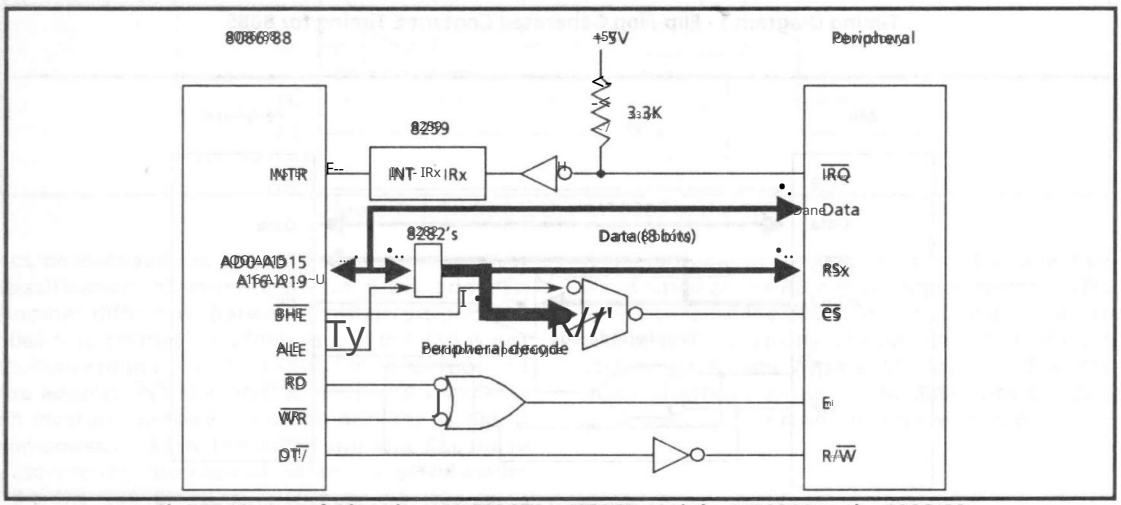

Figure 10 - Interfacing the MD65C51, MT8952, and the MT8980 to the 8086/88

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e// Różnice czasowe między układami przejściowymi przedstawionymi na rysunku 11 a rysunkiem 9 odzwierciedlają różnice w kolejności zdarzeń między Z8002 i Z8088.

These two circuits complete the Group 1 components. Fortunately, the following two groups are not complicated by the need for a constant E clock.

2.0 Group 2 Components

The interface of a Group 2 component is different from that of a Group 1 component in only two ways. The first difference is that there is no requirement for a Group 2 component to interrupt the microprocessor. This simplifies the circuit required by most of the microprocessors minimally, but for Motorola's 6800/02/08, 8086/88) the simplification is extensive. The other difference is that a Group 2 device may respond more slowly to microprocessor accesses. This suggests a

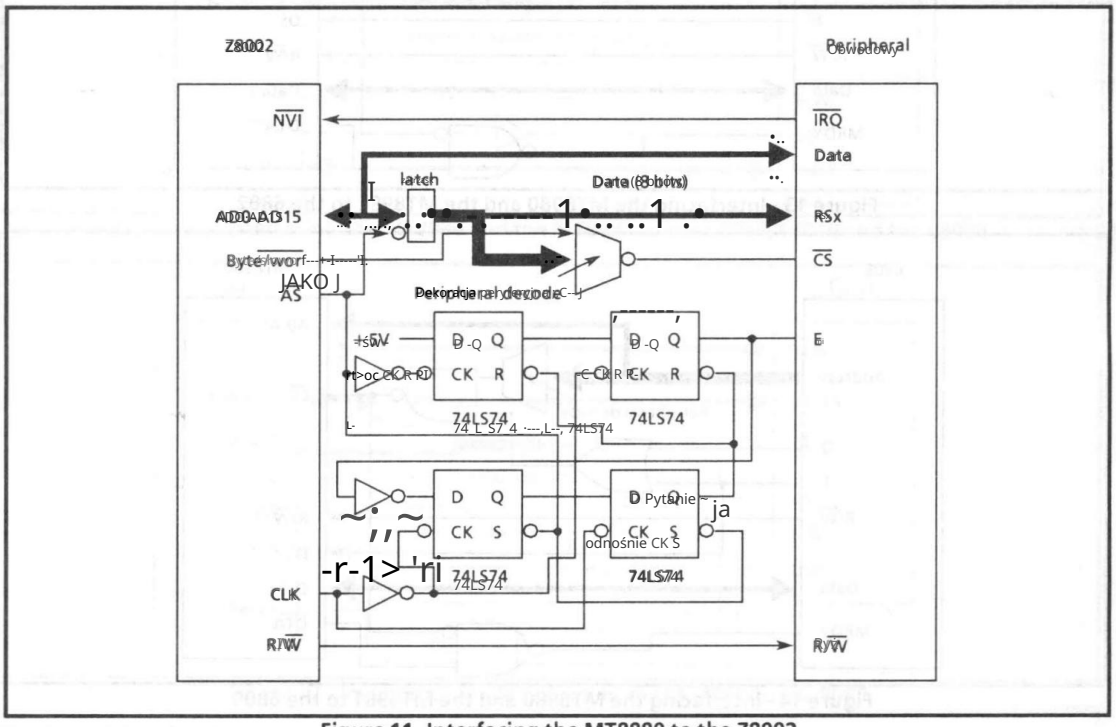

Figure 11 - Interfacing the MT8880 to the Z8002

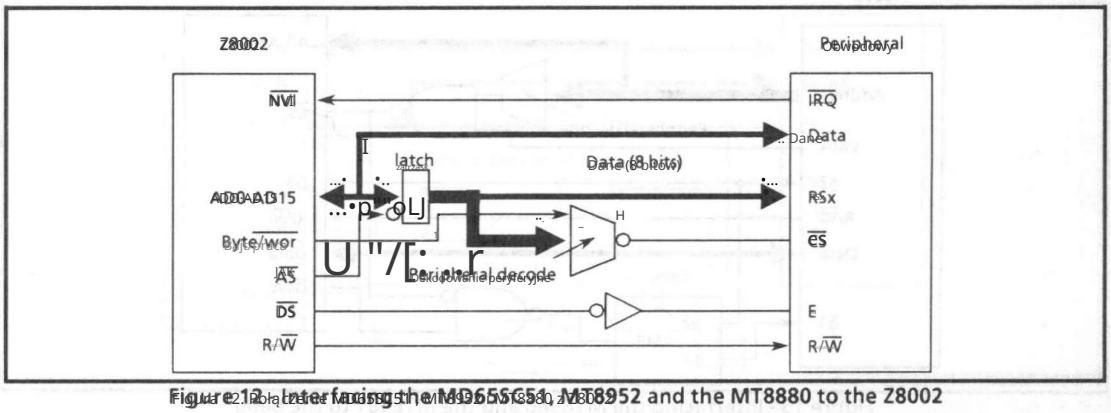

Figure 12 - Interfacing the MC6655G51, MT8952 and the MT8880 to the Z8002

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requirement for a Memory Ready output from the Group 2 component.

Actually, Group 2 components have an output called DTA which can also serve as an input

do DTACK in the 68000/10/08. In fact, DTA was designed for the 68000 so it needs extra circuitry to interface to the "memory ready" schemes of the synchronous microprocessors. This circuit consists of ANDing the signal that

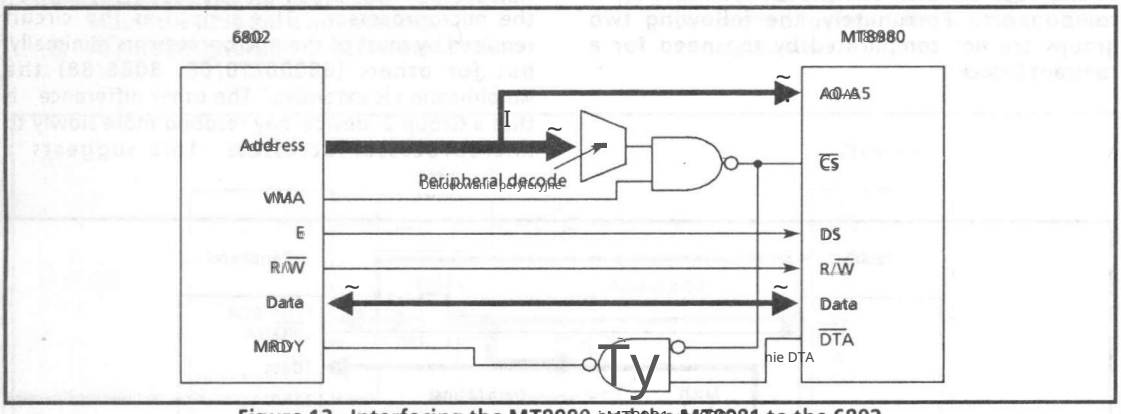

Figure 13 - Interfacing the MT8980 and the MT8981 to the 6802

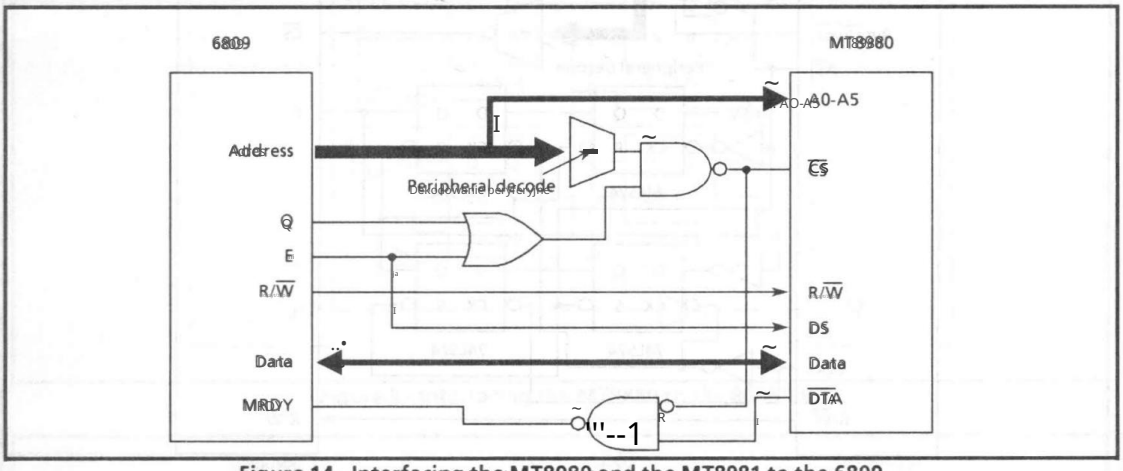

Figure 14 - Interfacing the MT8980 and the MT8981 to the 6809

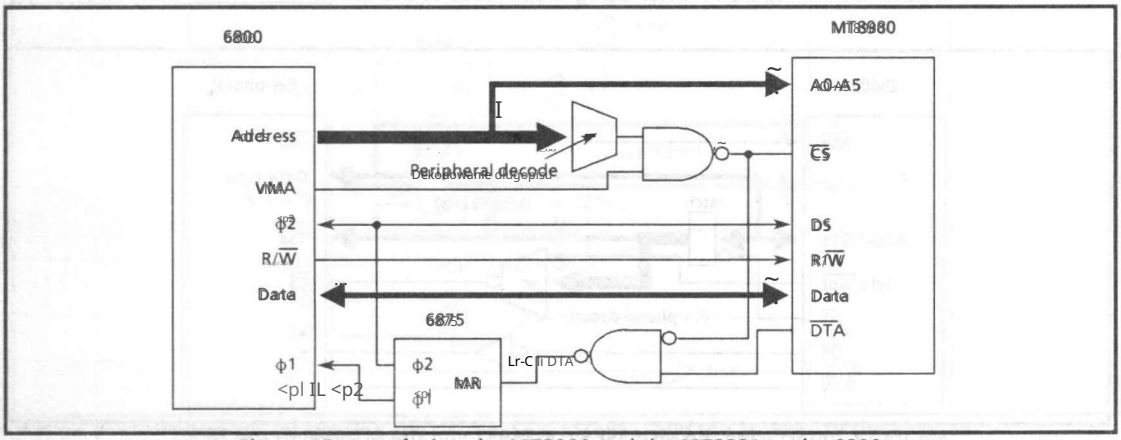

Figure 15 - Interfacing the MT8980 and the MT8981 to the 6800

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selects the Group 2 component with the $\overline{DTA}$ signal.

Aside from the above circuit change, each Group 2 interface circuit is the same as the Group 1 circuit, so a discussion on each circuit is not necessary. Note, however, that the 68000/10/08 circuit does not require the use of the E/$\overline{VMA}$/$\overline{VPA}$ interface (data strobe from the microprocessor must be inverted). Interfaces for Group 2 components are shown in Figures 13 to 20.

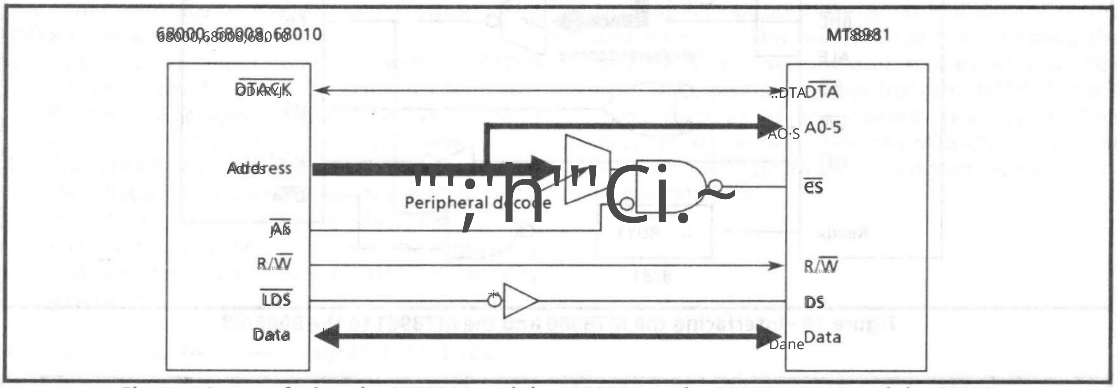

Figure 16 - Interfacing the MT8980 and the MT8981 to the 68000, 68010 and the 68008

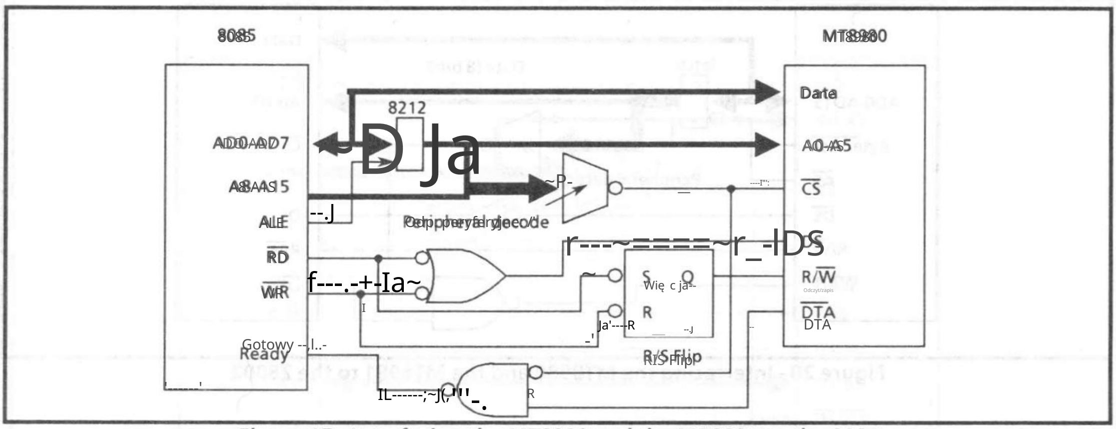

Figure 17 - Interfacing the MT8980 and the MT8981 to the 8085

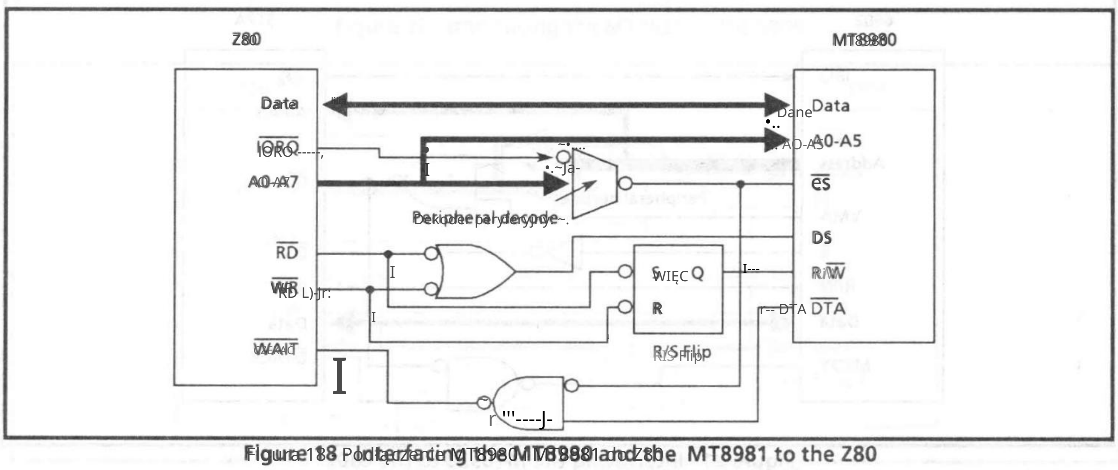

Figure 18 - Interfacing the MT8980 and the MT8981 to the Z80

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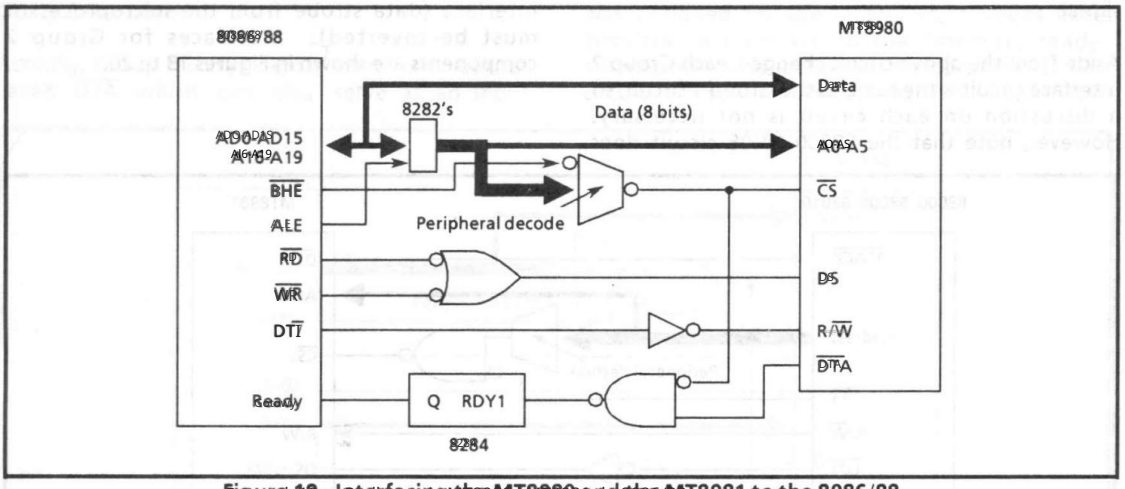

Figure 19 – Interfacing the MT8980 and the MT8981 to the 8086/88

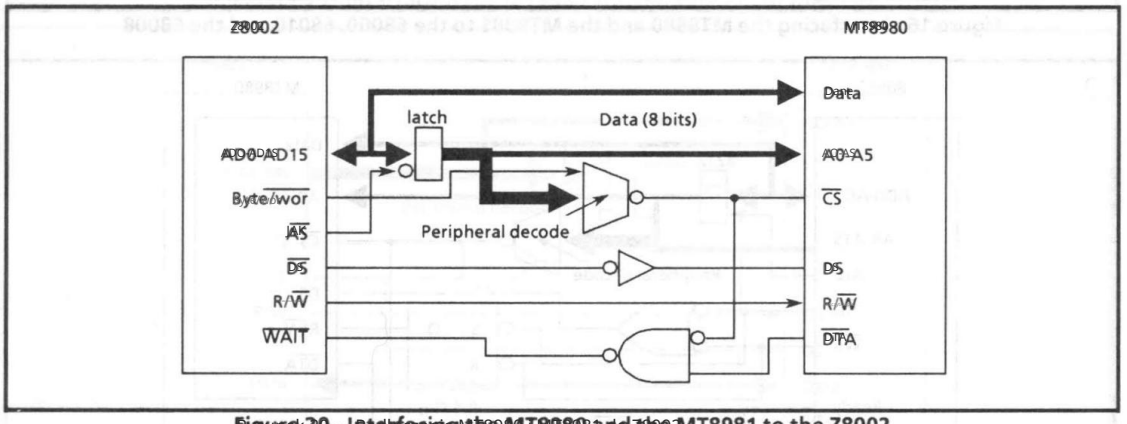

Figure 20 – Interfacing the MT8980 and the MT8981 to the Z8002

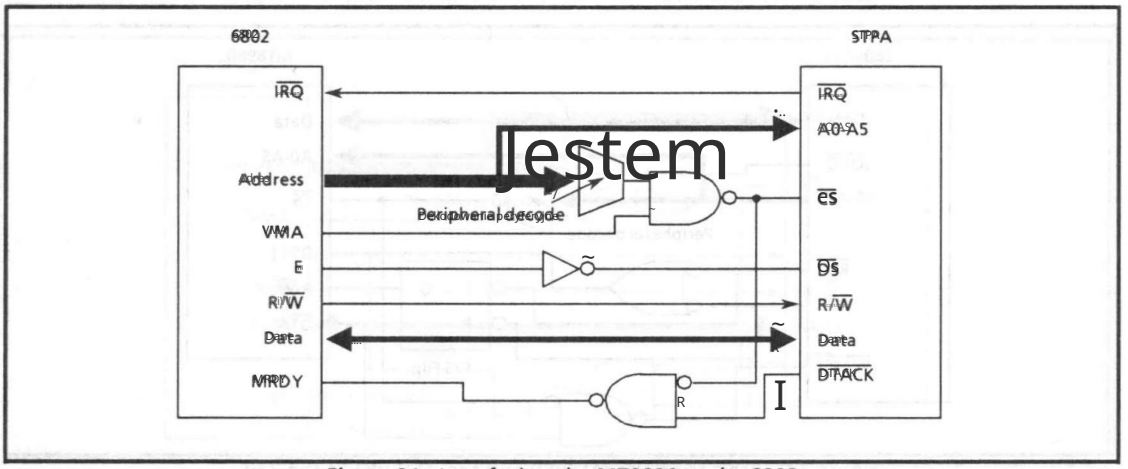

Figure 21 – Interfacing the MT8920 to the 6802

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3.0 Group 3 Components

The Group 3 component is a device called the ST-BUS Parallel Access (STPA). The STPA has three operating modes but only one mode was designed specifically for microprocessor control, so the others shall not be covered. The STPA has almost the same interface as the Group 1 devices. The differences are:

a/ Data strobe is the proper polarity for the 68000 which can be wired directly to Motorola 8-bit microprocessors. Only slight modifications are performed for other microprocessors.

b/ The STPA can provide vectored interrupts for the 68000. This will change the 68000/10/08 interface circuit (Figure 24), but other microprocessors should ignore this capability and use "autovectoring" schemes already described.

Figures 21 to 28 show diagrams of Group 3 interfaces.

3.1 Interfacing to the 68000/10/08

Figure 24 shows the circuit required to interface the MT8920 to the 68000. Note, the $\overline{IACK}$ is decoded, but rather than being combined with the chip select signal to produce VPA, $\overline{IACK}$ combines with the state of A1-3 to provide an alternative select to the MT8980 (as opposed to the normal decode of the address bus). This dual approach to selecting the MT8980 is used because an interrupt acknowledge cycle transfers information from the MT8920 in the same manner as any normal read cycle. The decoded signal $\overline{IACK}$ tells the MT8920 that it must transfer the interrupt vector programmed into it on to the data bus.

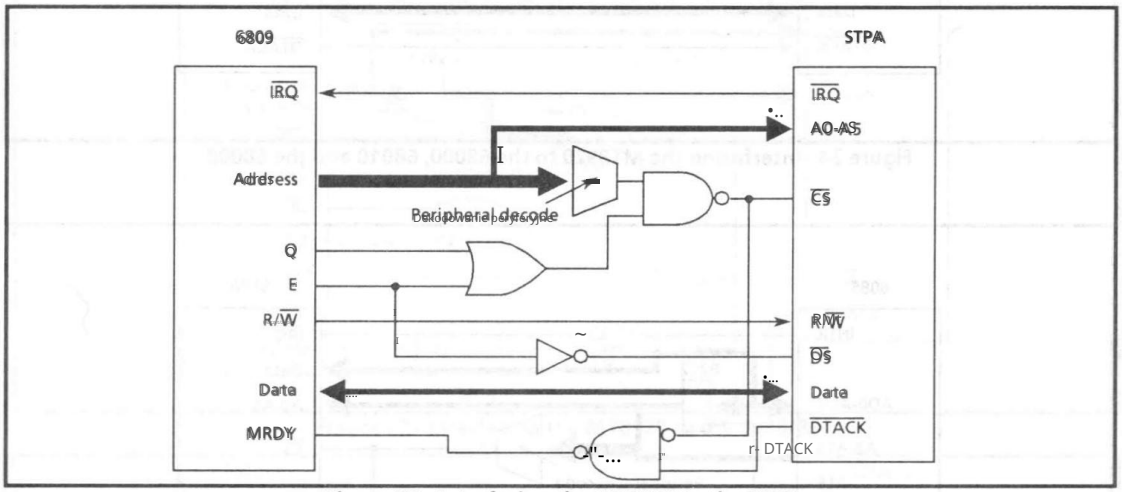

Figure 22. Interfacing the MT8920 to the 6809

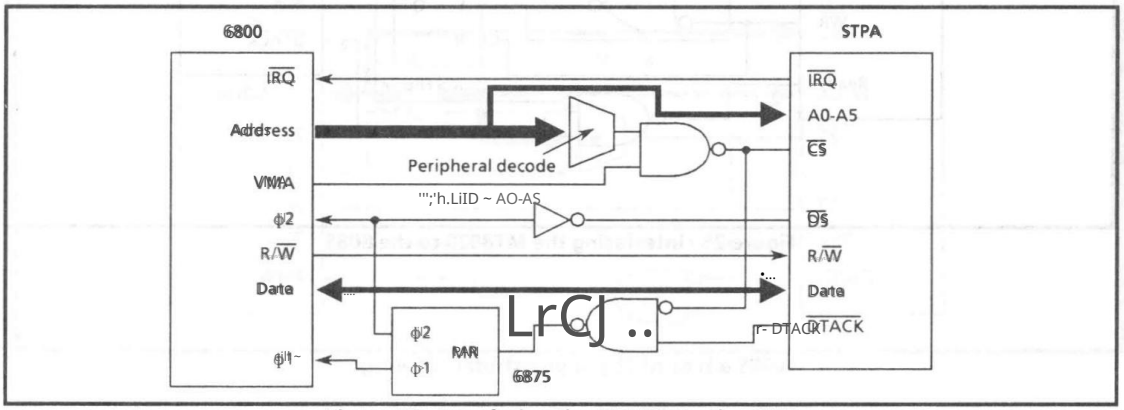

Figure 23. Interfacing the MT8920 to the 6800

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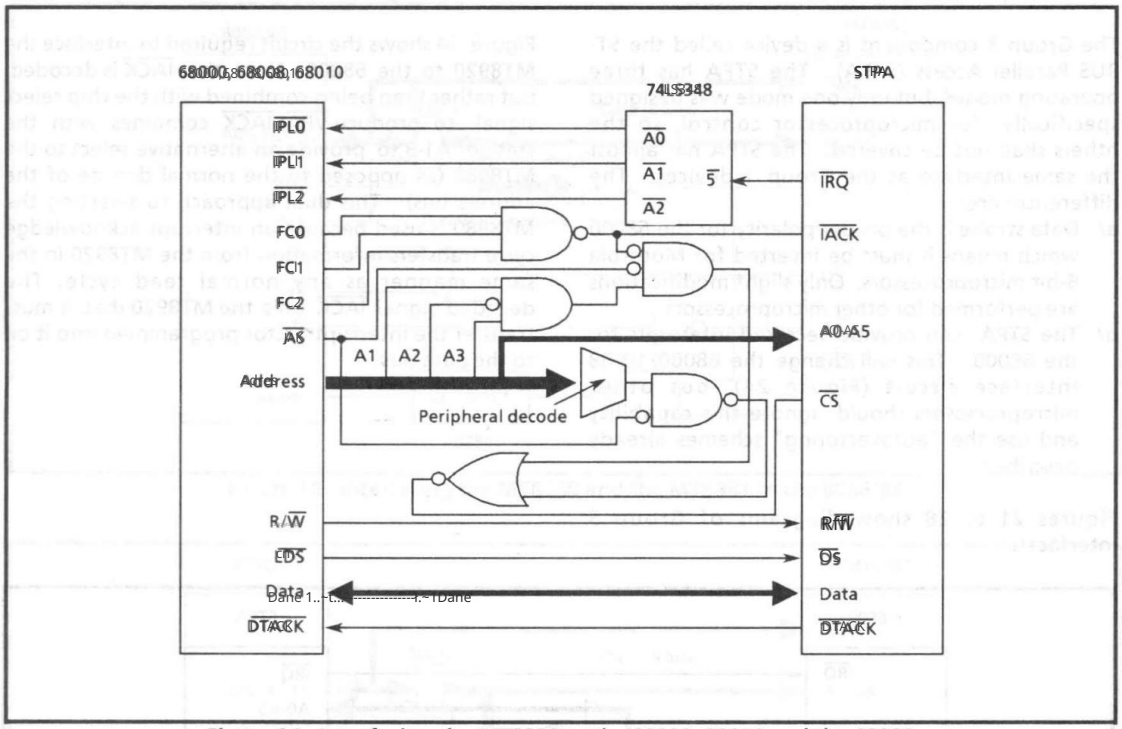

Figure 24 - Interfacing the STPA to the 68000, 68010 and the 68008

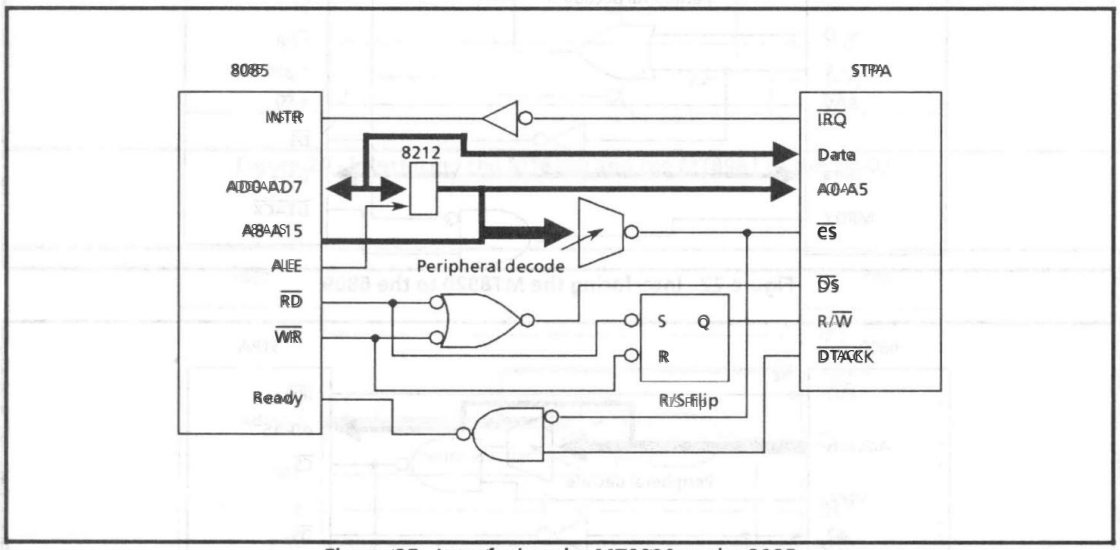

Figure 25 - Interfacing the STPA to the 8085

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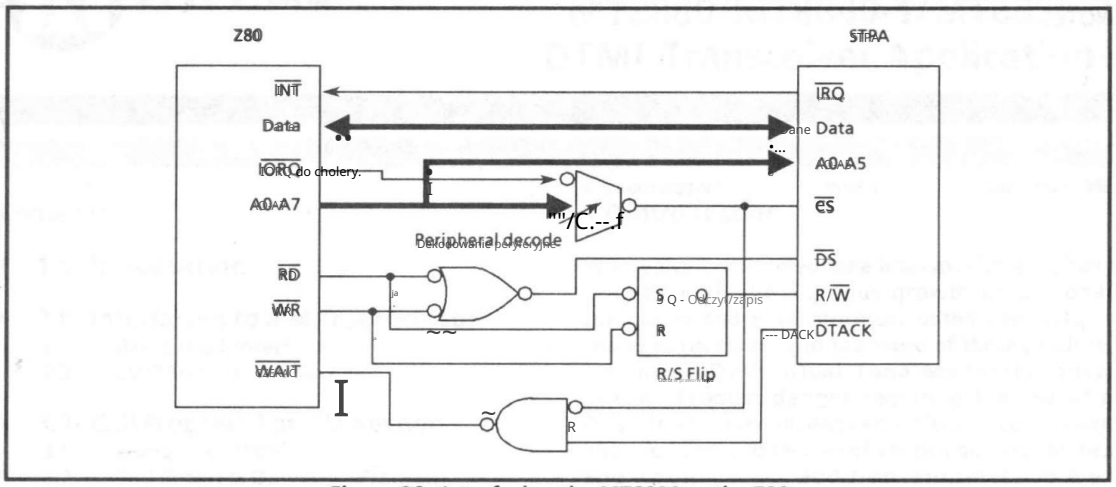

Figure 26 – Interfacing the MT8920 to the Z80

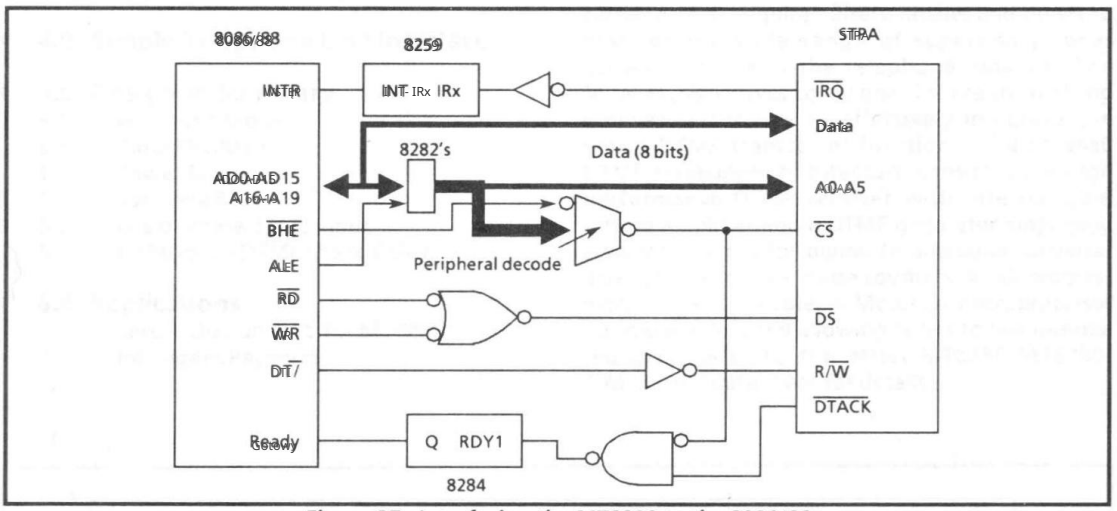

Figure 27 – Interfacing the MT8920 to the 8086/88

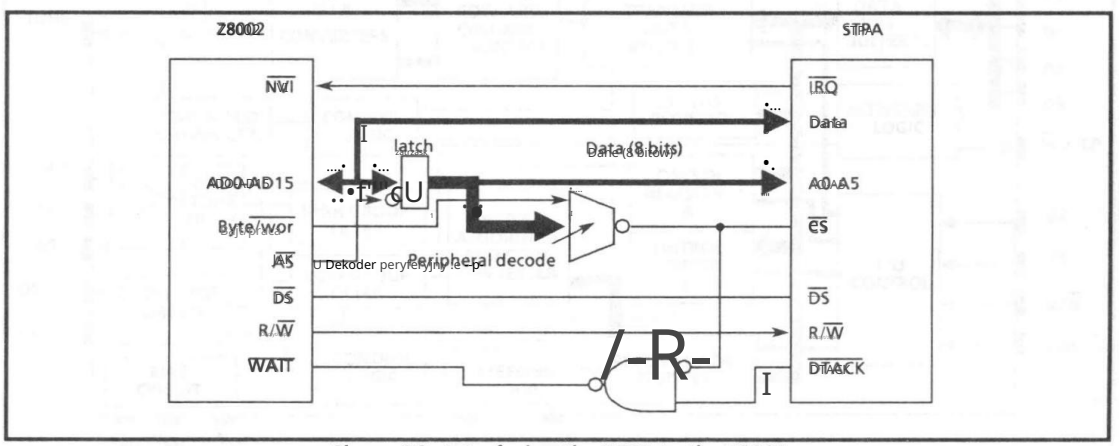

Figure 28 – Interfacing the MT8920 to the Z8002

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1.0 Introduction

1.0 Wprowadzenie

With voice grade telephone lines available globally coupled with the vigorous growth of personal computers and microprocessor based products, it comes as no surprise to see more of these products employing DTMF (Dual Tone Multi-Frequency) devices. Product designs requiring the use of a DTMF transmitter, receiver and microprocessor have also required a collection of various buffers, latches and counters. In addition, automatic dialer applications (mobile radio and alternate common carrier access) require filters, latches and timers to monitor the wide range of supervisory tones currently in use in the telephone network. The Mitel MT8880 saves costly board space by applying innovative circuitry to effectively integrate the call progress and DTMF transceiver function. The MT8880 DTMF transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator employing a switched capacitor digital to analogue converter and automatic burst mode counters. A call progress mode is also available. A Motorola microprocessor interface is included allowing access to five internal registers. Refer to Mitel MT8880/MT8880-1/MT8880-2 data sheet for details.

Z wielu dostępnymi na całym świecie liniami telefonicznymi o jakości głosowej, w połączeniu z dynamicznie rozwijającym się rynkiem komputerów osobistych i produktów opartych na mikroprocesorach, nie jest zaskoczeniem, że coraz więcej produktów wykorzystuje DTMF (Dual Tone Multi-Frequency). Urządzenia. Projekty produktów wymagające użycia nadajnika, odbiornika i mikroprocesora DTMF mają również wymagane kolekcje różnych buforów, zatrzasków i liczników. Ponadto aplikacje automatycznego dialera (radio mobilne i alternatywny dostęp do operatora) wymagają filtrów, zatrzasków i timerów do monitorowania szerokiego zakresu tonów nadzorczych obecnie używanych w sieci telefonicznej. Mitel MT8880 pozwala zaoszczędzić kosztowne miejsce na płytce, integrując zaawansowany układ elektroniczny umożliwiający efektywną integrację funkcji postępu połączenia i transceivera DTMF. Architektura transceivera DTMF MT8880 składa się z wysokiej wydajności odbiornika DTMF z wbudowanym wzmacniaczem o zmiennym wzmocnieniu i generatora DTMF wykorzystującego przetwornik cyfrowo-analogowy z przełączanymi kondensatorami i automatyczne liczniki trybu burst. Tryb postępu połączenia jest również dostępny. Zapewniony jest interfejs mikroprocesora Motorola, który umożliwia dostęp do pięciu wewnętrznych rejestrów. Szczegóły można znaleźć w arkuszu danych Mitel MT8880/MT8880-1/MT8880-2.

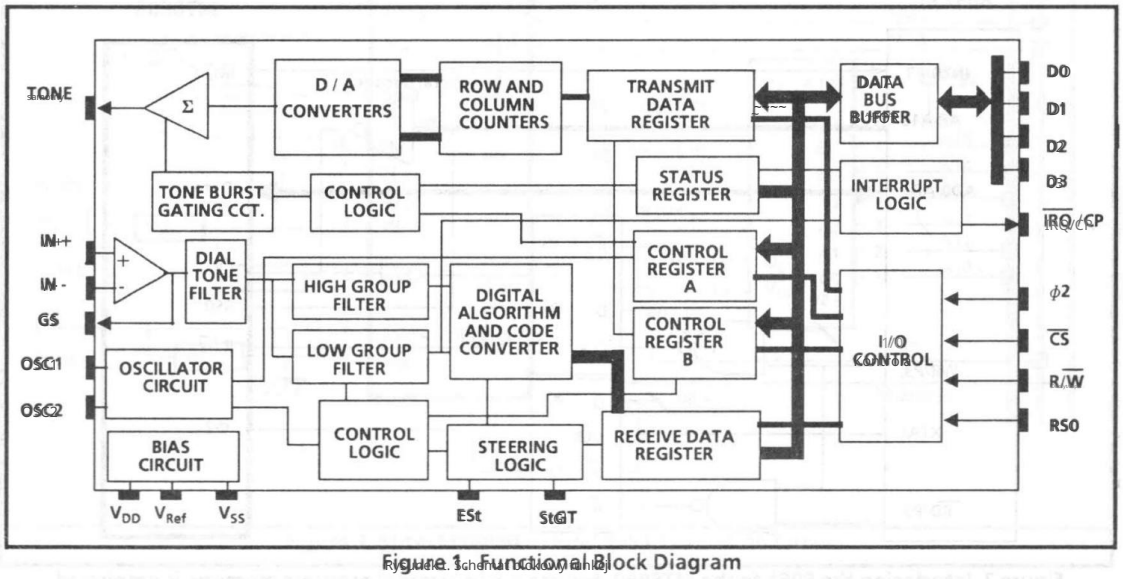

Figure 1. Functional Block Diagram

Rysunek 1. Schemat blokowy funkcji

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2.0 Interfacing to a Microprocessor

2.1 INTEL 8051 Interface

The Intel 8051 is a microcomputer which can provide a cost effective solution for many controller applications. Very compact systems including autodialers, secure access modems, credit card verification and telemetry can be implemented with the MT8880 and the 8051. The circuitry shown in Figure 2 shows how the MT8880 and 8051 can be interfaced. The application outlined here uses the internal program memory on the 8051 and accesses the MT8880 via external data memory. By using external data memory the RD and WR pins (alternate functions of P3.7 and P3.6) are activated which can be used to generate the required Phase 2 clock and R/$\overline{W}$ signals on the MT8880. When external data memory is not being accessed, there will be no activity on the RD and WR outputs, however, the MT8880 requires a clock input on the Phase 2 pin at all times. Activity is necessary to update the internal registers and provide interrupt signals used in servicing the DTMF receiver or transmitter functions. If the MT8880 is not being accessed, the frequency of the Phase 2 signal may be reduced. The recommended maximum Phase 2 period (when the MT8880 is not selected) is 1 ms. Durations longer than this may result in failure to produce an interrupt at the correct time or failure in updating the Status Register. Suitable activity for the Phase 2 input can be obtained by writing or reading to external data memory with attention given to the maximum Phase 2 period mentioned above. If external program memory is being used, this allows the output PSEN to be used as a source of activity suitable for the MT8880 Phase 2 input. The circuit shown in Figure 4 could be modified to make Phase 2 a function of RD, WR and PSEN. When external program memory is not being used, some 8051 internal timer can be used as a baud rate generator set up in mode 0. This mode sets up a baud rate which is 1/12 the oscillator frequency. The output is transmitted through TXD.

During the period when the MT8880 is being accessed (external data memory), the circuit shown in Figure 4 will provide proper timing. The RD and WR signals are NANDed and fed to the Reset input on RS latch 1 (see Figure 2). The output of RS latch 1 is connected to the phase 2 input of the MT8880. A WR signal from the 8051 will set the output of latch 2 low inducing a Write condition at the MT8880 R/$\overline{W}$ input. Phase 2 will be asserted on the next rising edge of the system clock allowing suitable setup time. Following the Write operation (when the MT8880 is deselected) Phase 2 is reset to a logic low condition and the output of RS latch 2 (see Figure 2) will be set to a logic high which will induce a "read" condition. When accessing external memory the low byte of the address is time multiplexed with the data byte on port 0. However, in this application the low order address byte is not used and as such no demultiplexing circuitry is used. Note that EA

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MSAN-120 Application Note

2.0 Interfacing to a Microprocessor

2.1 INTEL 8051 Interface

Intel 8051 to mikrokomputer, który może zapewnić ekonomiczne rozwiązanie dla wielu zastosowań kontrolera. Bardzo kompaktowe systemy, w tym automatyczne wybieranie numerów, modemy bezpiecznego dostępu, weryfikacja kart kredytowych i systemy telemetryczne, można zrobić za pomocą MT8880 i 8051. Układ pokazany na rysunku 2 pokazują, jak można połączyć MT8880 i 8051. Przedstawiona tutaj aplikacja wykorzystuje wewnętrzną pamięć programów 8051 i uzyskuje dostęp do MT8880 za pośrednictwem zewnętrznego pamięć danych. Poprzez użycie zewnętrznej pamięci danych sygnały RD i WR (alternatywne funkcje P3.7 i P3.6), które mogą być używane do generowania wymaganego zegara Phase 2 i sygnałów R/W na MT8880. Gdy zewnętrzna pamięć danych nie jest dostępna, wyjścia RD i WR nie będą aktywne, jednak MT8880 wymaga wejścia zegara na pinie Phase2 przez cały czas. Aktywność jest konieczna do aktualizacji rejestrów wewnętrznych i dostarczania sygnałów przerwania używanych do obsługi funkcji odbiornika lub nadajnika DTMF. Jeśli MT8880 nie jest dostępny, częstotliwość sygnału Phase 2 może zostać zmniejszona. Zalecany maksymalny okres Phase2 (gdy MT8880 nie jest wybrany) wynosi 1 ms. Czasy dłuższe niż ten mogą spowodować brak wygenerowania przerwania we właściwym czasie lub brak aktualizacji rejestru stanu. Odpowiednią aktywność dla wejścia Phase2 można uzyskać, zapisując lub odczytując

external data memory with attention given to the maximum Phase 2 period mentioned above. If external program memory is being used, this allows the output PSEN to be used as a source of activity suitable for the MT8880 Phase 2 input. The circuit shown in Figure 4 could be modified to make Phase 2 a function of RD, WR and PSEN. When external program memory is not being used, some 8051 internal timer can be used as a baud rate generator set up in mode 0. This mode sets up a baud rate which is 1/12 the oscillator frequency. The output is transmitted through TXD.

Układ pokazany na rysunku 4 można zmodyfikować tak, aby faza 2 była funkcją RD, WR i PSEN. Jeżeli zewnętrzna pamięć programów nie jest używana, wewnętrzny timer 8051 może być użyty jako generator szybkości transmisji ustawiania jeden na 8051 w trybie 0. Ten tryb ustawia szybkość transmisji o 1/12 częstotliwości oscylatora. Dane wyjściowe przesyłane są poprzez TXD.

W okresie, gdy MT8880 jest dostępny (zewnętrzna pamięć danych), obwód pokazany na rysunku 4 zapewni właściwe taktowanie. Sygnały RD i WR są NANDowane i podawane do wejścia Reset na zatrzasku RS 1 (patrz rysunek 2). Wyjście zatrzasku RS 1 jest podłączone do wejścia fazy 2 MT8880. Sygnał WR z 8051 ustawi wyjście zatrzasku 2 na niski, indukując warunek zapisu na wejściu R/W MT8880. Faza 2 zostanie potwierdzona na następnym dodatnim zboczu zegara systemowego, umożliwiając odpowiedni czas konfiguracji. Po operacji zapisu (gdy MT8880 jest odznaczony), faza 2 jest resetowana do stanu niskiego logicznego, a wyjście RSlatch 2 (patrz Rysunek 2) zostanie ustawione na wysoki logiczny, co wywoła stan „odczytu” podczas uzyskiwania dostępu do adapamięci zewnętrznej, niski bajt adresu jest multipleksowany czasowo z bajtem danych na porcie 0. Jednak w tej aplikacji bajt adresu nie jest używany, jako taki nie jest używany żaden obwód demultipleksujący. Należy zauważyć, że EA

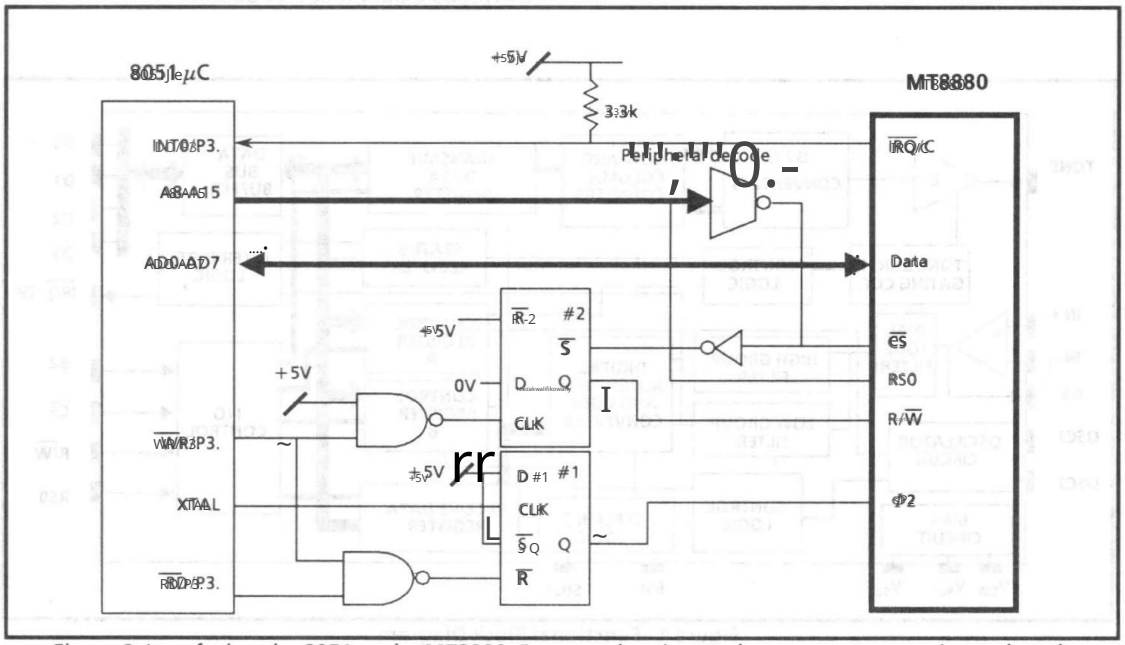

Figure 2. Interfacing the 8051 to the MT8880. For use when internal program memory is employed.

Rysunek 2. Podłączanie układu 8051 do układu MT8880. Do stosowania w przypadku korzystania z wewnętrznej pamięci programu.

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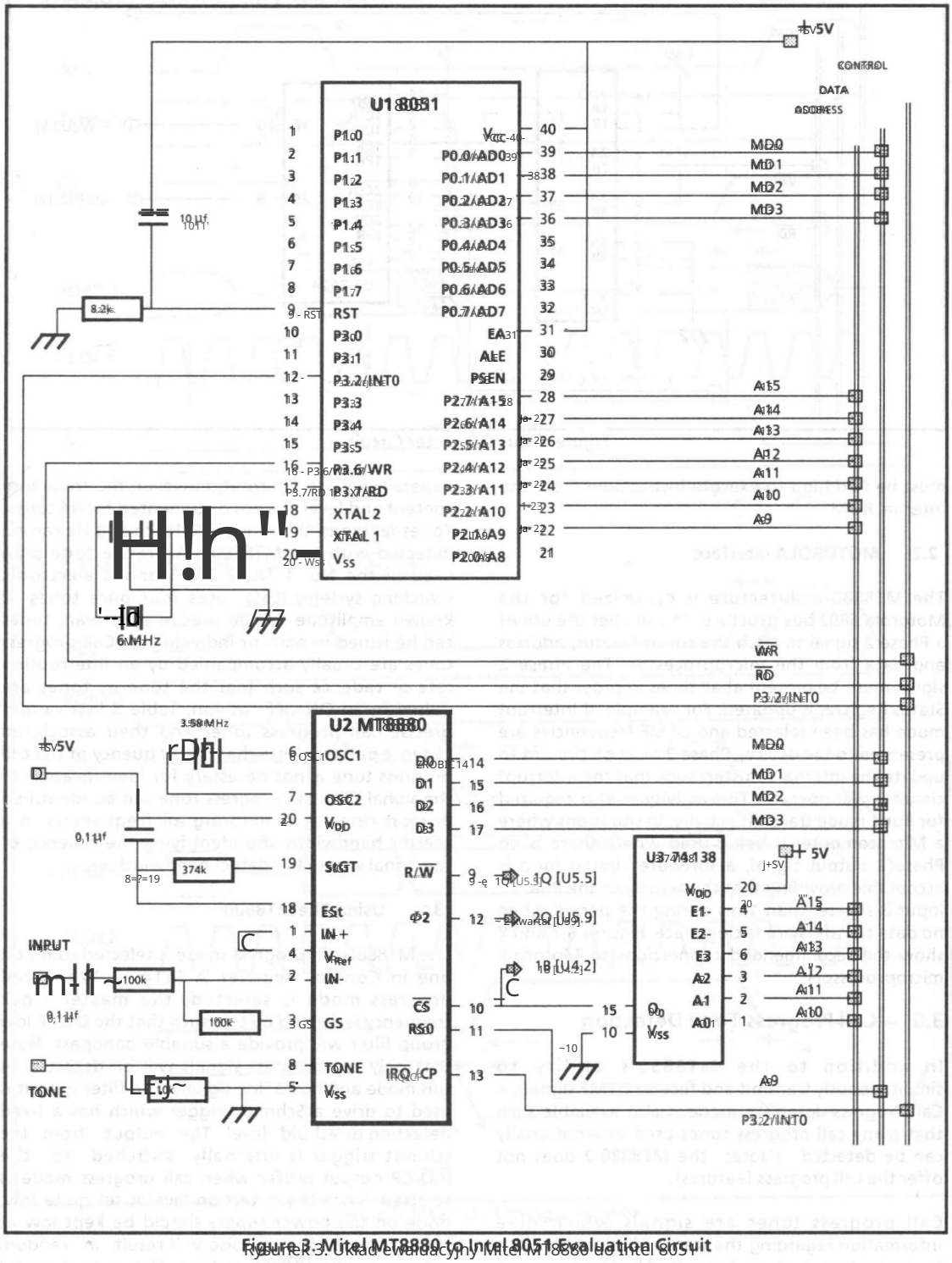

Figure 3. Mitel MT8880 to Intel 8051 Evaluation Circuit

Rysunek 3. Układ ewaluacyjny Mitel MT8880 do Intel 8051

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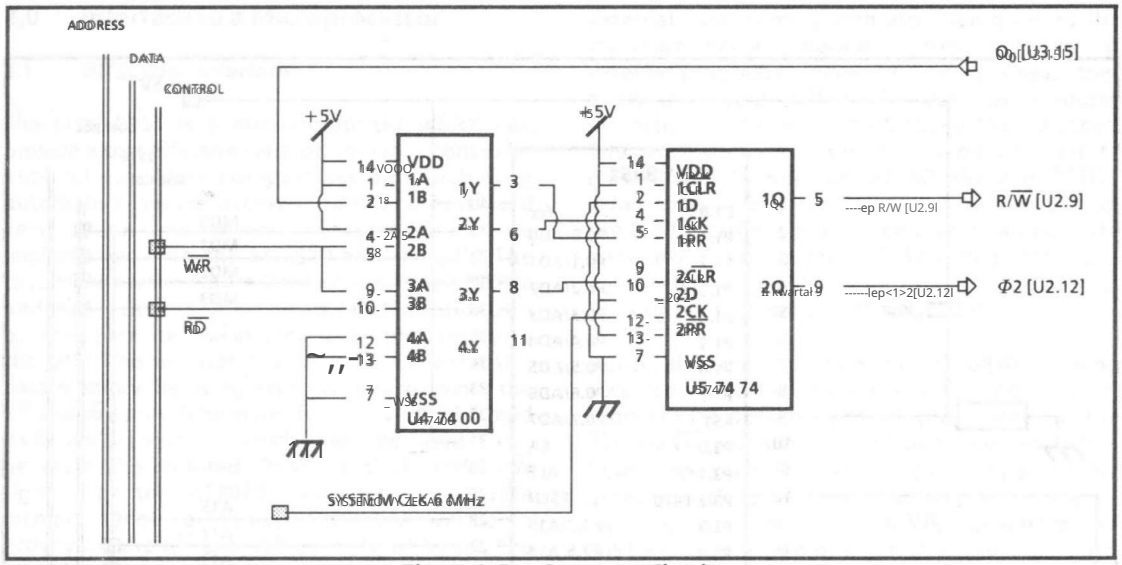

Figure 4 Bus Converter Circuit

must be tied high to execute instructions from the internal ROM.

2.2 MOTOROLA Interface

The MT8880 architecture is optimized for the Motorola 6802 bus structure. This implies the use of a Phase 2 signal to latch the control status, address and data from the microprocessor. The Phase 2 signal must be present at all times in order that the Status Register is updated. For example, if interrupt mode has been selected and DTMF frequencies are presented to the device, Phase 2 must be present to update the internal registers such that the interrupt circuitry will become active. This scenario also applies for Burst mode transmit activity. In situations where a Microcomputer is being used where there is no Phase 2 output signal, a software timing loop is acceptable providing that the activity to the Phase 2 input is shorter than 1 ms during the period when no data transfers are taking place. Figures 6,7 and 8 show the recommended connections to Motorola microprocessors.

3.0 Call Progress Tone Detection

In addition to the MT8880's ability to simultaneously transmit and receive DTMF signals, a Call Progress detection mode is also available such that many call progress tones used internationally can be detected. (Note: the MT8880-2 does not offer the call progress features).

Call progress tones are signals which give information regarding the status of telephone calls to operators and customers. These tones are generally easy to interpret, however, the frequency content and level are not documented for all tones. Tones falling in the range 320 Hz to 510 Hz can be detected with the MT8880. A precise tone plan is used in the No. 1A, 2A, 3 and 4 electronic switching systems (ESS) uses four pure tones of known amplitude. In the precise tone plan, tones can be presented singly or in pairs. Individual tones are usually accompanied by an interruption in order to indicate such that the tone or tones are pulsed in an ON/OFF fashion. Table 3 lists various precise call progress tones and their associated cadence pattern. Note that the frequency of the call progress tone is not necessary for identification of the signal. The call progress tone can be identified in most cases by monitoring all frequencies in a specific bandwidth and identifying the cadence of the signal within the detect bandwidth.

3.1 Using The MT8880

The MT8880 call progress mode is selected using bit CP in Control Register 1 (b1 = 1). When call progress mode is activated, the master clock frequency is divided by seven and the DTMF low group filter will provide a suitable bandpass. Note that only call progress signals will be detected in this mode and no DTMF signals. The filter output is used to drive a Schmitt trigger which has a fixed detection threshold level. The output from the Schmitt trigger is internally switched to the IRQ/CP output buffer. In call progress mode, IRQ/CP will output the call progress signal. Since the detection level is very low, noise on the power supply should be kept low at the device. Excessive noise will result in random activity on the IRQ/CP output. The output signal

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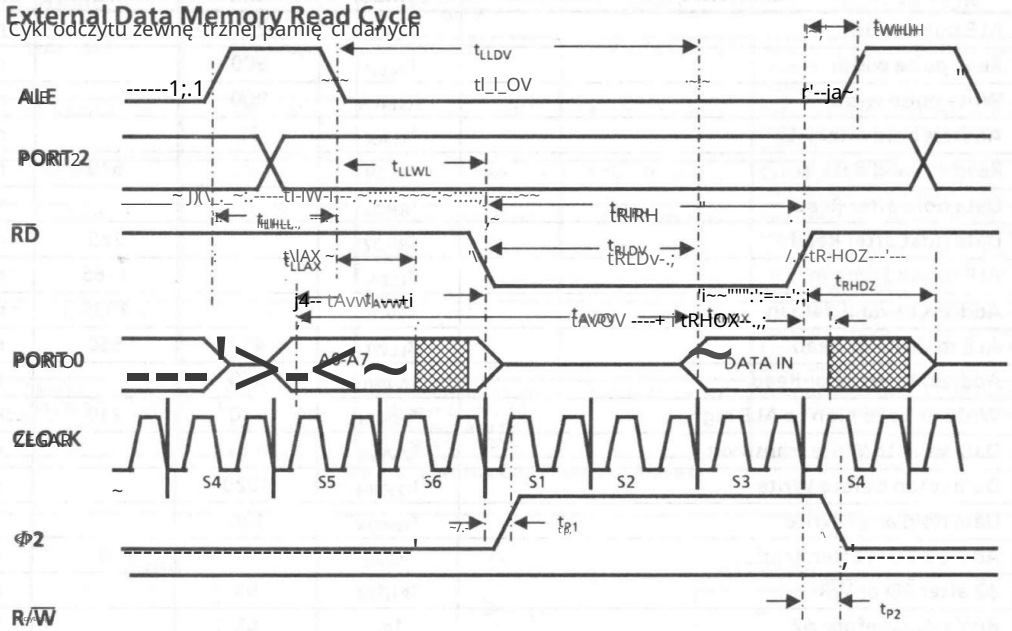
External Data Memory Read Cycle

Cykl odczytu zewnętrznej pamięci danych



External Data Memory Write Cycle

Cykl zapisu zewnętrznej pamięci danych

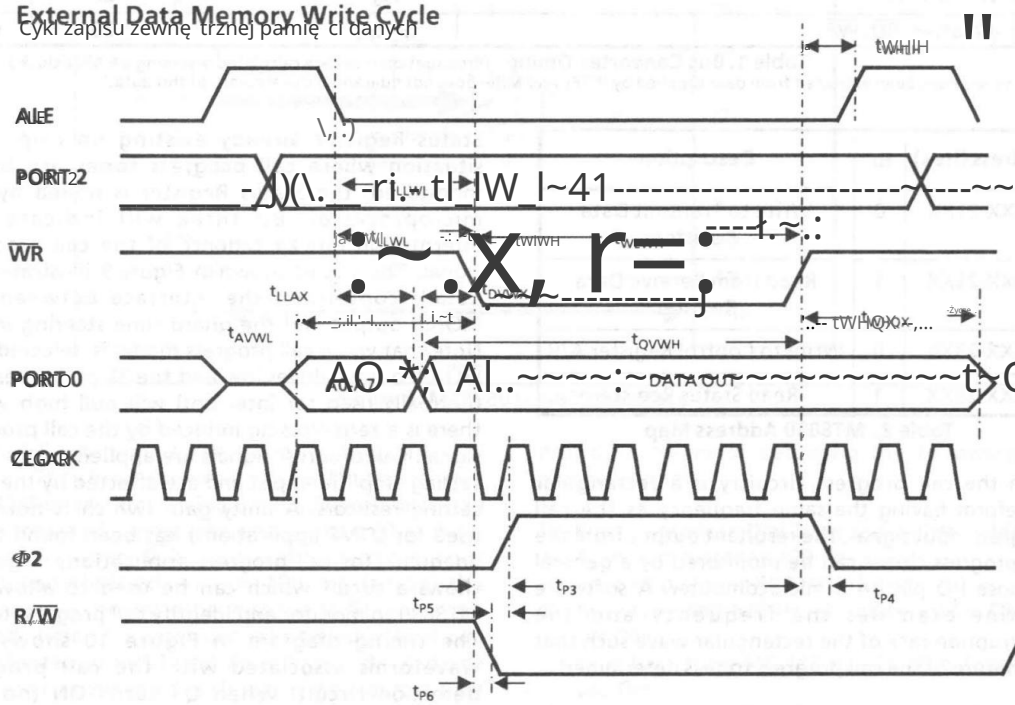


Figure 5. Interface Timing Diagrams

Rysunek 5. Diagramy czasowe interfejsu

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	Parameters	Symbol	Min	Max	Units
1	ALE pulse width	t_{LHLL}	295		ns
2	Read pulse width	t_{RLRH}	900		ns
3	Write pulse width	t_{WLWH}	900		ns
4	Address hold after ALE	t_{LLAX}	35		ns
5	Read to valid data in	t_{RLDV}		670	ns
6	Data hold after Read	t_{RHDX}	0		ns
7	Data float after Read	t_{RHDZ}		265	ns
8	ALE to valid data in	t_{LLDV}		1185	ns
9	Address to valid data in	t_{AVDV}		1335	ns
10	ALE to Write or Read	t_{LLWL}	450	550	ns
11	Address to Write or Read	t_{AVWL}	540		ns
12	Write or Read high to ALE high	t_{WHLH}	130	210	ns
13	Data valid to Write transition	t_{DVWX}	110		ns
14	Data setup before Write	t_{QVWH}	1020		ns
15	Data hold after Write	t_{WHQX}	120		ns
16	Address float after Read	t_{RLAZ}		0	ns
17	φ2 after $\overline{RD}$ or $\overline{WR}$	t_{p1}, t_{p3}	85		ns
18	R/$\overline{W}$ setup before φ2	t_{p5}	65		ns
19	$\overline{WR}$ to R/$\overline{W}$	t_{p6}		20	ns
20	φ2 after $\overline{RD}$, $\overline{WR}$	t_{p2}, t_{p4}		20	ns

Table 1 Bus Converter Timing (Propagation delays calculated assuming a 6 MHz clock.)
Values have been extracted from data supplied by INTEL and MITEL does not guarantee the accuracy of this data.

Address (Hex)	R/	Description
20XX-21XX	0	Write to Transmit Data Register
20XX-21XX	1	Read from Receive Data Register
22XX-23XX	0	Write to Control Register A/B
22XX-23XX	1	Read Status Register

Table 2. MT8880 Address Map

from the call progress circuitry is a rectangular waveform having the same frequency as the call progress input signal. The resultant output from the call progress circuit can be monitored by a general purpose I/O pin on a microcomputer. A software routine can examine the frequency and the interruption rate of the rectangular wave such that the nature of the call progress tone is determined.

In a system where no I/O ports are available, as is the case in the microprocessor arrangements shown in Figures 6, 7 and 8, a very simple solution exists. The call progress output can be used to drive the steering circuitry (tone verification circuitry) normally used for DTMF which will update the Status Register already existing on chip. In a situation where call progress tones are being monitored, the Status Register is polled by the microprocessor. Bit three will indicate the interruption rate or cadence of the call progress signal. The circuit shown in Figure 9 illustrates the details concerning the interface between the $\overline{IRQ}$/CP output and the guard time steering input. Note that when call progress mode is selected, the $\overline{IRQ}$/CP output drives low and the 3k pullup resistor (normally used for interrupt) will pull high when there is a zero crossing induced by the call progress signal. Call progress signals are applied at the gain setting input and are affected by the gain setting resistors. A unity gain (which is normally used for DTMF applications) has been found to be adequate for call progress applications. Figure 8 shows a circuit which can be used to allow the MT8880 to monitor and identify call progress tones. The timing diagram in Figure 10 shows the waveforms associated with the call progress detection circuit. When Q1 turns ON (no Call Progress tone), ESt is forced high and will stay in the high state unless the tone present guard time has elapsed. The threshold voltage on U1 is set by the MT8880 V_{Ref} Output. The tone present guard time is determined by the time constant formed by R3 and C2 plus the time constant determined by R5 and C3.

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NAME	FREQUENCIES (Hz)	INTERRUPTION RATE	LEVEL	DESCRIPTION
DIAL TONE	350 + 440	STEADY	-13dBm/frequency	Indicates that the receiving end is ready to receive dial pulse or DTMF signals.
AUDIBLE RINGBACK	440 + 480	2 sec. ON 4 sec. OFF	-19 dBm/frequency	Indicates that called line has been reached and that ringing has started.
LINE BUSY	480 + 620	0.5 sec. ON 0.5 sec. OFF	-24 dBm/frequency	Called customer's line has been reached but line is currently in use.
REORDER	480 + 620	0.25 sec. ON 0.25 sec. OFF	-24 dBm/frequency	Indicates that the local or toll switching transmission paths to the CO or equipment serving the customer are busy. May also indicate unassigned code.
PARTIAL DIAL TONE	480	STEADY	-17 dBm	Notifies calling party that dialing has not been processed to the allotted time and that not enough digits have been dialed.
AUTOMATIC CREDIT CARD DIALING PROMPT TONE	941 + 1477 followed by 440 + 350	940 ms exponentially decayed from -10 dBm/freq. at a time constant 200 ms	-10 dBm/frequency	Informs the customer that credit card information must be keyed in.

Table 3. Various Call Progress Tones

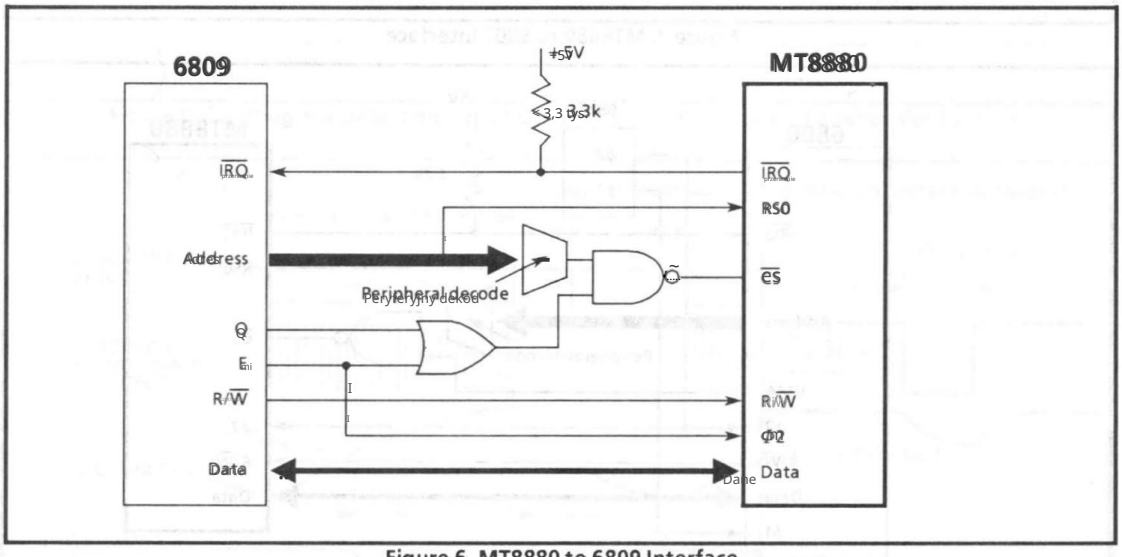

Figure 6. MT8880 to 6809 Interface

R3 and C2 determine the value for t_{GTA} in DTMF mode. The circuit shown in Figure 9 is transparent in DTMF operation. Timing is not adversely affected as a result of using the circuit since Q1 is high impedance when IRQ/CP is high. Interrupts must be acknowledged within 100 ms (using the components shown), otherwise the St/GT pin will be forced high. The interrupt acknowledge time can be adjusted with C3 and R6 in Figure 9. A diode (D2) can be connected as shown in the diagram such that interrupts from other devices are ignored.

3.2 Call Progress Detection Program

The program shown in Appendix 1 was used in conjunction with the circuit shown in Figure 9 to provide a means of detecting the following call progress signals;

1) North American Dial Tone 350/440Hz, -13dBm.
2) European dial tone 425 Hz, -6 dBm.
3) Far East dial tone 400 Hz, -15 dBm.
4) Busy tone 480/620 Hz, -24 dBm, 0.5 sec ON 0.5 sec OFF.
5) Ring back tone 440/480 Hz, -24 dBm 2 sec ON 4 sec OFF.
6) Reorder tone 480/620 Hz, -24 dBm, 0.2 sec ON 0.5 sec OFF.

Also the detection scheme correctly ignored the 850 Hz European dial tone second harmonic at -44 dBm. The detection program makes use of two

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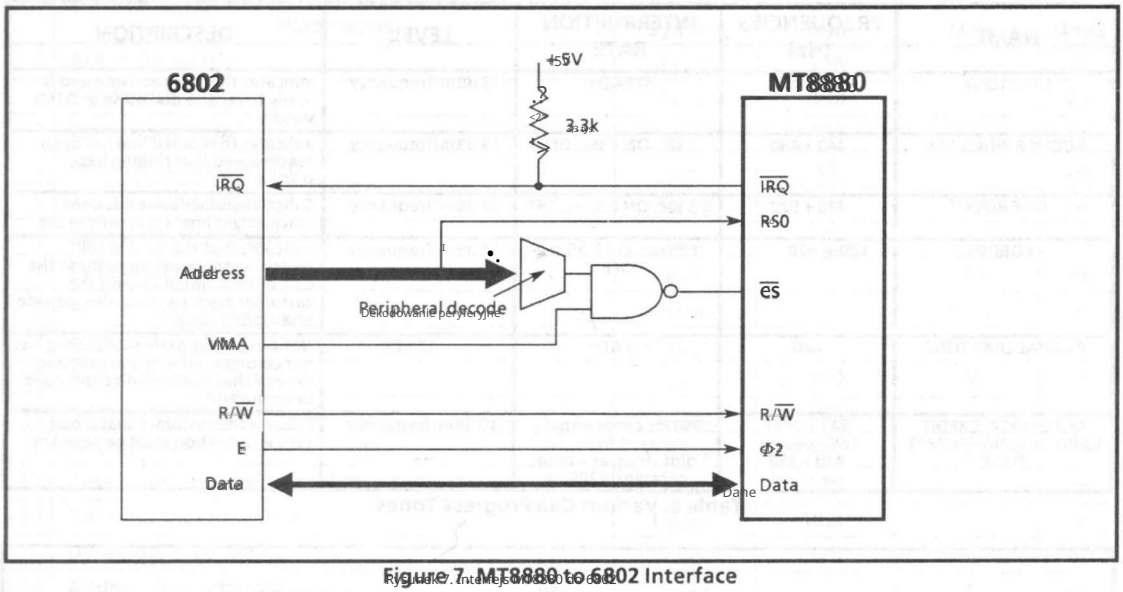

Figure 7. MT8880 to 6802 Interface

Rysunek 7. Interfejs MT8880 do 6802

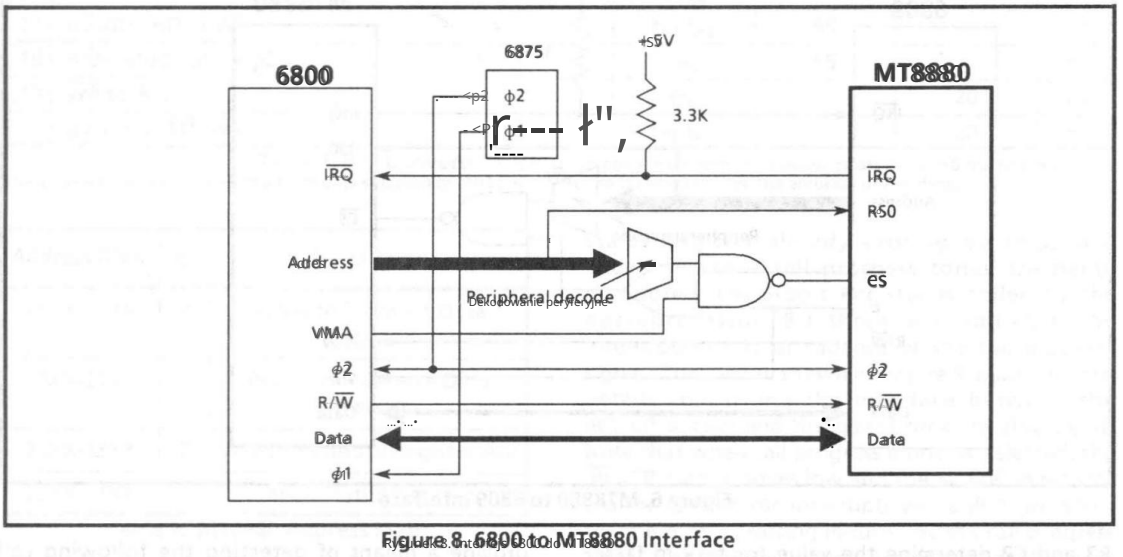

Figure 8. 6800 to MT8880 Interface

Rysunek 8. Interfejs 6800 do MT8880

software counters in real time and as such the values shown in the program for counter verification limits must be tailored for every system due to the different clock rates and various microprocessor systems. Counter one monitors the time that the tone was interrupted (tone absent) and counter two monitors the time the tone was present. The two resulting counts are compared against the upper and lower limits initially specified in the program. These limits were found experimentally by checking the average count and then assigning suitable tolerances. An error counter allows some error before resetting each counter and an error from the identification register. Reference to the flowchart in Figure 11 will clarify details.

3.3 Voice Detection Using the MT8880

Voice signals can, in fact, be detected with the MT8880. The fact that voice signals are concentrated in the 500 Hz region (on the average), allows these signals to be detected using the Call Progress mode. A very useful application for this system is in telemarketing systems that must detect when the called party has answered. The fact that most people usually respond with the word "Hello" or some other short response can be used as a criterion to indicate that the called party has gone off-hook and is waiting for response. The speech detection is accomplished in exactly the same way as other call progress tones with the only difference

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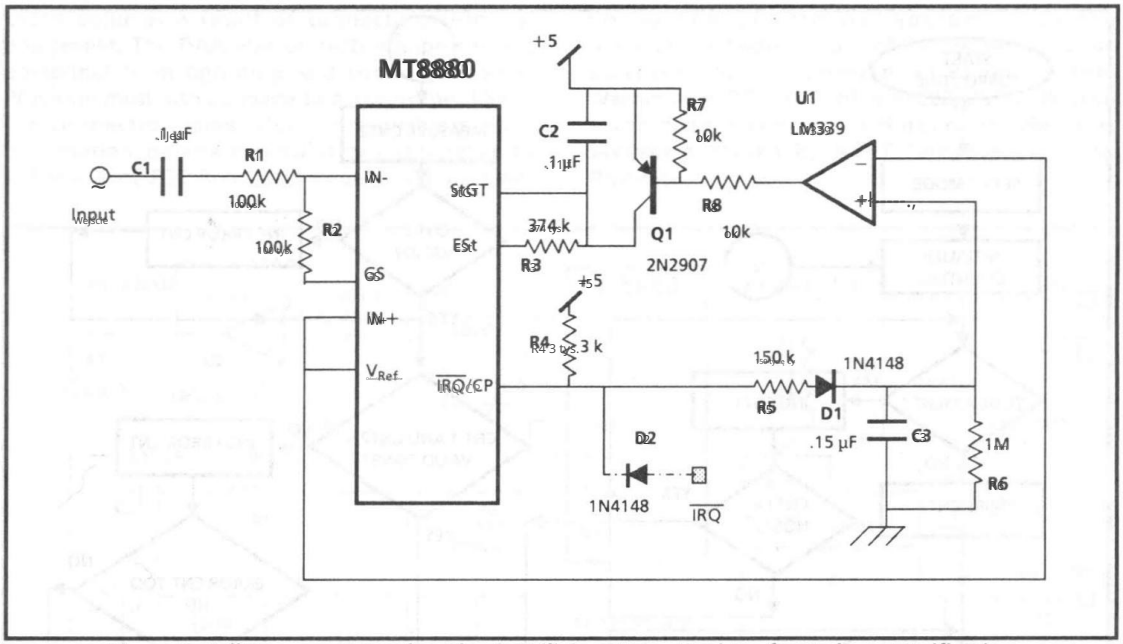

Figure 9. Call Progress Detection Circuit Utilizing Status Register for Cadence Verification

Rysunek 9. Obwód CallProgressDetection wykorzystujący rejestr ustawień do weryfikacji rytmu

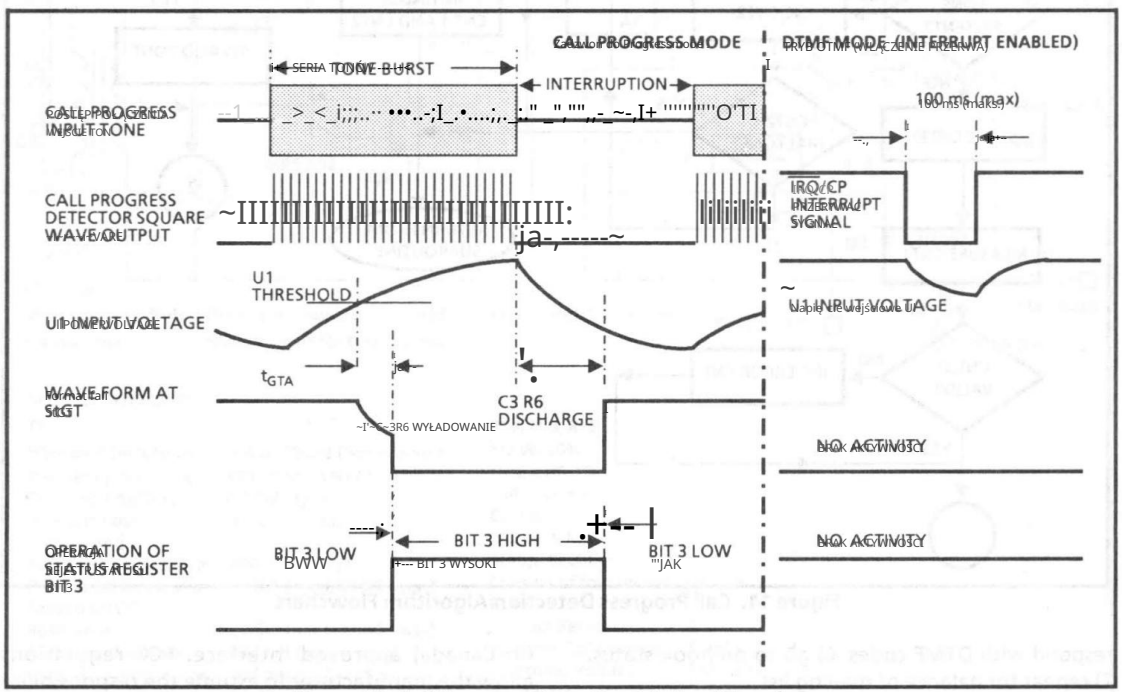

Figure 10. Call Progress Detection Timing Waveforms

Rysunek 10. Przebieg czasowy CallProgressDetection

being the accept/reject limits in the detection algorithm. The detection algorithm shown in Appendix 1 incorporates the voice detection function and can correctly detect "hello" with a 90% success rate. A typical scenerio using this

technika ta obejmowałaby: 1) sprawdzenie sygnału wybierania, 2) automatyczne wybieranie sygnałów DTMF, 3) monitorowanie tonu postępu połączenia, 4) wysłanie nagranej wcześniej wiadomości przedzwonowej jeśli odbiorca połączenia odpowie „cześć" 5) poproszenie klienta o

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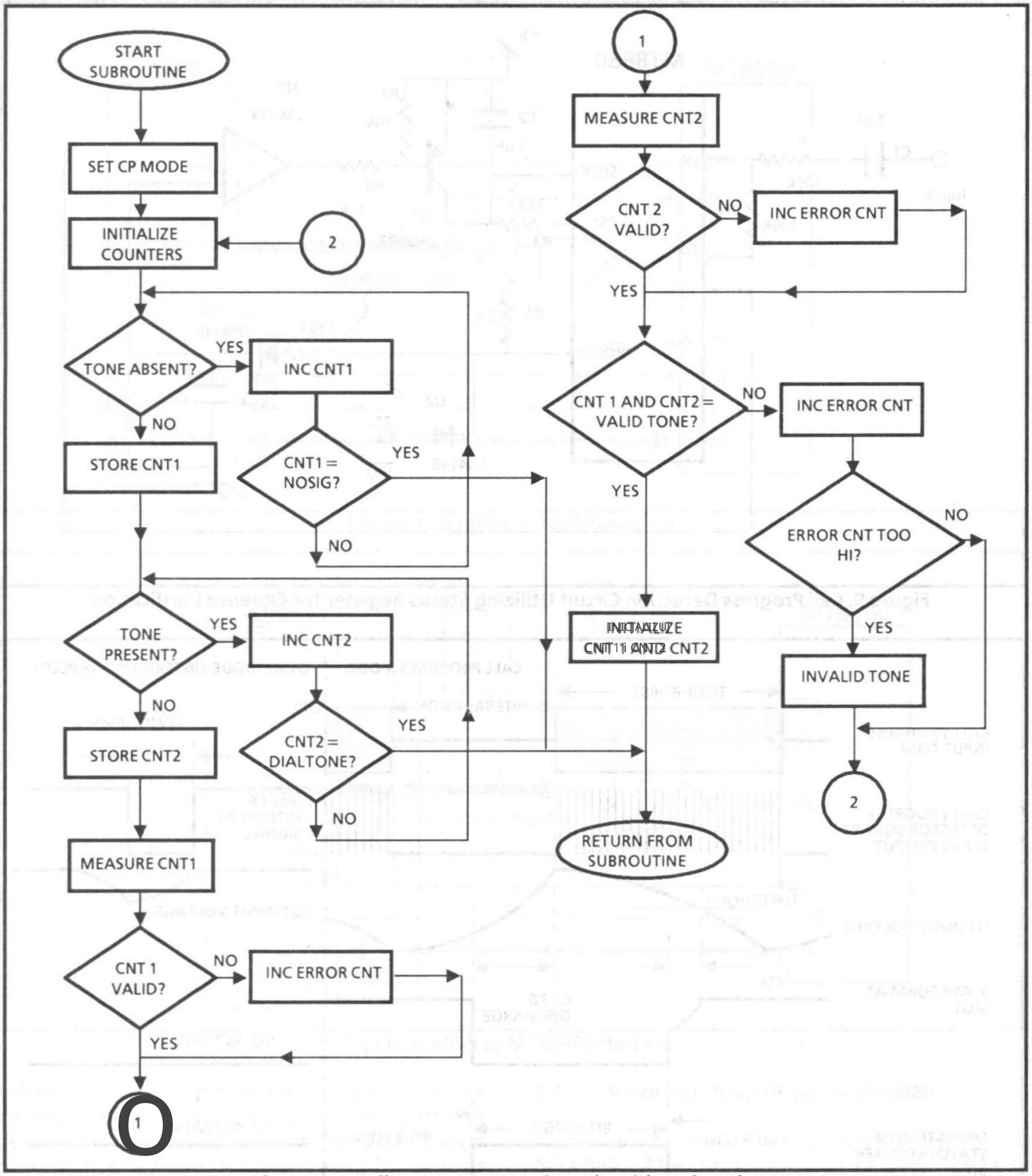

Figure 11. Call Progress Detection Algorithm Flowchart

respond with DTMF codes. 6) go to on hook status. 7) repeat for balance of mailing list.

4.0 Simple Telephone Line Interface

Many applications employing the MT8880 require an interface to the telephone line to provide access to the outside world. A system which connects to the telephone network must employ an FCC or DOC (in Canada) approved interface. FCC regulations allow the manufacturer to assume the responsibility of providing a protection and interface circuit commonly referred to as a data access arrangement (DAA). Historically, the manufacturer was not given this freedom and had to purchase a DAA from the telephone company. FCC Rules and Regulations part 68 provides a set of standards designed to protect the network from possible damage that

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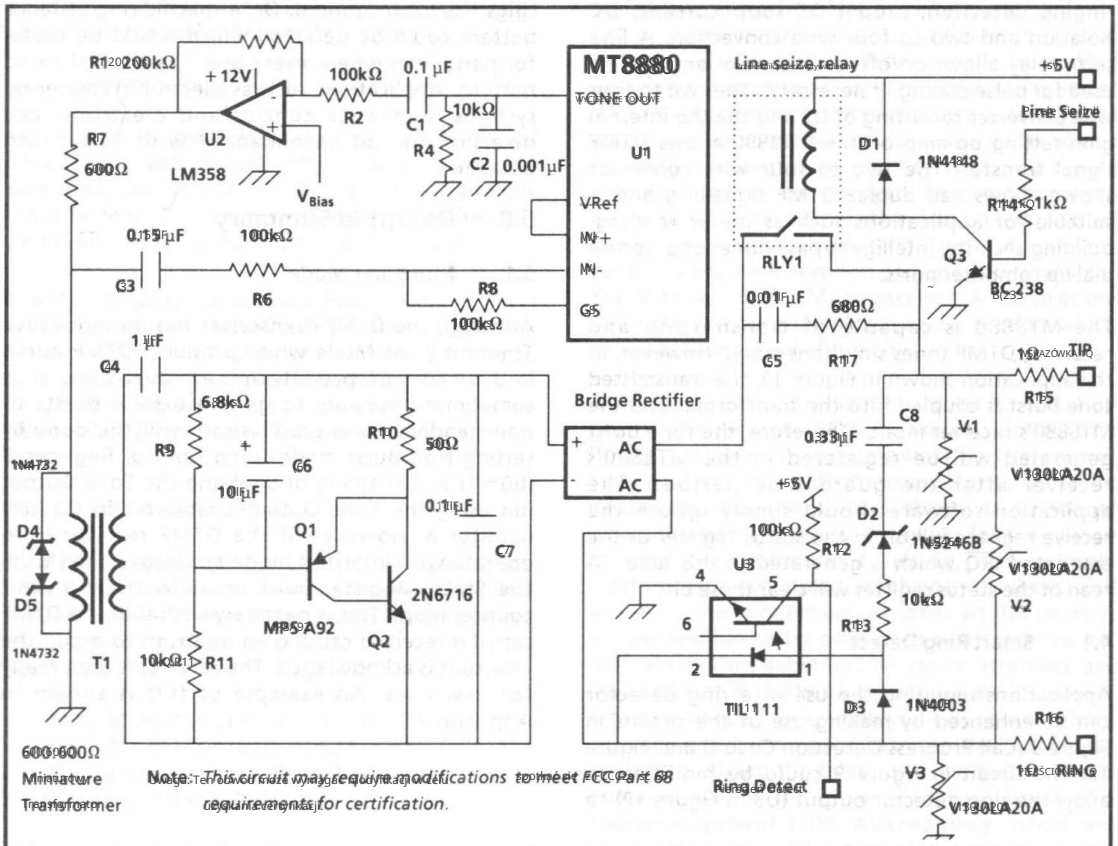
could vary as a result of connecting terminal equipment. The DAA also protects equipment and personnel from hazardous conditions.

Revision must also be made to allow proper billing for connection. Project Designers wishing more information on these requirements should refer to Volume 2 of FCC Rules and Regulations part 68: Connection of terminal equipment to the telephone network. A copy of the document can be obtained from the Government Printing Office, Washington, DC 20402 (202) 783-3238. Also another useful reference is Notes on the Network, Section 4, issued by AT&T Network Planning Division.



Note: This circuit may require modifications to meet FCC Part 68 requirements for certification.

COMPONENTS LIST:

T1
Harmonic Distortion: 1% at 300Hz (0dBm input)
Frequency Response: 300 Hz to 5 kHz (2dB)
Coupling Coefficient: 0.9993 (typ)
Insertion Loss: 2.0 dB (at 1kHz)
Primary and Secondary Impedance: 600Ω (at 1kHz)
Primary DC Resistance: 38.0Ω (min), 43.0Ω (max)
Secondary DC Resistance: 31.6Ω (min), 33.5Ω (max)
Primary Inductance: 462 mH (at Q = 48.6)
Secondary Inductance: 465 mH (at Q = 45.9)
Longitudinal Balance: 53 dB

U1
MITEL MT8880D/MH *Transceiver*

R1, R2, R6, R8
1/4W, 1%

R4, R7, R9, R11, R12, R13, R14, R17
1/4W, 10%

R10, R15, R16
1/2W, 10%

C4, C6, C6, C7
100 Volt, 5%

C5, C8
200 Volt, 5%

Bridge Rectifier
Consists of four diodes 1N4003

RLY1
Contact Resistance: 0.5Ω
Nominal Coil Voltage: 5 Volts
Switching Voltage: 250 Volts

V1, V2, V3
Continuous Voltage: 130 Volt (RMS)
Energy: 70 Joules (10 x 1000 µs)
Varistor Voltage: 200 Volts (min @ DC)
Clamp Voltage: 340 Volts (100 Amps, 8/20µs)
Capacitance: 1000 pF

Figure 12. Telephone Line Interface

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Although a DAA can be purchased separately, the cost of such a device usually equates to a high proportion of the overall cost of the application. The circuit shown in Figure 12 is a DAA which is optimized for the MT8880 DTMF transceiver. Although the circuit has not gone through the FCC approval cycle, it should meet the necessary approval requirements. The circuit provides transmission, ringing detection, proper DC loop current DC isolation and two to four wire conversion. A line seize relay allows on/off hook control and can be used for pulse dialing if necessary. The two to four wire converter consists of U2 and the internal gain setting op-amp on the MT8880 allows DTMF signal transfer. The two to four wire converter shown allows half duplex DTMF signalling and is suitable for applications such as meter reading, building security, intelligent payphones and secure dial up computer ports.

The MT8880 is capable of transmitting and receiving DTMF tones simultaneously however, in the application shown in Figure 12, the transmitted tone burst is coupled into the receiver and the MT8880's receiver will be triggered. Therefore, the tone burst generated will be registered by the MT8880's receiver after the transmit time. The application software should simply ignore the receive register full bit in the status register or the associated IRQ which is generated at this time. A read of the status register will clear these bits.

4.1 Smart Ring Detect

Applications requiring the use of a ring detector can be enhanced by making use of the circuit shown in Figure 9 (Call Progress Detection Circuit) and Figure 12. The circuit in Figure 9 could be modified to allow the ring detector output (U3 in Figure 12) to trigger the Steering/Guard Time circuitry normally used for the DTMF receiver. This would provide a means of detecting the presence of ringing voltage with the MT8880 (in Call Progress mode) by monitoring the state of bit 3 in the Status Register. A counter in the application software could monitor the number of ring bursts and cause an off hook condition when a predetermined value was counted. Or, specific ring cadence pattern could be detected which would be useful for party lines where several systems share a common pair. Applications such as electronic answering systems, voice mail, computer control and electronic call diversion can all be enhanced with smart ring detection.

5.0 Podsumowanie projektu

5.1 Tryb Normal Burst Mode

Although the DTMF Transceiver has an innovative Transmit Burst Mode which produces DTMF bursts and pauses of pre-determined duration, there are sometimes necessary to generate tone bursts of non-standard duration. This can easily be done by setting Normal mode (bit D3 = 0) and enabling or disabling the Tone Output pin using the Tone Output enable bit (bit D2) in Control Register A. However, if the DTMF receiver is to operate with interrupts enabled, a read from the Status Register must occur in the transmit counter loop. This is necessary such that if a DTMF signal is received causing an interrupt to occur, the interrupt is acknowledged. The receiver is then ready for new data. An example of this is shown in Appendix 2.

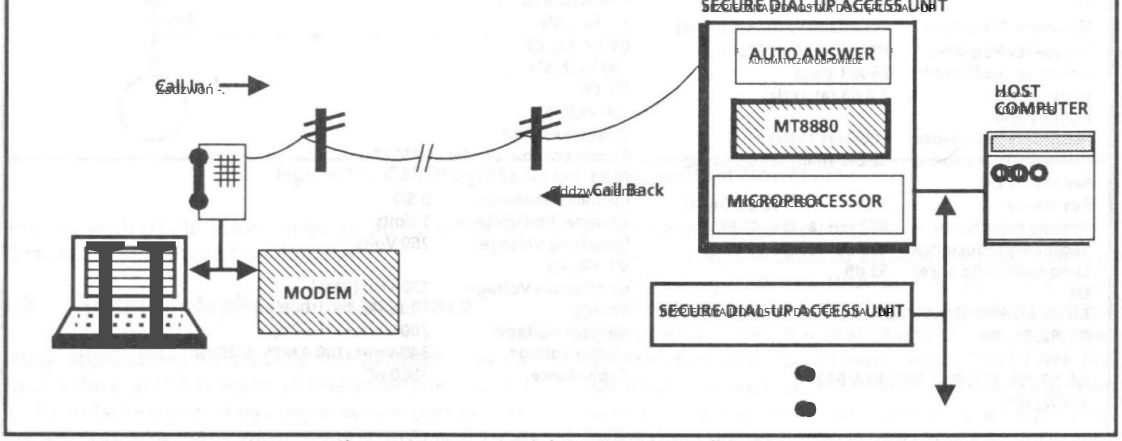

Figure 13. Secure Dial Up Access Application

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5.2 Oscylator Clock

MT8880 wykorzystuje obwód oscylatora on chip, który jest uzupełniony o kryształ 3,5795 MHz. Wiele urządzeń może być sterowanych jednym źródłem zegara poprzez sterowanie OSC 1 na wszystkich urządzeniach. Sterownik powinien być sprzężony pojemnościowo przez kondensator 0,01 f. Alternatywnie, urządzenia mogą być połączone szeregowo (z ograniczeniami), tak aby pierwsze urządzenie w łańcuchu było głównym oscylatorem.

5.3 Zasilanie

Należy podjąć kroki poprzez zastosowanie kondensatorów odsprzęgających lub innych środków w celu zmniejszenia szumu zasilania w urządzeniu. Jest to szczególnie ważne w trybie Call Progress, ponieważ szum może powodować losowe przełączanie na wyjściu IRQ/CP.

Próg wykrywania Call Progress jest ustawiony na poziomie, który jest określony przez histerezę wyzwalacza Schmitta używanego w filtrze podziału pasma DTMF low group. Poziom ten jest dość niski i nie można go regulować. Jednak można uzyskać pewną dostosowanie, zmieniając wzmocnienie układu na chipie. wzmacniacz.

5.4 Resetowanie oprogramowania

Reset oprogramowania jest konieczny po włączeniu zasilania, ponieważ urządzenie może się uruchomić w nieznanym stanie. Sekwencja jest dość prosta i powinna być stosowana na początku wszystkich programów.

Resetuj sekwencję:

Wpisz 00(hex) do REJESTRU KONTROLNEGO
Wpisz 00(hex) do REJESTRU KONTROLNEGO
Wpisz 08(hex) do REJESTRU KONTROLNEGO
Wpisz 00(hex) do REJESTRU KONTROLNEGO

5.5 Wykorzystanie Fazy 2 (ϕ2) Wejście

Architektura magistrali jest zoptymalizowana dla mikroprocesora MOTOROLA 6800 i jako taka wymaga sygnału Fazy 2. Sygnał ten jest nie tylko niezbędny do przesyłania danych, ale musi być również obecny, aby zaktualizować rejestr stanu. Jeśli dane nie są przesyłane, okres zegara fazy 2 można wydłużyć do 1 ms. Okres dłuższy niż 1 ms może skutkować utratą danych.

5.6 Opóźnienie CP Mode do DTMF Mode

Przejście z trybu Call Progress do trybu DTMF wymaga skończonego czasu, który jest częściowo określany przez obwody filtrujące. Aplikacje, które wymagają, aby sygnały DTMF były odbierane bezpośrednio po wyjściu z trybu Call Progress, co może mieć miejsce w przypadku wykrywania inteligentnego pierścienia, wymagają co najmniej 10 ms, gdy przełączają się na tryb DTMF, aby mieć pewność, że żadne dane DTMF nie zostaną utracone.

6.0 ZASTOSOWANIA

6.1 Secure Port Dial-Up dla modemów

Coraz większe jest zainteresowanie zapewnieniem dodatkowej ochrony systemom komputerowym. Istnieje wiele aspektów, które należy wziąć pod uwagę w całościowym systemie bezpieczeństwa, od technik bezpiecznego systemu operacyjnego po bezpieczne systemy zarządzania bazą danych. Zorientowany sprzętowo bezpieczny system dostępu i systemy wymienione powyżej można połączyć, aby uzyskać wysoce bezpieczną sieć. Zorientowane sprzętowo bezpieczne systemy dostępu stają się popularne w wyniku zwiększonego wykorzystania komputerów opartych na mikroprocesorach do uzyskiwania dostępu do systemów sieciowych za pośrednictwem łączy telefonicznych dial-up.

Nadajnik-odbiornik DTMF MT8880 może stanowić serce produktu umożliwiającego oddzwanianie i uzyskiwanie dostępu do połączeń telefonicznych, co gwarantuje wysoki poziom bezpieczeństwa.

Popularną metodą ograniczania dostępu do portu dial-up w przeszłości było po prostu powstrzymanie się od podawania numeru telefonu. Działanie to z pewnością ograniczy nadużywanie komputera do pewnego stopnia, ale może powodować problemy dla personelu, który powinien mieć do niego dostęp. Jednak dla osoby poszukującej komputera do nadużycia, jest to prosta sprawa, aby wybrać kolejne numery telefonów w poszukiwaniu operatora modemu. W tym momencie możliwe jest wypróbowanie haseł lub próba obejścia schematów szyfrowania. W miarę podejmowania kolejnych prób, prawdopodobieństwo uzyskania dostępu wzrasta.

Dość nowy schemat wykorzystuje protokół wywołania zwrotnego, w którym jednostka podłączona między modemem (po stronie hosta) a linią telefoniczną automatycznie odpowiada na przychodzące połączenie bez tonu potwierdzenia. Alternatywnie, gdy odbierane jest połączenie, może zostać wydany fałszywy sygnał zajętości, tak aby osoby nieupoważnione uwierzyły, że linia jest zajęta.

Niezależnie od użytego schematu, po odebraniu połączenia przez hosta, kod dostępu jest wprowadzany za pomocą sygnalizacji DTMF. Po wprowadzeniu kodu, jednostka bezpiecznego dostępu przechodzi na widełki. Po dopasowaniu kodu dostępu do zaprogramowanego numeru telefonu, jednostka bezpieczeństwa jest zwracana, w którym to momencie następuje normalna aktywność uzgadniania modemu, po której następuje transmisja danych. Nieco inny schemat, który pozwala użytkownikowi na dowolną zmianę lokalizacji, obejmuje użycie zakodowanego numeru telefonu, który jest wprowadzany po kodzie dostępu. Jednostka bezpiecznego dostępu dekoduje numer telefonu i wykonuje połączenie zwrotne do tej lokalizacji.

Próby uzyskania dostępu przez nieupoważniony personel mogą wywołać stan alarmowy, co spowoduje powiadomienie operatora systemu i podjęcie odpowiednich działań.

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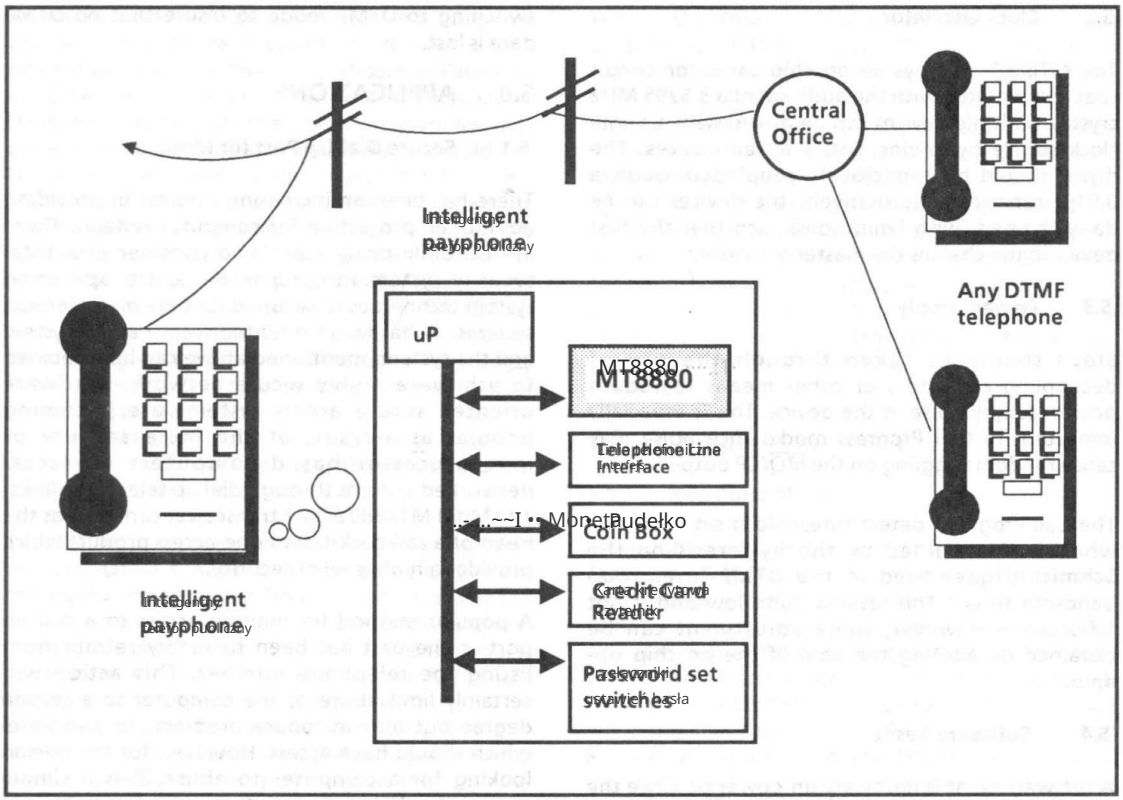

Figure 14. Program Your Own Rates With Intelligent Payphone

action taken. A data switch serving a large network could be fitted with security access circuitry at each dial up port providing a high level of security for sensitive data. Also users of smaller networks such as those found in real estate or sales applications could benefit from added security. Figure 13 shows a typical arrangement.

6.2 Intelligent Payphone

Intelligent payphones can be installed in such places as variety or convenience stores, bowling alleys and other suitable locations where they can be used as a source of income for the owner. Persons wanting to use the phone must deposit the fee as programmed by an authorized user. The MT8880 can play a key role in such an intelligent payphone system and is illustrated in Figure 14.

Any person having a telephone number and password for a specific intelligent payphone can do such things as program the calling rates, check the amount of coin in the box or even check to see if the phone has been vandalized. An FCC approved data access arrangement must be used to connect the system to telephone lines with an automatic ringdetect circuit providing incoming call signal. Upon receiving an incoming call, the software could be set up such that the payphone issues false ringback tones or busy tones to discourage unauthorized users. Personnel with the password however, could simply enter DTMF codes over the false call progress tones to gain access. Once the password has been correctly entered (from any DTMF phone) commands can then be entered.

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APPENDIX 1
Call Progress and Voice Detection Algorithm

```
1                *
2                * THIS PROGRAM PROVIDES AN ALGORITHM TO CHECK THE
3                * CADENCE OF CALL PROGRESS SIGNALS. THE CALL PROGRESS DETECT CIRCUIT
4                * MUST BE USED. THE CIRCUIT UTILIZES A CHARGE PUMP WHICH FEEDS INTO
5                * THE ANALOG GUARD TIME CIRCUIT NORMALLY USED FOR DTMF. WHEN IN
6                * DTMF MODE, TRANSISTOR Q1 IS IN A HIGH IMPEDANCE STATE
7                * THIS NOT AFFECTING THE NORMAL OPERATION OF THE GUARD TIME CIRCUIT.
8                * IE OPERATING IN INTERRUPT MODE, PQ/C2 IS NORMALLY HIGH, HOWEVER
9                * INTERRUPTS MUST BE SERVICED WITHIN 200MS OR THE DTMF TIMING WILL BE
10               * TEMPORARILY CORRUPTED. THIS INTERRUPT SERVICE TIME CAN BE ADJUSTED
11               * WITH C3 AND R6.
12               * IN PRACTICE THE STATUS REGISTER (BIT 3) IS POLLED LOOKING FOR THE
13               * CONDITION OF BIT 3. THIS PROGRAM HAS TWO COUNTERS. COUNTER 1 DETERMINES
14               * HOW LONG THERE IS AN ABSENCE OF ENERGY IN THE PASSBAND AND COUNTER 2
15               * DETERMINES HOW LONG THERE IS A PRESENCE OF ENERGY IN THE PASSBAND.
16               * AN ERROR COUNTER ALLOWS ERRORS FROM THE SIGNAL ABSENT AND SIGNAL PRESENT
17               * COUNTERS IN ADDITION TO THE COUNT MATCH REGISTER.
18               * THE RESULT OF THE DETECT ALGORITHM IS PRINTED ON THE CRT
19               * ALSO, A FORM SPEECH DETECTION ALGORITHM INDICATES WHEN THE WORD 'HELLO'
20               * HAS BEEN RECEIVED AT THE INPUT OF THE MT8880.
21               *
22   4400        START EQU $4400
23   2000        TXRX EQU $2000
24   2001        CRSR EQU $2001
25   8662        CRLF EQU $8662
26   867B        HEX4 EQU $867B
27   8655        HEAD EQU $8655
28   8686        HEX2 EQU $8686
29   866E        SPACE2 EQU $866E
30               *                    MJR  MAR 1986
31               * CPVREF.LST
32   4400        ORG START
33               *
34               * PROGRESS TONE IDENTIFIER DATA
35               *
36   4400 A 86 00    LDAA #$00      DAA #$00
37   4402 A B7 479D  STAA REORDR     TONE 1 REORDER TONE
38   4405 A 86 01    LDAA #$01      DAA #$01
39   4407 A B7 479C  STAA RNGBK      TONE 2 RINGBACK TONE
40   440A A 86 02    LDAA #$02      DAA #$02
41   440C A B7 479B  STAA BUSY       TONE 3 BUSY TONE
42   440F A 86 03    LDAA #$03      DAA #$03
43   4411 A B7 479E  STAA DIALTN     TONE 4 DIAL TONE
44   4414 A 86 04    LDAA #$04      DAA #$04
45   4416 A B7 479F  STAA NOTONE     TONE 5 NO SIGNAL
46   4419 A 86 05    LDAA #$05      DAA #$05
47   441B A B7 47A0  STAA HELLO      TONE 6 HELLO
48               *
49               * ERROR COUNT
50               *
51   441E A C6 04    LDAB #$04      DAB #$04
52   4420 A B7 47A3  STAA ERRCNT
53               *
54               * TONE IDENTIFIERS
```

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```
                        *
4423 CE 0000    LDX #$0000
4426 FF 47A8    STX REORDX

MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2) 257.18-MAR-86 16:14:56 PAGE 2

4429 CE 0101    LDX #$0101
442C FF 47A6    STX RNGBKX
442F CE 0002    LDX #$0002
4432 FF 47A4    STX BUSYX
4435 CE 0303    LDX #$0303
4438 FF 47AA    STX DIALX
443B CE 0404    LDX #$0404
443E FF 47AC    STX NOTONX
4441 CE 0505    LDX #$0505
4444 FF 47AE    STX HELLOX
                *           TONE 1 PRESENT LIMITS
                *
4447 CE 0400    LDX #$0900      LOWER LIMIT
444A FF 4848    STX TLO1LL
444D CE 04FF    LDX #$04FF      UPPER LIMIT
4450 FF 484A    STX TLO1UL
                *
                *           TONE 1 ABSENT LIMITS
                *
4453 CE 0A00    LDX #$0500      LOWER LIMIT
4456 FF 484C    STX THI1LL
4459 CE 0C00    LDX #$0600      UPPER LIMIT
445C FF 484E    STX THI1UL
                *
                *           TONE 2 PRESENT LIMITS
                *
445F CE 6D00    LDX #$7200      LOWER LIMIT
4462 FF 4850    STX TLO2LL
4465 CE 6EFF    LDX #$74FF      UPPER LIMIT
4468 FF 4852    STX TLO2UL
                *
                *           TONE 2 ABSENT LIMITS
                *
446B CE 4050    LDX #$3B00      LOWER LIMIT
446E FF 4854    STX THI2LL
4471 CE 4255    LDX #$3DFF      UPPER LIMIT
4474 FF 4856    STX THI2UL
                *           TONE 3 PRESENT LIMITS
                *
4477 CE 0400    LDX #$0900      LOWER LIMIT
447A FF 4858    STX TLO3LL
447D CE 04FF    LDX #$04FF      UPPER LIMIT
4480 FF 485A    STX TLO3UL
                *
                *           TONE 3 ABSENT LIMITS
                *
4483 CE 3A00    LDX #$0E00      LOWER LIMIT
4486 FF 485C    STX THI3LL
4489 CE 1460    LDX #$0520      UPPER LIMIT
448C FF 485E    STX THI3UL
                *
                *           TONE 4 PRESENT LIMITS
                *
```

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```
448F A   CE 5000  LDX #$5000 ;LOWER LIMIT
4492 A   FF 4860  STX THI4LL
4495 A   CE 5010  LDX #$5010 ;UPPER LIMIT
4498 A   FF 4862  STX THI4UL

MODULE;   MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 3
               *
               *         NOTONE 5 - SIGNAL ABSENT LIMITS

               *
449B A   CE 9000  LDX #$9000
449E A   FF 4864  STX TLO5LL
44A1 A   CE 9010  LDX #$9010
44A4 A   FF 4866  STX TLO5UL
               *
               *
               *         HELLO 6 - SIGNAL PRESENT LIMIT
               *
44A7 A   CE 05BA  LDX #$05BA ;TONE 6 LOWER LIMIT
44AA A   FF 486C  STX THI6LL
44AD A   CE 0CFF  LDX #$08FF ;TONE 6 UPPER LIMIT
44B0 A   FF 486E  STX THI6UL
               *
               *
               *         HELLO 6 SIGNAL ABSENT LIMIT
               *
44B3 A   CE 1000  LDX #$1000 ;TONE 6 LOWER LIMIT
44B6 A   FF 4868  STX TLO6LL
44B9 A   CE 8000  LDX #$8000 ;TONE 6 UPPER LIMIT
44BC A   FF 486A  STX TLO6UL
               *
               * RESET
               *
44BF A   86 00    LDAA #$00
44C1 A   B7 2001  STAA CRSR
44C4 A   B7 2001  STAA CRSR
44C7 A   86 08    LDAA #$08
44C9 A   B7 2001  STAA CRSR
44CC A   86 00    LDAA #$00
44CE A   B7 2001  STAA CRSR
               *
               * CALL PROGRESS MODE WITH IRQ ENABLED
               *
44D1 A   86 06    LDAA #$06
44D3 A   B7 2001  STAA CRSR
               *
               * MAIN PROGRAM
               *
44D6 A   BD 44FA  JSR RESET
44D9 A   BD 4516  JSR CHECB3
44DC A   BD 4536  JSR PRIME
44DF A   BD 452C  MORBINC JSR MORB3
44E2 A   BD 4516  JSR CHECB3
44E5 A   BD 45B3  JSR MEASLO
44E8 A   BD 4548  JSR MEASHI
44EB A   BD 4621  JSR MATCH
44EE A   BD 4689  JSR CHERR
44F1 A   BD 469F  JSR PRINT
44F4 A   BD 4536  JSR PRIME
```

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```
4457 A E7 44DF    CMP 44DF,MORINC
                  *
44FA A CE 0000    RESET LDX #$0000
44FD A FF 4844    STX CNT1
4500 A FF 4846    STX CNT2

MODULE;  MICROBENCH 6800 CROSS ASSEMBLER (V2) 257-18-MAR-86 16:14:56 PAGE 4

                  *
                  * SET ERROR COUNTER
                  *
4503 A E6 47A3    LDAB ERRCNT
4506 A F7 47A1    STAB MATERR
4509 A 39         RTS
                  *
                  * START OF DETECT ALGORITHM
                  * COUNTER 1 CHECKS TO SEE HOW LONG
                  * BIT 3 IS HI (ABSENCE OF SIGNAL)
                  *
450A A FE 4844    INCCNT LDX CNT1
450D A 08         INX
450E A FF 4844    STX CNT1
4511 A 8C 4862    CPX THI4UL
4514 A 22 32      BHI MEASHI
                  *
4516 A F6 2001    CHECB3 LDAB CRSR
4519 A C4 08      ANDB #$08
451B A C1 08      CMPB #$08
451D A 27 EB      BEQ INCCNT
451F A 39         RTS
                  *
                  *
                  *
                  * COUNTER 2 CHECKS TO SEE HOW LONG ENERGY IS PRESENT
                  *
4520 A FE 4846    MORCNT LDX CNT2
4523 A 08         INX
4524 A FF 4846    STX CNT2
4527 A 8C 4866    CPX TLO5UL
452A A 22 1A      BHI PATCH1
                  *
452C A B6 2001    MORCB3 LDAA CRSR
452F A 84 08      ANDA #$08
4531 A 81 08      CMPA #$08
4533 A 26 EB      BNE MORCNT
4535 A 39         RTS
                  *
4536 A CE 0000    PRIME LDX #$0000
4539 A FF 4844    STX CNT1
453C A FF 4846    STX CNT2
453F A CE FFFF    LDX #$FFFF
4542 A FF 4842    STX MATCHA
4545 A 39         RTS
                  *
                  *
4546 A 20 6B      PATCH1 BRA MEASLO
                  *
                  * COMPARE THE LOWER LIMIT AND UPPER LIMIT TO CNT1 WHICH
                  * CONTAINS THE TIME THE PROGRESS TONE WAS PRESENT
```

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```
                        *
4548 A 4844 EE 4844 MEASHI LDX CNT1
                        *
454B A 8D 86 7B BD 867B JSR HEX4
                        *
454E A 4844 FE 4844 LDX CNT1
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 18-MAR-86 16:14:56 PAGE 5

```
4551 A BC 484C CPX THI1LL
4554 A 27 17 BEQ CHH1UL
4556 A BC 4854 CPX THI2LL
4559 A 27 1A BEQ CHH2UL
455B A BC 485C CPX THI3LL
455E A 27 1D BEQ CHH3UL
4560 A BC 4860 CPX THI4LL ;ONLY CHECK THE LOWER LIMIT TONE PRESENT FOR DIALTONE
4563 A 27 3D BEQ T4HIID
4565 A BC 4866 CPX THI6LL
4568 A 27 1B BEQ CHH6UL
456A A 7E 4676 JMP NOQUD
                        *
456D A BC 484E CPX THI1UL
4570 A 23 1B BLS T1HIID
4572 A 7E 4556 JMP TH2LL
4575 A BC 485E CPX THI2UL
4578 A 23 1A BLS T2HIID
457A A 7E 4558 JMP TH3LL
457D A BC 485E CPX THI3UL
4580 A 23 19 BLS T3HIID
4582 A 7E 4560 JMP TH4LL
4585 A BC 486E CPX THI6UL
4588 A 23 22 BLS T6HIID
458A A 7E 4676 JMP NOQUD
                        *
                        *IDENTIFY THE MEASURED VALUE
                        *
458D A 86 79 LDAA REORDR
4590 A B7 4843 STAA MATCHB
4593 A 39 RTS
                        *
4594 A 86 79 LDAA RNGBK
4597 A B7 4843 STAA MATCHB
459A A 39 RTS
                        *
459B A 86 79 LDAA BUSY
459D A B7 4843 STAA MATCHB
45A0 A 39 RTS
                        *
45A2 A 86 79 LDAA DIALTN
45A5 A B7 4842 STAA MATCHA
45A8 A B7 4843 STAA MATCHB ;STORE IN MATCHA AND MATCHB SINCE ONLY CHECKING PRESENT TIME
45AB A 39 RTS
                        *
45AC A 86 79 LDAA HELLO
45AF A B7 4843 STAA MATCHB
45B2 A 39 RTS
                        *
                        *COMPARE THE LOWER LIMIT AND UPPER LIMIT TO CNT2
                        *WHICH CONTAINS THE TIME THE PROGRESS TONE WAS ABSENT
```

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```
                 *
45B3 A FE  4846 MEASLO LDX CNT2
                 *
45B6 A BD  867B        JSR HEX4
45B9 A BD  866E        JSR SPACE2
                 *
45BC A FE  4846        LDX CNT2
```

MODULE;   MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 18-MAR-86 16:14:56 PAGE 6

```
45BF A BC  4848        CPX TLO1LL
45C2 A 22  17          BHI CHL1UL
45C4 A BC  4850 T2LL   CPX TLO2LL
45C7 A 22  1A          BHI CHL2UL
45C9 A BC  4858 T3LL   CPX TLO3LL
45CC A 22  1D          BHI CHL3UL
45CE A BC  4864 T5LL   CPX TLO5LL
45D1 A 22  3D          BHI T5LOID
45D3 A BC  4868 T6LL   CPX TLO6LL
45D6 A 22  1B          BHI CHL6UL
45D8 A 7E  4676        JMP NONID
                 *
45DB A BC  484A CHL1UL CPX TLO1UL
45DE A 23  1B          BLS T1LOID
45E0 A 7E  45C4        JMP TL2LL
45E3 A BC  4852 CHL2UL CPX TLO2UL
45E6 A 23  1A          BLS T2LOID
45E8 A 7E  45C9        JMP TL3LL
45EB A BC  485A CHL3UL CPX TLO3UL
45EE A 23  19          BLS T3LOID
45F0 A 7E  45CE        JMP TL5LL
45F3 A BC  486A CHL6UL CPX TLO6UL
45F6 A 23  22          BLS T6LOID
45F8 A 7E  4676        JMP NONID
                 *
                 * IDENTIFY THE MEASURED VALUE
                 *
45FB A B6  479D T1LOID LDAA REORDR
45FE A B7  4842        STAA MATCHA
4601 A 39              RTS
                 *
4602 A B6  479C T2LOID LDAA RNGBK
4605 A B7  4842        STAA MATCHA
4608 A 39              RTS
                 *
4609 A B6  479B T3LOID LDAA BUSY
460C A B7  4842        STAA MATCHA
460F A 39              RTS
                 *
4610 A B6  479F T5LOID LDAA NOTONE
4613 A B7  4842        STAA MATCHA
4616 A B7  4843        STAA MATCHB
4619 A 39              RTS
                 *
461A A B6  47A0 T6LOID LDAA HELLO
461D A B7  4842        STAA MATCHA
4620 A 39              RTS
                 *
4621 A FE  4842 MATCH  LDX MATCHA
```

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```
50  4624 81 47AB CPX BUSYX  47A4 CPX BUSYX
51  4627 27 IC BEQ ZAJEC    BEQ BUSY1
52  4629 81 47AB CPX RNGBKX 47A6 CPX RNGBKX
53  462C 27 20 BEQ RNGBK1   BEQ RNGBK1
54  462E 81 47AB CPX REORDX 47A8 CPX REORDX
55  4631 27 25 BEQ REORD1   BEQ REORD1
56  4633 81 47AB CPX DIALX  47AA CPX DIALX
57  4636 27 2A BEQ DIALT1   BEQ DIALT1

MODULE; MICROENGH 6800 CROSS ASSEMBLER V2.1 257 18-MAR-86 16:14:56 PAGE 7

1   4638 81 47AC CPX NOTONX 47AC CPX NOTONX
2   463A 27 2F BEQ NOTON1   BEQ NOTON1
3   463D 81 47AE CPX HELLOX 47AE CPX HELLOX
4   4640 27 3D BEQ HELLO1   BEQ HELLO1
5   4642 7E 4678 JMP NONID  4678 JMP NONID
6               *
7               *
8               *
9   4645 CE 46A9 BUSY1 LDX  46A9 BUSY1 LDX #MSG1
10  4648 C6 02 LDAB #02     LDAB #$02
11  464A F7 47AF STAB MATERR STAB MATERR
12  464D 39         RTS     RTS
13  464E CE 46C0 RNGBK1 LDX 46C0 RNGBK1 LDX #MSG2
14  4651 F6 47A3 LDAB ERRCNT 47A3 LDAB ERRCNT
15  4654 F7 47AF STAB MATERR 47AF STAB MATERR
16  4657 39         RTS     RTS
17  4658 CE 46E5 REORD1 LDX 46E5 REORD1 LDX #MSG3
18  465B F6 47A3 LDAB ERRCNT 47A3 LDAB ERRCNT
19  465E F7 47AF STAB MATERR 47AF STAB MATERR
20  4661 39         RTS     RTS
21  4662 CE 470C DIALT1 LDX 470C DIALT1 LDX #MSG4
22  4665 F6 47A3 LDAB ERRCNT 47A3 LDAB ERRCNT
23  4668 F7 47AF STAB MATERR 47AF STAB MATERR
24  466B 39         RTS     RTS
25  466C CE 4740 NOTON1 LDX 4740 NOTON1 LDX #MSG5
26  466F F6 47A3 LDAB ERRCNT 47A3 LDAB ERRCNT
27  4672 F7 47A1 STAB MATERR 47A1 STAB MATERR
28  4675 39         RTS     RTS
29  4676 CE 474E NONID LDX  474E NONID LDX #MSG6
30  4679 C6 00 LDAB #00     LDAB #$00
31  467B F7 47A5 STAB ERFLAG 47A5 STAB ERFLAG
32  467E 39         RTS     RTS
33  467F CE 4770 HELLO1 LDX 4770 HELLO1 LDX #MSG7
34  4682 F6 47A3 LDAB ERRCNT 47A3 LDAB ERRCNT
35  4685 F7 47AF STAB MATERR 47AF STAB MATERR
36  4688 39         RTS     RTS
37  4689 F6 47AF HELLOX LDAB MATERR 47AF LDAB MATERR
38  468C F1 47A5 CMPB ERFLAG 47A5 CMPB ERFLAG
39  468F 27 04 BEQ UNIDEN   BLE UNIDEN
40  4691 7A 47AF DEC MATERR 47AF DEC MATERR
41  4694 39         RTS     RTS
42  4695 CE 477C UNIDEN LDX 477C UNIDEN LDX #INVLD
43  4698 F6 47A3 LDAB ERRCNT 47A3 LDAB ERRCNT
44  469B F7 47AF STAB MATERR 47AF STAB MATERR
45  469E 39         RTS     RTS
46              *
47  469F BD 8652 PRINT JSR CRLF 8652 PRINT JSR CRLF
48  46A2 BD 8695 JSR HEAD   8695 JSR HEAD
```

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```
46A5 A BD 866E      JSR SPACE2
46A8 A 39           RTS
              *
              *
              *
              *
              *
46A9 A 54 48  MSG1  FCC 'THE SIGNAL NOW PRESENT IS BUSY TONE'
46CC A 00           FCB 0
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 18-MAR-86 16:14:56 PAGE 8

```
46CD A 54 48  MSG2  FCC 'THE SIGNAL NOW PRESENT IS RINGBACK TONE'
46F4 A 00           FCB 0
46F5 A 54 48  MSG3  FCC 'THE SIGNAL NOW PRESENT IS REORDER TONE'
471B A 00           FCB 0
471C A 54 48  MSG4  FCC 'THE SIGNAL NOW PRESENT IS DIAL TONE'
473F A 00           FCB 0
4740 A 4E 4F  MSG5  FCC 'NO SIGNAL....
474D A 00           FCB 0
474E A 50 4C  MSG6  FCC 'PLEASE WAIT....PROCESSING TONE ID'
476F A 00           FCB 0
4770 A 48 45  MSG7  FCC 'HELLO'
4775 A 00           FCB 0
4776 A 54 48  INVLD FCC 'THE TONE NOW PRESENT IS UNIDENTIFIED'

479A A 00           FCB 0
              *
              *
479B A              BUSY RMB 1
479C A              RNGBK RMB 1
479D A              REORDR RMB 1
479E A              DIALTN RMB 1
479F A              NOTONE RMB 1
47A0 A              HELLO RMB 1
              *
47A1 A              MATERR RMB 1
47A2 A              ERFLAG RMB 1
47A3 A              ERRCNT RMB 1
              *
47A4 A              BUSYX RMB 2
47A6 A              RNGBKX RMB 2
47A8 A              REORDX RMB 2
47AA A              DIALX RMB 2
47AC A              NOTONX RMB 2
47AE A              HELLOX RMB 2
              *
47B0 A              RAMSG RMB 146
4842 A              MATCHA RMB 1
4843 A              MATCHB RMB 1
4844 A              CNT1 RMB 2 ;TONE ABSENT COUNT
4846 A              CNT2 RMB 2 ;TONE PRESENT COUNT
              *
4848 A              TLO1LL RMB 2 ;TONE 1 ABSENT LOWER LIMIT
484A A              TLO1UL RMB 2 ;TONE 1 ABSENT UPPER LIMIT
484C A              THI1LL RMB 2 ;TONE 1 PRESENT LOWER LIMIT
484E A              THI1UL RMB 2 ;TONE 1 PRESENT UPPER LIMIT
              *
4850 A              TLO2LL RMB 2 ;TONE 2 ABSENT LOWER LIMIT
```

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```
47   4852 A          TLO2UL RMB 2 ;TONE 3 ABSENT, UPPER LIMIT
48   4854 A          TLO2LL RMB 2 ;TONE 2 PRESENT, LOWER LIMIT
49   4856 A          TLO2UL RMB 2 ;TONE 2 PRESENT, UPPER LIMIT
50                   *
51   4858 A          TLO3LL RMB 2 ;TONE 3 ABSENT, LOWER LIMIT
52   485A A          TLO3UL RMB 2 ;TONE 3 ABSENT, UPPER LIMIT
53   485C A          TLH3LL RMB 2 ;TONE 3 PRESENT, LOWER LIMIT
54   485E A          TLH3UL RMB 2 ;TONE 3 PRESENT, UPPER LIMIT
55                   *
56   4860 A          TLH4LL RMB 2 ;TONE 4 PRESENT, LOWER LIMIT
57   4862 A          TLH4UL RMB 2 ;TONE 4 PRESENT, UPPER LIMIT

MODULE;  MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 - 18-MAR-86 16:14:56 PAGE 9

1                    *
2    4864 A          TLO5LL RMB 2 ;TONE ABSENT, LOWER LIMIT
3    4866 A          TLO5UL RMB 2 ;TONE ABSENT, UPPER LIMIT
4                    *
5    4868 A          TLO6LL RMB 2
6    486A A          TLO6UL RMB 2
7    486C A          TLH6LL RMB 2
8    486E A          TLH6UL RMB 2
9                    *
10                   END

MODULE;  MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 - 18-MAR-86 16:14:56 PAGE 10

SYMBOL TABLE

BUSY 479B BUSYX 47A4 BUSY1 4645
CHERR 4516 CHERR1 4689
CHH1UL 456D CHH2UL 4575 CHH3UL 457D CHH6UL 4585 CHL1UL 45DB
CHL2UL 45E3 CHL3UL 45EB CHL6UL 45F3 CNT 4844 CNT1 4844 CNT2 4846
CRLF 8662 CRSR1 2001 DIALTN 479E DIALT1 4662 DIALX 47AA
ERRCNT 47A2 ERRCN1 47A3 HEX0 8655 HEX1 47A0 HEX1X 47AE
HEX2 467F HEX2X 8686 HEX4 867B INCCNT 450A INCCN1 4776
MATCH 4621 MATCHA 4842 MATCHB 4843 MATERR 47A1 MEAS1 4548
MEAS2 45B3 MORB3 452C MORCNT 4520 MORIN1 44DF MSG1 46A9
MSG2 46CD MSG3 4655 MSG4 471C MSG5 4740 MSG6 474E
MSG7 4770 NONID 4676 NOTONE 479F NOTONX 47AC NOTON1 466C
PATCH1 4546 PRIME 4536 PRINT 4695 REORDA 47B0 REORDR 479D
REORDX 47A8 RESET 4658 RESET1 44FA RNGBK 479C RNGBKX 47A6
RNGBK1 464E SPACE2 8666 START = 4400 THH1LL 4844 THH1UL 484E
THH2LL 4854 THH2UL 4856 THH3LL 485C THH3UL 485E THH4LL 4860
THH4UL 4862 THH6LL 486C THH6UL 486E TIM2LL 4556 TIM3LL 455B
TLH4LL 4560 TLH6LL 4565 TLO1LL 4848 TLO1UL 484A TLO2LL 4850
TLO2UL 4852 TLO3LL 4858 TLO3UL 485A TLO5LL 4864 TLO5UL 4866
TLO6LL 4868 TLO6UL 486A TL2LL 45C4 TL3LL 45C9 TL5LL 45CE
TL6LL 45D3 TXRX = 2000 T1HHD 458D T1LOD 45FB T2HHD 4594
T2LOD 4602 T3HHD 4598 T3LOD 4609 T4HHD 45A2 T5LOD 4610
T6HHD 45AC T6LOD 461A UNDEF 4695 X% %

0000
ASCT 487000

MODULE
ERRORS DETECTED: 0

FREE CORE 8569. 8569. WORDS
)USR VSI 6800 MA6800 CPDEMOFIN/-SP = CPDEMOFIN/C
```

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MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2) 257.18-MAR-86 16:14:56 PAGE S-1
CROSS REFERENCE TABLE

BUSY 1-41 4-43 6-36 8-36# 6-36 8-17#
BUSY 4-51 6-51 7-9#
BUSYX 4-42 6-47 8-28# 6-50 8-28#
CHOCBC 3-43 3-43 3-46 3-46# 4-18#
CHERRY 3-50 3-37 7-37#
CHH1UL 5-32 5-13#
CHH2UL 5-34 5-16#
CHH3UL 5-36 5-19#
CHH6UL 5-40 5-22#
CHL1UL 6-32 6-13#
CHL2UL 6-34 6-16#
CHL3UL 6-36 6-19#
CHL6UL 6-40 6-22#
CNT1 3-56 3-56 4-44 4-42* 4-43 4-41* 8-34 8-41* 4-53 4-57 8-38#
CNT2 3-57 3-57 4-30 4-28* 5-42 5-30* 8-34 8-42* 5-52 5-57 8-39#
CREF 2-5 4-25# 7-47
CRSR 3-24# 3-24 3-29* 3-28* 3-33 3-29* 4-18 4-34 3-31* 3-33* 3-38* 4-18 4-34
DVALT 6-57 6-57 # 7-21#
DUMERNELEF 4-3U 1-5 3-10 5-40 8-20#
DVALDZ 2-6 6-56 ON 6-56 6-56 8-31#
ERRMAG 3-7 3-38 8-25#
ERRCNT 4-41 4-52* 7-14 4-42 7-26 7-14 7-48 7-18 7-22 7-26 7-34 7-43

8-26#
HEAD 1-21 4-27# 7-48
HELLO 4-47* 1-47 4-45 5-45 6-45 8-22#
HELLO 4-37 4-37#4 7-33#
HELLOX 7-3 8-3# 7-3 8-33#
HEX2 2-28# 4-28#
HEX4 4-26# 4-26# 4-54 4-55 5-54
INCONT 4-24 4-42# 4-21
MVLD 4-42 8-7 4-42 8-13#
MATCH1 6-39 6-49 6-49#
MATCHA 4-44 6-29 5-43 6-29 6-29# 6-33 6-49 6-37* 6-41* 6-46* 6-49

8-36#
MATCHB 2-29 2-29 5-37 5-32* 5-43 7-42* 8-42 8-42# 5-46* 6-42* 8-37#
MATERR 4-45 7-15 7-11 7-23 7-27* 7-39 7-37 7-23* 7-27* 7-35* 7-37

7-40 7-44 7-44# 8-24#
MEASH 3-48 3-48 4-16 4-53#
MEASL 3-47 3-47 5-52 4-48 5-52#
MORB 3-45 3-45 4-34#
MORGNT 4-28 4-28# 4-37
MORNG 3-45 3-45# 3-53
MSG1 7-9 7-56#
MSG2 7-13 8-1#
MSG3 7-17 8-3#
MSG4 7-21 8-5#
MSG5 7-25 8-7#
MSG6 7-29 8-9#
MSG7 7-33 8-11#
NONID 5-11 5-11 5-24 7-5 7-29# 6-24 7-5 7-29#
NOTNOT 7-23 7-25#

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NOTONE 1-45* 5-28 6-40 8-21#
NOTONX 2-8* 7-18-32 8-32#
PATCH 4-32 4-48#
PRMPT 3-44 3-52 4-40#
PRNT 3-54 7-47#
RAMSG 8-35#
RECORD 6-55 7-17#

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2) 257-18-MAR-86 16:14:56 PAGE S-2
CROSS REFERENCE TABLE

RECORD 6-28 8-19#
RECORX 6-54 8-30#
RESET 3-55#
RNGBK 5-32 6-32 8-18#
RNGBK1 7-13#
RNGBKX 6-52 8-29#
SPACE 5-55 7-49
START 1-32
TIMHI 5-28#
TIMOHI 6-28#
T2HIB 5-32#
T2OHIB 6-32#
T3HIB 5-36#
T3OHIB 6-36#
T4HIB 5-40#
T4OHIB 6-40#
T5HIB 5-45#
T5OHIB 6-45#
TH2LL 5-15
TH3LL 5-18
TH4LL 5-21
TH6LL 5-9#
THI1LL 2-21* 5-43#
THI1UL 5-13 8-44#
THV2LL 5-3 8-48#
THV2UL 5-16 8-49#
THW3LL 5-5 8-53#
THW3UL 5-19 8-54#
THW4LL 5-7 8-56#
THW4UL 4-15 8-57#
THW6LL 5-9 9-7#
THW6UL 5-22 9-8#
TIL2LL 6-15
TIL3LL 6-18
TIL5LL 6-21
TIL6LL 6-9#
TILO1LL 6-1 8-41#
TILO1UL 6-13 8-42#
TILO2LL 6-3 8-46#
TILO2UL 6-16 8-47#
TILO3LL 6-5 8-51#
TILO3UL 6-19 8-52#
TILO5LL 6-7 9-2#
TILO5UL 4-31 9-3#
TILO6LL 6-9 9-5#
TILO6UL 6-22 9-6#
TXRX 1-23#
UNDEF 7-42#

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APPENDIX 2
Transmitter in Non Burst mode, Receiver in Interrupt mode

```
MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2) 2.57 - APR-86 10:21:00 PAGE 1

1* THIS PROGRAM DEMONSTRATES THAT THE MT8880 CAN SEND TONE BURSTS IN THE NON
2* BURST MODE OF DURATION DETERMINED BY A SOFTWARE COUNTER LOOP. THE RECEIVER
3* IS SET TO OPERATE IN INTERRUPT MODE AND ON DETECTING A TONE PRODUCES AN
4* INTERRUPT WHICH MUST BE ACKNOWLEDGED BY A READ FROM THE STATUS REGISTER.
5*
6* EQUATES
7*
8    4500          START EQU $4500
9    2000          TXRX  EQU $2000
10   2001          CRSR  EQU $2001
11   8723          READ  EQU $8723
12   8655          HEAD  EQU $8655
13   5100          RAM   EQU $5100
14   8662          CRLF  EQU $8662
15   5000          DIGIT EQU $5000
16                 *
17   4500          ORG   START
18                 *
19                 * RESET
20                 *
21   4500 A6 00    LOOP  LDAA #$00
22   4502 B7 2001        STAA CRSR
23   4505 A6 00    LOOP  LDAA #$00
24   4507 B7 2001        STAA CRSR
25   450A A       LOOP  LDAA #$08
26   450C B7 2001        STAA CRSR
27   450F A       LOOP  LDAA #$00
28   4511 B7 2001        STAA CRSR
29                 *
30                 * ENABLE OUTPUT, IRQ, RSEL, NON BURST
31                 *
32   4514 A       LOOP  LDAA #$0D
33   4516 B7 2001        STAA CRSR
34   4519 A       LOOP  LDAA #$01
35   451B B7 2001        STAA CRSR
36                 *
37                 * WRITE MESSAGE
38                 *
39   451E BD 8662        JSR CRLF
40   4521 BD 8662        JSR CRLF
41   4524 CE 5100        LDX #MSG1
42   4527 BD 8655        JSR HEAD
43   452A BD 8662        JSR CRLF
44                 *
45                 * READ FROM THE KEYBOARD
46                 *
47   452D BD 8723  LOOP  JSR READ
48   4530 24 08          BCC LOOP
49   4532 B7 5000        STAA DIGIT
50   4535 B7 2000        STAA TXRX
51   4538 A           LOOP  DRA OK
```

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```
453A A    B6 5000 UPDATE LDAA DIGIT
453D A    B7 2000        STAA TXRX
                *
                * COUNTER
                *
4540 A    FE FFFF OK     LDX $FFFF
MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 2-APR-86 10:21:00 PAGE 2

4543 A    09      COUNTB DEX
                *
                * READ FROM THE STATUS REGISTER TO ACKNOWLEGDE IRQ
                *
4544 A    F6 2001        LDAB CRSR
4547 A    8C 00 00       CPX $0000
4549 A    26 F8          BNE COUNTB
                *
                * TURN OFF OUTPUT BUT ENABLE IRQ
                *
454B A    86 04   TONOFF LDAA #$04
454D A    B7 2001        STAA CRSR
4550 A    FE FFFF        LDX $FFFF
4553 A    09      COUNTP DEX
                *
                * READ FROM STATUS REGISTER TO ACKNOWLEGDE IRQ
                *
4554 A    F6 2001        LDAB CRSR
4557 A    8C 00 00       CPX $0000
4559 A    26 F8          BNE COUNTP
                *
                * ENABLE OUTPUT, IRQ AGAIN
                *
455B A    86 05          LDAA #$05
455D A    B7 2001        STAA CRSR
4560 A    7E 452D        JMP DATA
                *
     5100                ORG RAMMSG
5100 A    4E 4F   MSG1   FCC'NON BURST MODE, RX IRQ, ENTER DIGIT FOR TX'
512C A    00             FCB 0
                         END
```

```
MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2) 257 2-APR-86 10:21:00 PAGE 3
SYMBOL TABLE

COUNTB 4543    COUNTP 4553    CRLF 8662    CRSR =
2001 DATA  452D
DIGIT 5000     HEAD = 8655    MSG1 5100    OK
4540 RAMMSG = 5100
READ = 8723    START 4500     TONOFF 454B  TXRX =
2000 UPDATE 453A
X %0000
ASCT 512D 00
```

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MODULE
ERRORS DETECTED: 0

FREE CORE 8901 WORDS
)USR_VSI_6800:MA6800 TXNONBUR/LIB TXNONBUR/SP TXNONBUR/C

MODULE; MICROENGINE 6800 CROSS ASSEMBLER (V2.25 - NOV 86) 02-APR-86 10:21:00 PAGE S-1
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Projektowanie dużych macierzy przełączających

Korzystanie z analogowych tablic przełączników Mitel

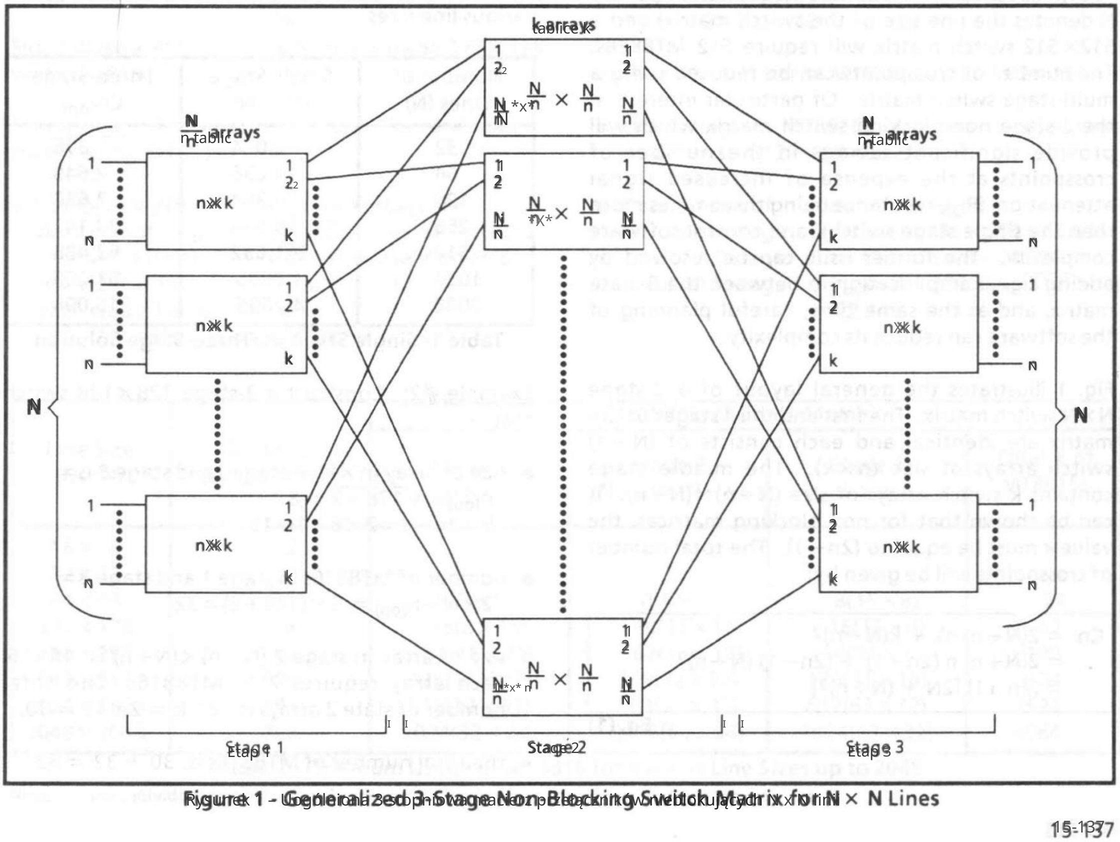
9161-001-050-NA WYDANIE 1 Styczeń 1990

Wstęp

Tradycyjnie projekt dużego przełącznika analogowego macierze opierają się na wykorzystaniu przełączniki elektromechaniczne. Jako takie, wiele ruchomych części zostały wykorzystane do budowy tych przełączników matryce. Dzięki postępom w elektronice przełączniki elektromechaniczne mogą być teraz zastąpione równoważne przełączniki półprzewodnikowe, które oferują bardziej ekonomiczne rozwiązania, a także ulepszone niezawodność. Mitel rodzina analog crosspoint urządzenia przełączające można łatwo skonfigurować w różnych rozmiary matryc przełączników ze względu na ich różnorodność konfiguracje tablic przełączników i ich doskonałe wydajność elektryczna.

Celem niniejszej notatki aplikacyjnej jest pokazanie, w jaki sposób można zastosować 3-stopniową matrycę przełączników bez blokowania wdrożone przy użyciu minimalnej liczby Mitel przełączniki tablicowe. Teoria optymalizacji 3-stopniowej zostanie krótko omówiona macierz przełączników i przykłady zostanie zaprezentowany. MT8816 8 x 16 crosspoint przełącznik jest używany jako główny przykład, ponieważ jego duży rozmiar zmniejszy całkowitą liczbę urządzeń do konkretnego projektu macierzy przełączników. Jednakże, ćwiczenie można łatwo powtórzyć z innymi produktami Mitel przełączać tablice.

Najczęściej stosowana metoda w analogowych projekt macierzy przełączającej to podział przestrzeni przełączania gdzie sygnały są fizycznie przełączane z jednego linii sygnałowej do drugiej. W przeciwieństwie do podziału czasu przełączanie stosowane w matrycach cyfrowych, jest mało opóźnienie dodane do sygnału z powodu przełączania mechanizm. Rzeczywiste opóźnienie jest określone przez czas propagacji przez półprzewodnik przełącznik i obwód lokalny. To, w połączeniu z niskimi wartości oporu włączenia, umożliwia macierze różnych konfiguracje do zbudowania przy małym sygnale degradacja.



Rysunek 1 - Uogólniona 3-stopniowa macierz przełączników nieblokujących N x N linii

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Single Stage Solution

The simplest switching structure is a single stage non-blocking array of crosspoints. This switch matrix consists of M × N rectangular array of crosspoints. It always makes connection from one of its M inputs/outputs to one of its N inputs/outputs regardless of which connections are already established, e.g. MT8816 can connect any one of 8 Xi inputs/outputs to any one of 16 Yi inputs/outputs. Altogether there are (8 × 16) crosspoint switches within the matrix. Normally for designing a system with a small matrix size, the number of analog switch arrays can be determined directly by their sizes.

Example #1: Construct a 32 × 32 switch matrix using MT8816. The number of MT8816s in the vertical (Y) direction is given by 32 ÷ 16 = 2. The number of MT8816s in the horizontal (X) direction is given by 32 ÷ 8 = 4. Therefore, 8 (4 × 2) MT8816s will be required.

Multi-stage Solution

However, when the number of lines gets very large, the number of switch arrays increase substantially. A 128 × 128 switch matrix will require 128 MT8816 for a N × N single stage matrix (where N denotes the line size of the switch matrix) and a 512 × 512 switch matrix will require 512 MT8816s. The number of crosspoints can be reduced using a multi-stage switch matrix. Of particular interest is 3-stage non-blocking switch matrix which will provide significant savings in the number of crosspoints. It does however introduce additional signal attenuation (RON resistance) being three times more than the single stage switch, and control software complexity. The former issue can be resolved by adding signal amplification in between the 3-state matrix, and as these are same planning of the software can reduce its complexity.

Fig. 1 illustrates the general layout of a 3-stage N × N switch matrix. The first and third stages of the matrix are identical and each consists of (N ÷ n) switch arrays of size (n × k). The middle stage contains k identical switch arrays of size (N ÷ n) × (N ÷ n). It can be shown that for non-blocking matrices, the value k must be equal to (2n − 1). The total number of crosspoints will be given by:

$$C_n = 2N(k + (N \div n)^2) = 2N(n(2n-1) + (2n-1)(N \div n)^2 = 2n(2n-1)[2N + (N \div n)^2]$$

...Eqn (1)

To obtain the optimal value of n, differentiate C_n w.r.t. n and set the equation to 0:

$$\frac{dC_n}{dn} = 2(2N + 2(2n-1)(N \div n)^2 - 2(2n-1)(N \div n)^3 = 0$$

$$2n^3 - nN = 0 \quad \text{or} \quad N = 0$$

...Eqn (2)

As N gets very large, Eq. (2) can be approximated by:

$$2n^3 - nN = 0$$

$$n_{(op)} = \sqrt{\left(\frac{N}{2}\right)}$$

...Eqn (3)

where $n_{(op)}$ denotes the optimum value of n.

The optimum value of C_n, $C_{n(op)}$ can be found by substituting Eq. (3) into Eq. (1):

$$C_{n(op)} = 4N[\sqrt{2N} - 1]$$

...Eqn (4)

where $C_{n(op)}$ denotes the minimum number of crosspoints.

Table 1 compares the number of crosspoints in a single-stage matrix versus a three-stage matrix for various line sizes.

Number of Lines (N)	Single Stage (N × N)	Three Stage $C_{n(op)}$
32	1,024	896
64	4,096	2,640
128	16,384	7,680
256	65,536	22,147
512	261,632	63,488
1024	1,048,576	181,248
2048	4,210,688	516,096

Table 1 - Single Stage vs. Three Stage Solution

Example #2: Construct a 3-stage 128 × 128 switch matrix.

- size of array (n × k) in stage 1 and stage 3 is: $n_{(op)} = \sqrt{128 \div 2} = 8$, $k = 2n - 1 = 2 \times 8 - 1 = 15$
- number of MT8816s in stage 1 and stage 3 = $2N(n_{(op)}) = 2(128 \div 8) = 32$
- size of array in stage 2 = $(N \div n) \times (N \div n)$ is: 16×16. Each array requires 2×2 MT8816s. The total number of MT8816s for stage 2 arrays is: $2 \times k = 2 \times 15 = 30$.
- the total number of MT8816s is: 30 + 32 = 62.

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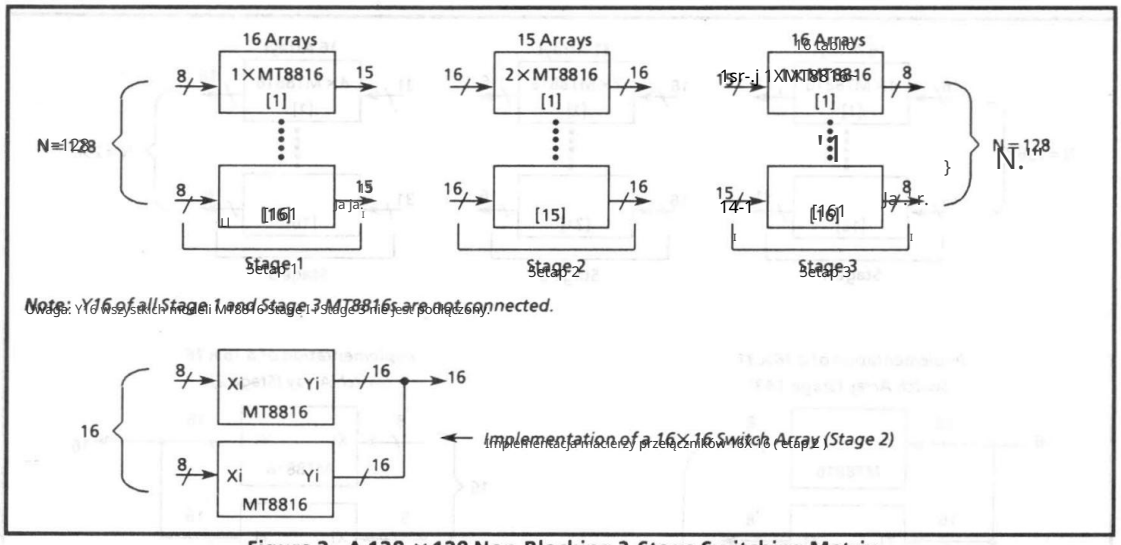

Figure 2 - A 128 × 128 Non-Blocking 3-Stage Switching Matrix

- The savings in MT8816s over the single stage solution is: 128 − 62 = 66

- comparison of number of crosspoints:
  single stage: $C_n = N \times N = 128 \times 128 = 16{,}384$
  3-stage: $C_n = 66 \times 16 \times 8 = 8{,}448$
  optimal 3-stage: $C_{n(op)} = 4 \times 128 \times [\sqrt{(256)} - 1)] = 7{,}680$

Fig 2 illustrates the structure of a 3-stage 128 × 128 switch matrix.

Example #3: Construct a 3-stage 256 × 256 switch matrix using MT8816s.

- size of array (n × k) in stage 1 and stage 3 is:
  notice that $n = \sqrt{128 \div 2}$ is not an integral number, a better line size in this case is given by:
  $n = \sqrt{256} = 16$, $k = 2n - 1 = 2 \times 16 - 1 = 31$.
  Each stage 1 array requires:
  $(32 \div 16) \times (16 \div 8) = 4 \times$ MT8816s

- number of MT8816s in stage 1 and stage 3:
  $2 \times (N \div n) \times 4 = 2 \times (256 \div 16) \times 4 = 128$

- Size of array in the second stage is: $(N \div n) \times (N \div n) = 16 \times 16$. Each stage 2 array requires $(16 \div 16) \times (16 \div 8) = 2 \times$ MT8816s.
  The total number of MT8816s for stage 2 is:
  $2 \times k = 2 \times 31 = 62$

- the total number of MT8816s = 128 + 62 = 190.

- the savings in MT8816s over the single stage solution is: 512 − 190 = 332.

- Comparison of number of crosspoints:
  single stage: $C_n = N \times N = 256 \times 256 = 65{,}536$
  3-stage: $C_n = 190 \times 16 \times 8 = 24{,}320$
  optimal 3-stage: $C_{n(op)} = 4 \times 256 \times [\sqrt{(512)} - 1)] = 22{,}147$

Line Size (N × N)	MT8816 (Single Stage)	MT8816s (3-Stage Matrix)			
		Stage 1 n × k	Stage 2 (N ÷ n) × (N ÷ n)	Stage 3 k × n	Total # of MT8816s
16 × 16	2	---	---	---	---
32 × 32	8	---	---	---	---
64 × 64	32	8(8 × 15)	8(8 × 8)	8(15 × 8)	24
128 × 128	128	16(8 × 15)	30(16 × 16)	16(15 × 8)	62
256 × 256	512	64(16 × 31)	62(16 × 16)	64(31 × 16)	190
512 × 512	2048	128(16 × 31)	248(32 × 32)	128(31 × 16)	504
1024 × 1024	8192	512(32 × 63)	504(32 × 32)	512(63 × 32)	1524
2048 × 2048	32768	1024(32 × 63)	2016(64 × 64)	1024(63 × 32)	4064

Table 2 - Optimum Usage of MT8816 for Various Line Sizes up to 2048

Note: the individual array sizes are shown inside the brackets for a number of 3-stage matrices.

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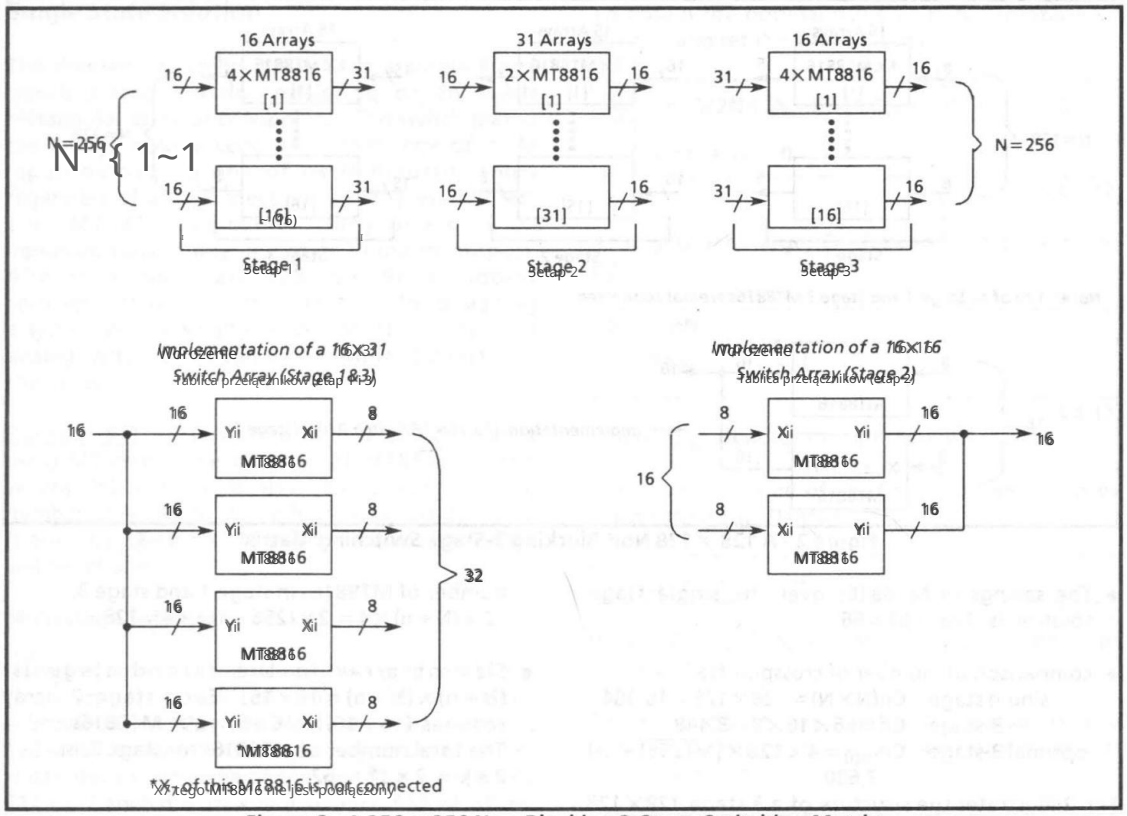

Figure 3 - A 256 x 256 Non-Blocking 3-stage Switching Matrix

Rys. 3 ilustruje strukturę 3-stopniowej matrycy przełączników 256 × 256.

Tabela 2 pokazuje optymalne wykorzystanie MT8816 do różnych rozmiarów linii do 2048.

Conclusion

Jak zaobserwowano, chociaż trzystopniowa matryca, taka jak tablica przełączników, może być bardzo duża, sprawia, że jest ekonomiczna. Rozwiązanie to przyjęto w celu zmniejszenia złożoności projektowej lub wprowadzenia częściowego blokowania bez zwiększania liczby tablic przełączników.

References

Charles Clos, "A Study of Non-Blocking Switching Networks", Bell System Technical Journal, March 1953, pp 406-424.

John Bellamy, Digital Telephony, 220-242, 220-242, pub. by John Wiley & Sons, 1982, ISBN 0-471-89089-6.

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